MOSTEK

INDUSTRIAL PRODUCTS

Counter Time-Base Circuit

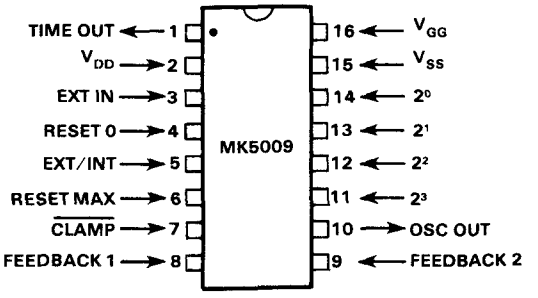
MK5009(N/P)

FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Internal clock operates from:
  External signal
  External RC network
  External crystal
- ☐ Operates dc to above 1 MHz
- ☐ Binary-encoded for frequency selection
- ☐ Resettable to highest or lowest state
- ☐ Twenty different modes of division

PIN CONNECTIONS

Figure 1



DESCRIPTION

Refer to Figure 2 for Block Diagram.

The MK5009 is a highly versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load ion-implantation process and P-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36 x 10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

The MK5009 consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36 x 10^8 counter stages, which are fully synchronous with each other.

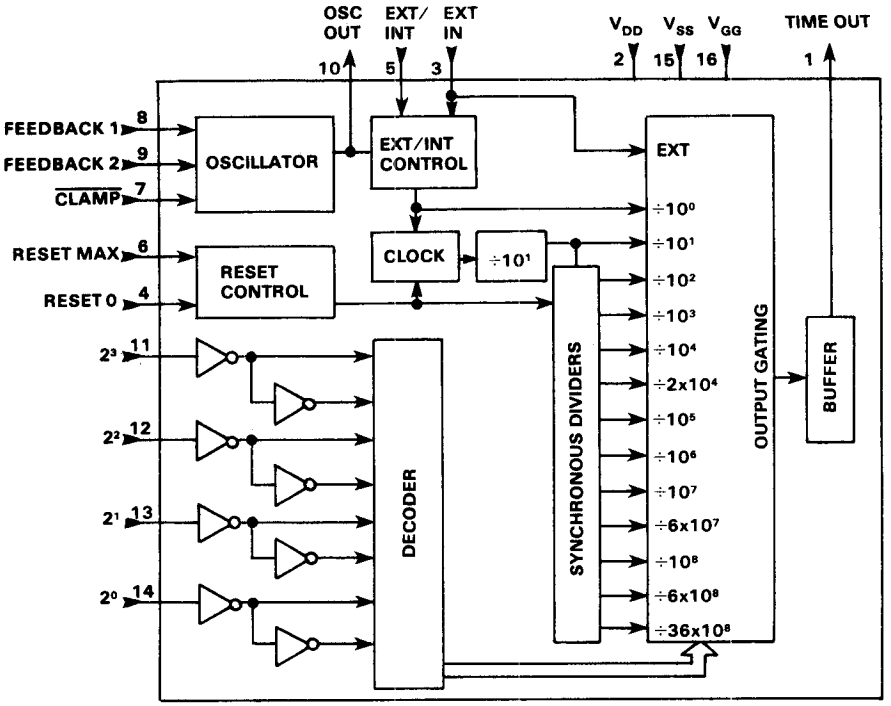
With an input frequency of 1 MHz, the MK5009 provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK5009 can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave; its frequency is determined by the selected counter division, and by the oscillator or external input frequency. The falling edge of the output square wave should be used to control external circuitry.

Pin connections for the MK5009 are shown in Figure 1.

BLOCK DIAGRAM

Figure 2



FUNCTIONAL DESCRIPTION

TIME OUT, Pin 1

TIME OUT is the output of the divider chain. It is a square wave whose period depends upon the division mode. For this reason, external circuitry should be triggered on the falling edge of this signal.

V_{DD}, Pin 2

V_{DD} is normally ground for the chip and the other supply voltages are measured with respect to V_{DD}.

EXT IN, Pin 3

When using an external frequency source to operate the MK5009, that signal should be applied at EXT IN and EXT/INT should be brought to a logic 1 level. The counters are incremented on the falling edge of EXT IN and the signal applied to this pin must be TTL-compatible. When unused, this pin can be tied either high or low.

RESET 0, Pin 4

A positive going pulse of 10 μs or longer applied to RESET 0 will reset the counters to their lowest state. Taking RESET 0 to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes according to Table 1.

EXT/INT, Pin 5

A logic 1 level on EXT/INT will gate the signal present at EXT IN through to the counters. A logic 0 level applied to EXT/INT will gate the internal oscillator (RC/crystal) through to the counters.

RESET MAX, Pin 6

A positive going pulse of 10 μs or longer on RESET MAX will reset counters to their highest state. RESET MAX enables the user to set up the counters to provide a falling TIME OUT edge at the next oscillator cycle or negative going EXT IN, regardless of which divider chain is selected.

Taking RESET MAX to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes given in Table 1.

$\overline{\text{CLAMP}}$, Pin 7

$\overline{\text{CLAMP}}$ is used in conjunction with the RC mode of operation. Its purpose is to provide accurate start-up operations.

When $\overline{\text{CLAMP}}$ is taken to a logic 0 level, the internal circuitry is held at a fixed reference voltage. Then, when $\overline{\text{CLAMP}}$ is taken to a logic 1 level, the oscillator's first cycle will be a full cycle.

DIVISION MODES VS. CONTROL INPUTS

Table 1

DIVISION* SELECTORS				NORMAL	BYPASS MODES		
				Mode 0	Mode 1	Mode 2	Mode 3
2^3	2^2	2^1	2^0	$R_{MAX} = 0$ $R_0 = 0$	$R_{MAX} = V_{GG}$ $R_0 = 0$	$R_{MAX} = 0$ $R_0 = V_{GG}$	$R_{MAX} = V_{GG}$ $R_0 = V_{GG}$
0	0	0	1	$\div 10^1$	$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$	$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$	$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$	$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6 \times 10^7$	$\div 6 \times 10^4$	$\div 6 \times 10^4$	$\div 6 \times 10^1$
1	0	1	0	$\div 36 \times 10^8$	$\div 36 \times 10^5$	$\div 36 \times 10^5$	$\div 36 \times 10^2$
1	0	1	1	$\div 6 \times 10^8$	$\div 6 \times 10^5$	$\div 6 \times 10^5$	$\div 6 \times 10^2$
1	1	1	0	$\div 2 \times 10^4$	$\div 2 \times 10^1$	$\div 2 \times 10^1$	$\div 2 \times 10^1$

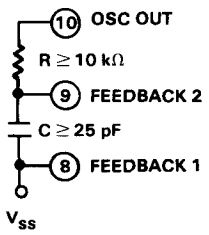
*SPECIAL ADDRESSES:

0000 - Oscillator signal selected by EXT/INT appears at TIME OUT.
1100 or 1101 - Forces TIME OUT to logic 0 level.
1111 - Signal at EXT IN appears at TIME OUT.

Logic 1 = High = V_{SS}
Logic 0 = Low = V_{DD}

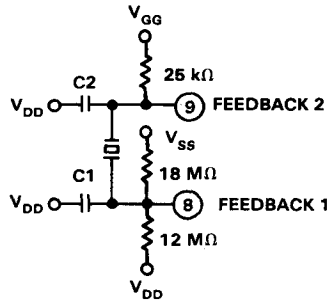
RC OPERATION

Figure 3



CRYSTAL OPERATION

Figure 4



FEEDBACK 1 and FEEDBACK 2, Pins 8 and 9

FEEDBACK 1 and FEEDBACK 2 are oscillator ports. Operation in the RC mode is achieved as shown in Figure 3. Frequency is approximately 0.8/RC. R must be greater than or equal to 10 kΩ and C must be greater than or equal to 25 pF for proper operation. Operation in the crystal oscillator mode is shown in Figure 4. The crystal operates in the parallel resonant mode, should operate properly with a 5 mW drive, and should have a loading capacitance (C_L) of $\leq$ 32 pF. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. The series combination of C1 and C2 should not exceed the value of C_L.

OSC OUT, Pin 10

The oscillator output, provided at Pin 10, is not a true logic output but may be used to drive a high impedance device such as other MOS circuitry. OSC OUT reflects the state of the internal oscillator.

2^3, 2^2, 2^1, and 2^0, Pins 11 through 14

The division selector inputs are used to select the ratio of the TIME OUT frequency to the oscillator input frequency. The effect of specific combinations of logic levels on these pins is shown in Table 1. Note that when all division selector inputs

are high, the signal applied to EXT IN appears at the TIME OUT output. Also when RESET 0 and RESET MAX are used in conjunction with the division selector inputs, several more modes can be accessed. (See Table 1)

V_{SS}, Pin 15

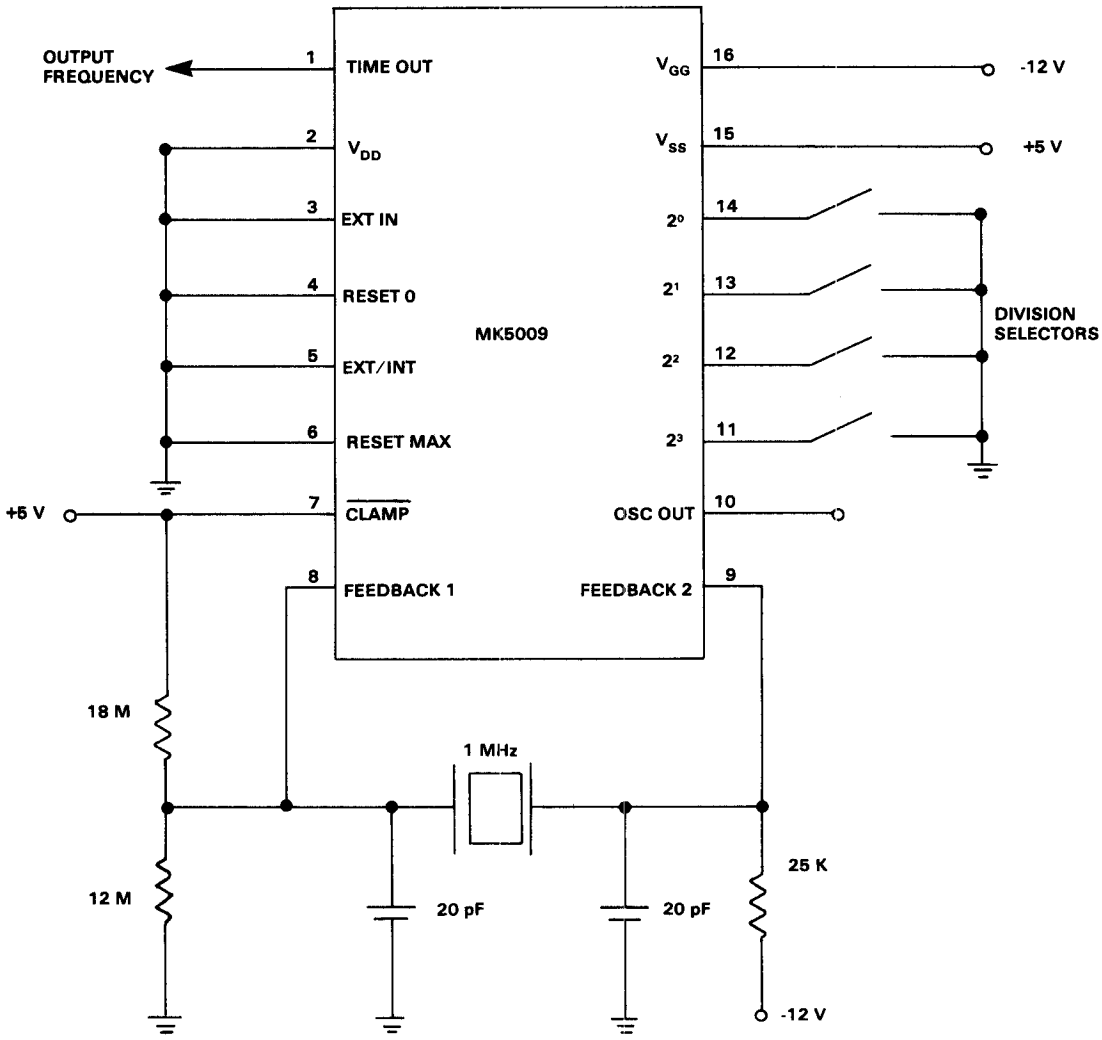
V_{SS} is the positive supply voltage and should be maintained at 5 Vdc ± 10% with respect to V_{DD}.

V_{GG}, Pin 16

V_{GG} is the negative supply voltage and should be maintained at -12 Vdc with respect to V_{DD}.

Figure 5 shows a very simple test circuit which demonstrates the MK5009 in the crystal oscillator mode. The division selector switches control the divide mode. The output frequency will be related to the 1 MHz oscillator frequency according to Table 1.

SIMPLE TEST CONFIGURATION
Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Terminal Relative to V_{SS} ..... +0.3 V to -20 V
Operating Temperature Range (Ambient) ..... 0°C to +70°C
Storage Temperature Range (Ambient) ..... -55°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{SS} = +5 V ±10%; V_{DD} = 0 V; V_{GG} = -12.0 V ±20%; 0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.5		+5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	-9.6		-14.4	V	
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
R	Feedback Resistance	0.1		2.5	MΩ	Fig. 3
V_{IL}	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V_{GG}		V_{GG}+1.0	V	Note 2
	All Other Logic Inputs			0.8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}-1.0	V_{SS}	V_{SS}+0.3	V	
I_{IL}	Input Current, Logic 0			-1.6	mA	Note 2; V_I=0.4 V
V_{OL}	Output Voltage, Logic 0			0.4	V	I_{OL}=1.6 mA*
V_{OH}	Output Voltage, Logic 1	2.4			V	I_{OH}=-40 μA*

AC CHARACTERISTICS

(V_{SS} = +5 V ±10%; V_{DD} = -12.0 V ±20%; 0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP†	MAX	UNITS	NOTES
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	dc		200	kHz	
f_{EXT}	External Frequency	dc		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{CLAMP}$	$1/2f_{OSC}$				Note 5
	EXT IN	200			ns	
t_{PH}	Logic 1 Pulse Width, EXT IN	200			ns	
	RESET MAX	10.0			μs	
	RESET 0	10.0			μs	
f_{STA}	Frequency Stability					
	w/Volt. Change, RC Mode		±3.0		%/V	Note 3
	/Temp. Change, RC Mode		-0.2		%/°C	
	Crystal Mode		—			Note 4
t_{ee}	Jitter, Edge-to-Edge Variation			15	ns	Temp. & Supply Voltage Constant

NOTES

† Typical values at V_{SS} = +5 V, V_{DD} = 0 V, V_{GG} = -12 V, and T_A = 25°C

1. Logic inputs at V_{SS}, output open-circuited. Each logic input (see Note 2) contributes an additional 1.6 mA (max) to I_{SS} when at logic 0 level.
2. Logic inputs are: RESET MAX; RESET 0; Address inputs; EXT IN; EXT/INT; and CLAMP.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at CLAMP input is 50% of oscillator period. (f_{OSC} ≡ oscillator frequency)

*V_{OH}, V_{OL} apply only to TIME OUT.

MOSTEK

USING MOSTEK'S MK5009(N/P) COUNTER TIME-BASE CIRCUIT

Application Note

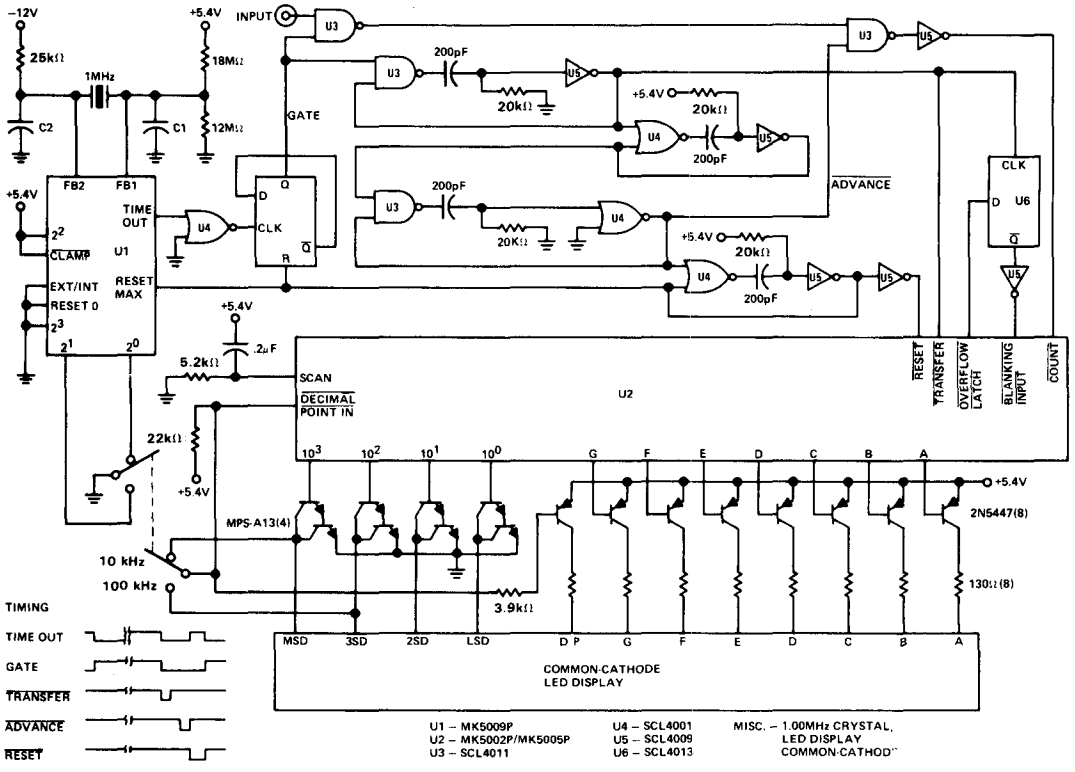
DIGITAL FREQUENCY METER

The 100kHz frequency meter which can be battery operated is illustrated schematically in Figure 1. The +5.4V power required is supplied by four C cells and a series diode. Since most of the 200mA required is used in the LED display, it is advantageous to employ a "push-to-read" function on the meter. This is easily accomplished by using either a Mostek MK5002 or MK5005 as the counting device and display driver. If an unconditional reset is applied to the U-6 flip-flop, to be released only when the display is to be read, the display normally will be blanked.

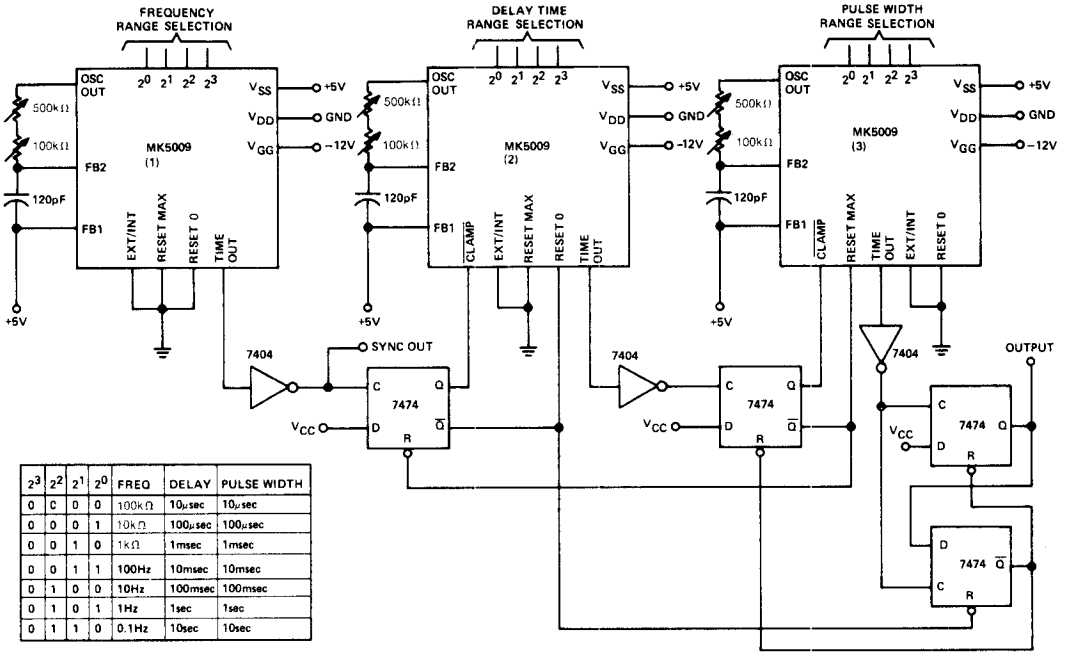
The circuit's input responds to a +5V signal. A more general purpose front end, if desired, could be added to the NAND gate U3. The range of the meter could also be expanded by using decade prescalers at the input.

The timing diagram in Figure 1 also shows the interface timing between the MK5009 and MK5002. Basic C/MOS one-shots are used to conserve power; but if battery operation is not required, standard TTL one-shots can be used. The four one-shots generate the following times; transfer pulse width (at the end of a measurement period); time delay between the transfer pulse and count negative edge; count negative edge; and reset pulse width. To obtain an accurate time-out interval on the MK5009, a flip-flop is used to count two consecutive negative edges of the Time-Out output.

This simple circuitry gives a 4-digit frequency meter with crystal-controlled accuracy, typically requiring 8mA from the positive supply and 5mA from the negative supply, excluding display power.



PULSE GENERATOR



2^3	2^2	2^1	2^0	FREQ	DELAY	PULSE WIDTH
0	0	0	0	100kΩ	10μsec	10μsec
0	0	0	1	10kΩ	100μsec	100μsec
0	0	1	0	1kΩ	1msec	1msec
0	0	1	1	100Hz	10msec	10msec
0	1	0	0	10Hz	100msec	100msec
0	1	0	1	1Hz	1sec	1sec
0	1	1	0	0.1Hz	10sec	10sec

PULSE GENERATOR

An extremely versatile pulse generator requiring few components is easily built using the MK5009. Three MK5009 circuits are used, as shown in Figure 2, to provide the three essential pulse generator elements: (1) a frequency source to determine pulse repetition rate; (2) a variable time delay; and (3) a pulse width generator.

This circuit provides repetition rates from 0.1Hz to 100kHz with delay times and pulse widths from 10μ to 10 seconds. Range selection is obtained by selecting the appropriate dividers, so that only three RC circuits are required. This eliminates the requirement for a different RC combination for each decade, commonly found in commercial instruments. Decade selection is accomplished by a binary code at the inputs to each MK5009, which could be provided by a coded rotary or thumbwheel switch. The vernier control is a 500k potentiometer. A 100k potentiometer is used as a trimmer for initial calibration. External TTL control logic is used to capture the accurately-controlled negative edges as they emerge from each MK5009. The Reset and Clamp Inputs allow synchronization and first-cycle accuracy from the time-base circuits.

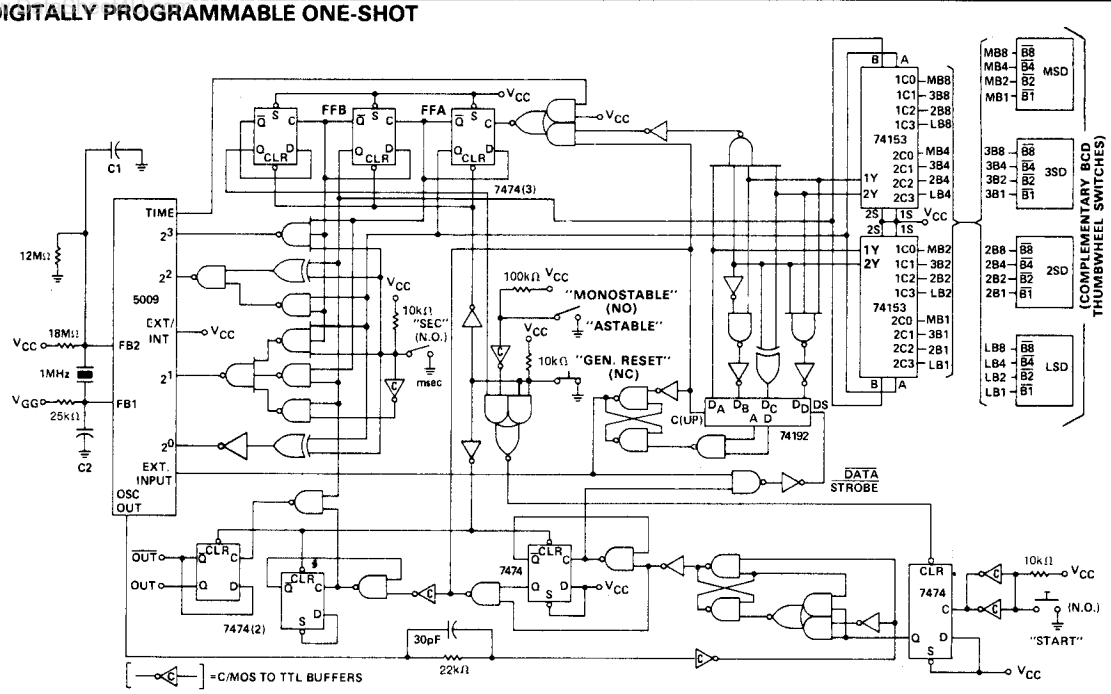
Other features can be added to the basic circuitry shown in Figure 2. For example, the output amplitude can be made adjustable by using high-voltage, open-collector TTL circuitry with potentiometer control for amplitude. An extra position can be used on the frequency selection switch for an external trigger source. This trigger source should be connected to the first control D-type latch in lieu of the output from the MK5009 (1). The frequency range may even be extended to 1.0MHz with time delays reduced to 1 μs, although some loss in RC stability would occur since the recommended data sheet frequency has been exceeded.

DIGITALLY PROGRAMMABLE ONE-SHOT

Using the MK5009 in the circuit shown in Figure 3 results in a very accurate one-shot which is digitally programmable. Four decades of thumbwheel switches allow pulse-width selection from 0.1 to 999.9 seconds, or 0.1 to 999.9 milliseconds, depending on the range selected. To indicate how the circuit functions, a general description of a typical one-shot application is used.

The user determines the required one-shot pulse width, for example 800.7 seconds. He must also determine desired output pulse polarity, i.e., (OUT or $\overline{\text{OUT}}$). The time is entered in the thumbwheel switch, the range switch is put in "Seconds", the mode select switch is put at "Monostable" and "Reset/Halt" is depressed momentarily.

To start the cycle, the "Start" button is depressed. This gates in the 1MHz clock from the MK5009 through the C/MOS-to-TTL buffer. The first clock pulse is used to strobe the MSD into the variable-modulo counter (74192). (Actually the nine's complement is supplied to the counter through the BCD switch multiplex circuitry.) The ÷N counter divides the 1MHz clock by the integer value of the MSD. The states of flip-flops FFA and FFB determine which digit (or decade range) is being



processed.

When the Time Out output from the MK5009 completes its time cycle, it advances the state counter, selects the next digit to be processed, and then changes the variable modulo counter to correspond to this new digit. If the next digit happens to be a zero, the flip-flops (FFA and FFB) are toggled at the 1 MHz rate until a non-zero digit is found. In the example given (800.7 seconds) after timing of the 800 seconds is complete, the flip-flops would toggle through the second and third digits to ".7", the first non-zero digit, and count the remaining 7/10 second.

However, the one-shot may also be operated in an "astable" mode which results in a square-wave output with a period equal to twice the dial setting. Once the circuitry is started it will free-run until either the mode is changed or the Reset button is depressed.

Because of the synchronous nature of the MK5009 counters, there should be no timing errors associated with the decade selection switching. The synchronous nature of the MK5009 counters and processing the digits from MSD to LSD enables the circuit to operate without being reset and therefore does not introduce an additional time delay.

Further, the potential problem of timing errors at the beginning of a cycle is eliminated, since there is ample time (500 ns) to load a new digit integer code before the load command is taken away. This is true for either timing range, seconds or milliseconds.

FURTHER DESIGN APPLICATIONS

This basic design can be extended to accomplish a programmable sequence timer. Any kind of ROM (programmable, fixed mask, or diode matrix) can be used to contain all the times (BCD) codes for the required steps. A state counter of sufficient capacity can be used to control the addressing of the ROM.

Numerous applications for systems of this kind exist wherever a timed sequence of events is required, such as a photographic processing, process control, test sequences, and innumerable industrial applications.

USE WITH 2.0MHz CRYSTAL

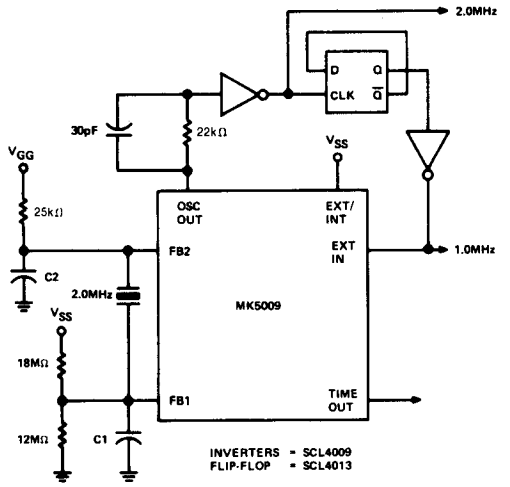
In some applications a different crystal frequency (such as 2.0MHz) may be more readily available, although the actual requirements on the output might be decade divisions of 1.0MHz. Figure 4 shows one way to accomplish this.

A 2.0MHz crystal is used in the recommended circuit and the frequency at the Oscillator Output pin is divided by 2 by the flip-flop. The 1.0 MHz is then fed back into the chip at the External Input pin. The interface is constructed with C/MOS circuitry since it presents a very high input impedance which does not load down the oscillator output.

Use of C/MOS-to-TTL type inverters allows direct drive of the External input on the MK5009 with its internal pull-up resistor.

This circuitry also provides a buffered 1.0MHz (or 2.0MHz) signal which can be used as a self-check input for a frequency meter without excessively loading the Oscillator Output.

USE WITH 2.0MHz CRYSTAL



INTERNAL CONFIGURATION OF THE MK5009 OSCILLATOR CIRCUIT

As can be seen in Figure 5 (a), the basic oscillator section of the MK5009 is fairly simple. It consists of two parts: an active device, Q1, for gain in the crystal mode of operation; and a Schmitt trigger and inverting buffer for wave-shaping the waveform at Feedback 2.

In the RC oscillator mode, Figure 5 (b), Feedback 1 is tied to V_{SS}. This keeps Q1 off and effectively removes it from the circuit. One end of the timing capacitor and one end of the timing resistor are tied to Feedback 2. Osc. Out is connected to the other end of the resistor. The input at Feedback 2 is "squared-up", inverted, and used to drive Osc. Out, which causes the RC voltage waveform to change polarity. The nominal upper and lower trip points for the Schmitt trigger are -1.5V and -7.0V respectively.

In the crystal oscillator mode, Figure 5 (c), Q1 is used as the active device. A resistor, nominally 25kΩ, is placed from Feedback 2 to V_{GG}, serving as the load element for Q1. In practice the resistor should not have a value lower than 15kΩ. The RC product of this load resistor and the crystal loading capacitance should be smaller than $1/f_{XTAL}$, or the RC combination will affect the oscillator frequency. An inductance, or other external load network, can also be substituted for the load resistor. The device, Q1, has a width/length ratio of about 20 and a nominal g_M of 60 μmhos.

INTERNAL CONFIGURATION OF THE MK5009 OSCILLATOR CIRCUIT

Figure 5(a)

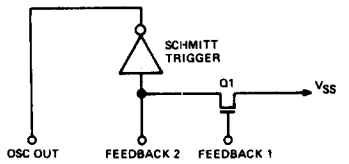


Figure 5(b)

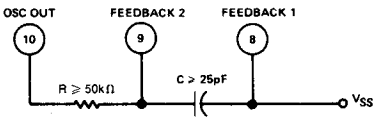


Figure 5(c)