

Designer's Data Sheet

Full Pak

NPN Silicon Power Transistor

1.0 kV Switchmode III Series

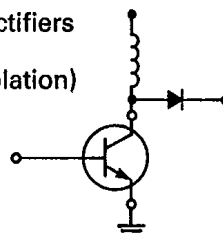
For Isolated Package Applications

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

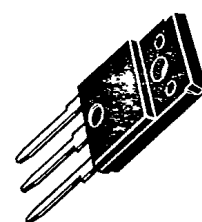
Features:

- Collector-Emitter Voltage — $V_{CEV} = 1000 \text{ Vdc}$
- Fast Turn-Off Times
 - 80 ns Inductive Fall Time — 100°C (Typ)
 - 120 ns Inductive Crossover Time — 100°C (Typ)
 - 800 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
 - Reverse-Biased SOA with Inductive Load
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents
- Extended FBSOA Rating Using Ultrafast Rectifiers
- Extremely High RBSOA Capability
- Isolated Overmold Package (4000 V_{RMS} Isolation)



MJF16006A

POWER TRANSISTOR
8.0 AMPERES
500 VOLTS
50 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	1000	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
RMS Isolation Voltage (for 1 sec, $T_A = 25^\circ\text{C}$, Relative Humidity $\leq 30\%$)	Per Figure 18 V_{ISOL1}	4000	V
	Per Figure 19 V_{ISOL2}	3000	V
Collector Current — Continuous	I_C	8.0	Adc
Collector Current — Peak(1)	I_{CM}	16	Adc
Base Current — Continuous	I_B	6.0	Adc
Base Current — Peak(1)	I_{BM}	12	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}^*$	P_D	50	Watts
Derate above $T_C = 25^\circ\text{C}$		20	Watts
		0.4	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	260	$^\circ\text{C}$

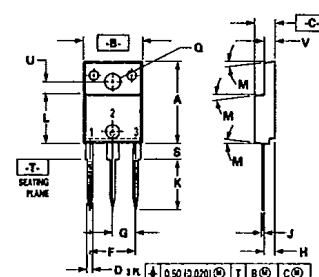
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle $\leq 10\%$.

* Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8 in·lbs.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Designer's, Full Pak and SWITCHMODE are trademarks of Motorola Inc.

OUTLINE DIMENSIONS



STYLE 1
 PIN 1 BASE
 2 COLLECTOR
 3 EMITTER

NOTES
 1. DIMENSIONING AND TOLERANCING PER
 ANSI Y14.5M, 1982
 2. CONTROLLING DIMENSION INCH

DIM	MILLIMETERS	INCHES
A	15.97	0.795
B	13.97	0.550
C	4.81	0.189
D	1.10	0.043
E	10.98	0.432
F	5.44	0.214
G	2.52	0.099
H	0.51	0.020
J	11.94	0.470
K	11.92	0.470
L	11.92	0.470
M	7.14	0.281
N	3.41	0.134
O	3.56	0.140
P	2.95	0.116
Q	2.52	0.099

CASE 340B-03



MOTOROLA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS(1)

Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	500	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = 1000\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = 1000\text{ Vdc}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	— —	0.003 0.02	0.15 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 1000\text{ Vdc}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	0.02	1.0	mAdc
Emitter Cutoff Current ($V_{EB} = 6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	0.005	0.15	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			

ON CHARACTERISTICS(1)

Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.6\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	0.35 0.5 0.6	0.7 1.0 1.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 5.0\text{ Adc}$, $I_B = 1.0\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	1.0 1.0	1.5 1.5	Vdc
DC Current Gain ($I_C = 8.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	5.0	8.0	—	—

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	—	—	350	pF
Collector to Heatsink Capacitance	C_{c-hs}	—	5.0	—	pF

SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	$(I_C = 5.0\text{ Adc},$ $I_{B1} = 0.66\text{ Adc},$ $V_{BE(off)} = 5.0\text{ Vdc},$ $V_{CE(pk)} = 400\text{ Vdc})$	$(T_J = 100^{\circ}\text{C})$	t_{sv}	—	800	2000	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	120	300	
Storage Time		$(T_J = 150^{\circ}\text{C})$	t_{sv}	—	1000	—	
Fall Time			t_{fi}	—	90	—	
Crossover Time			t_c	—	150	—	
Resistive Load (Table 2)							
Delay Time	$(I_C = 5.0\text{ Adc},$ $V_{CC} = 250\text{ Vdc},$ $I_{B1} = 0.66\text{ Adc},$ $PW = 30\text{ }\mu\text{s},$ $\text{Duty Cycle} \leq 2.0\%)$	$(I_{B2} = 1.3\text{ Adc},$ $R_{B2} = 4.0\text{ }\Omega)$	t_d	—	25	100	ns
Rise Time			t_r	—	400	700	
Storage Time			t_s	—	1400	3000	
Fall Time			t_f	—	175	400	
Storage Time		$(V_{BE(off)} = 5.0\text{ Vdc})$	t_s	—	475	—	
Fall Time			t_f	—	100	—	

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

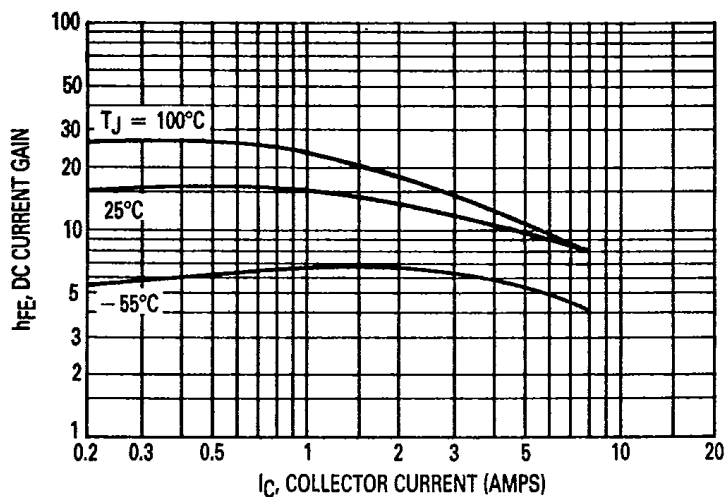


Figure 1. DC Current Gain

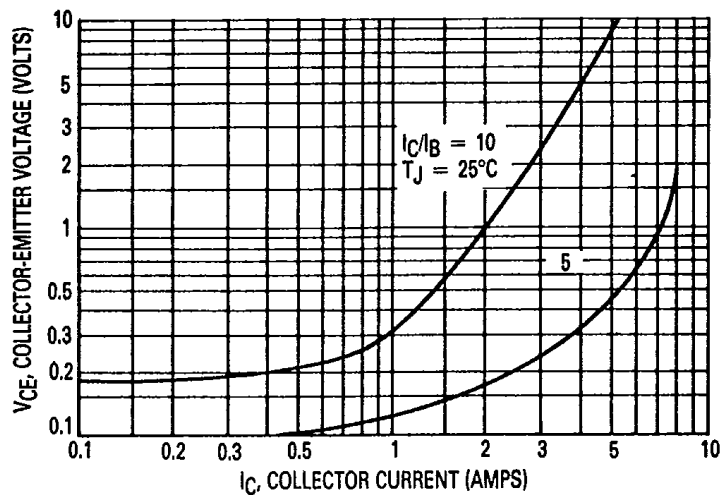


Figure 2. Collector-Emitter Saturation Region

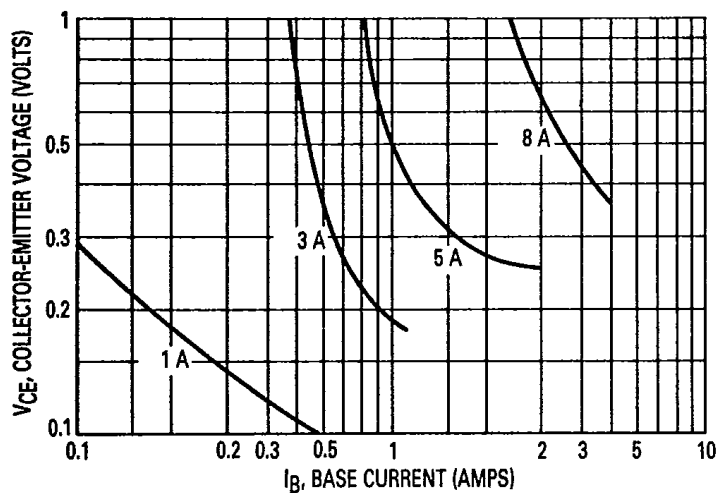


Figure 3. Collector-Emittor Saturation Region

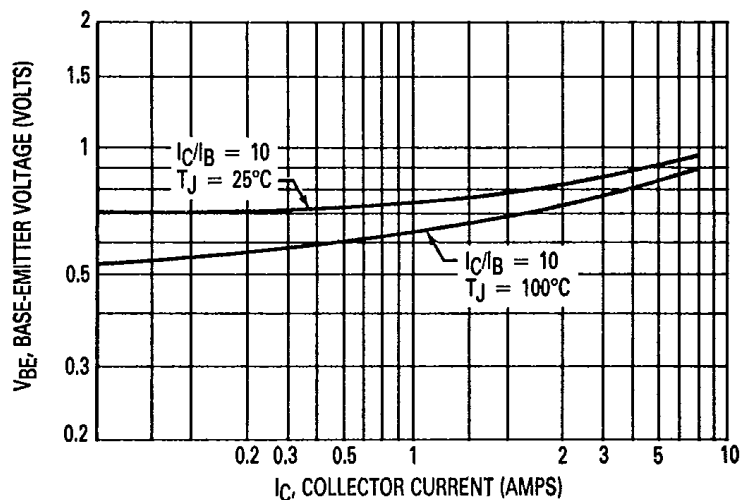


Figure 4. Base-Emitter Saturation Region

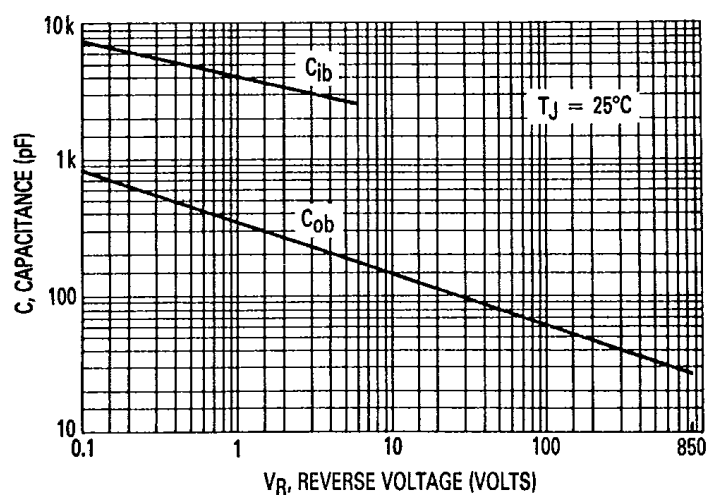


Figure 5. Capacitance

$I_C/I_{B1} = 5, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

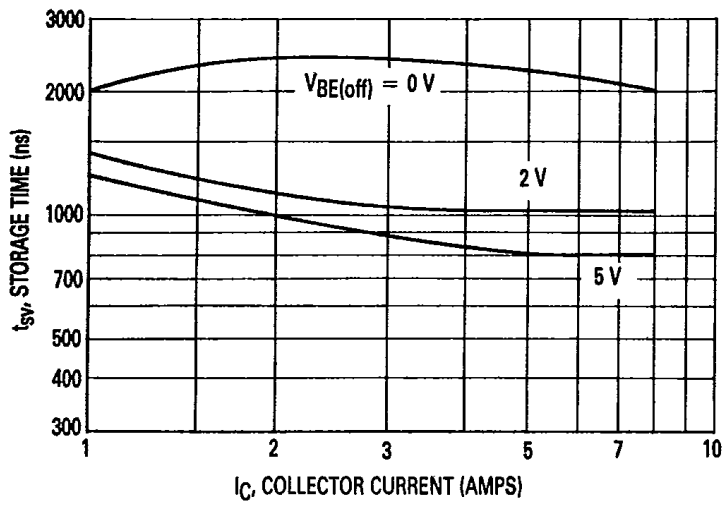


Figure 6. Storage Time

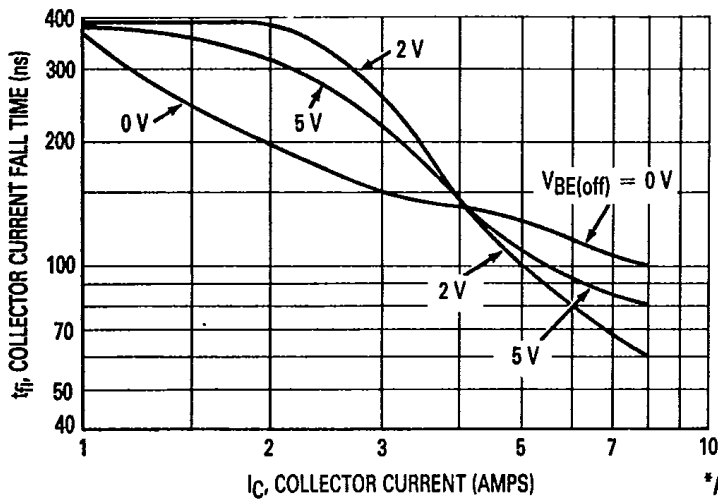


Figure 8. Collector Current Fall Time

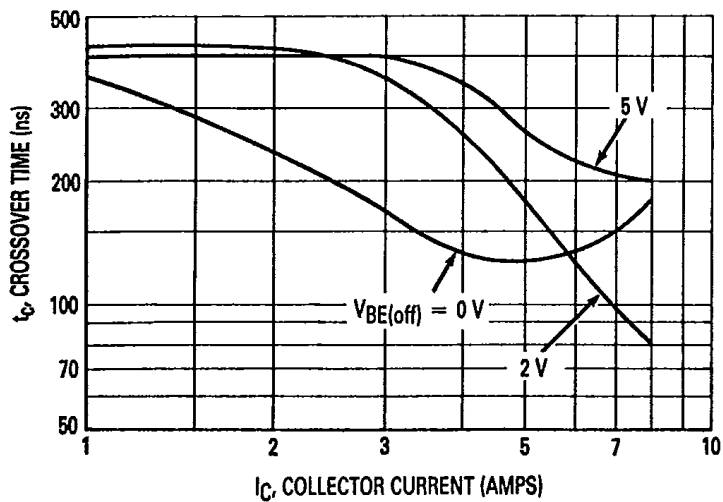


Figure 10. Crossover Time

$I_C/I_{B1} = 10, T_C = 75^\circ\text{C}, V_{CE(pk)} = 400\text{ V}$

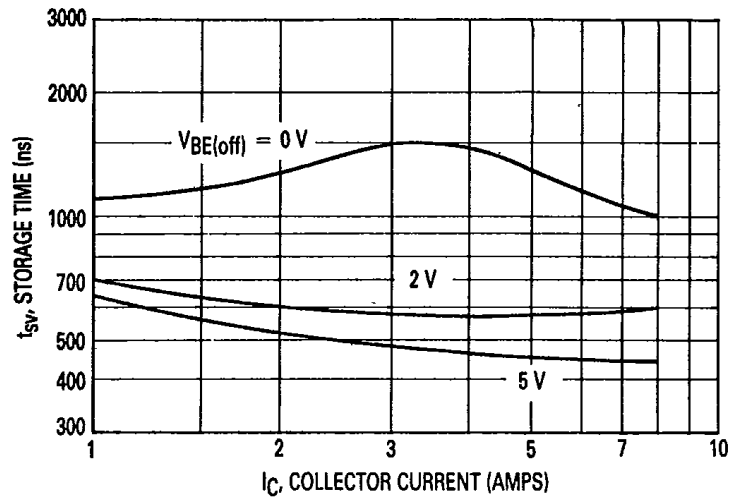


Figure 7. Storage Time

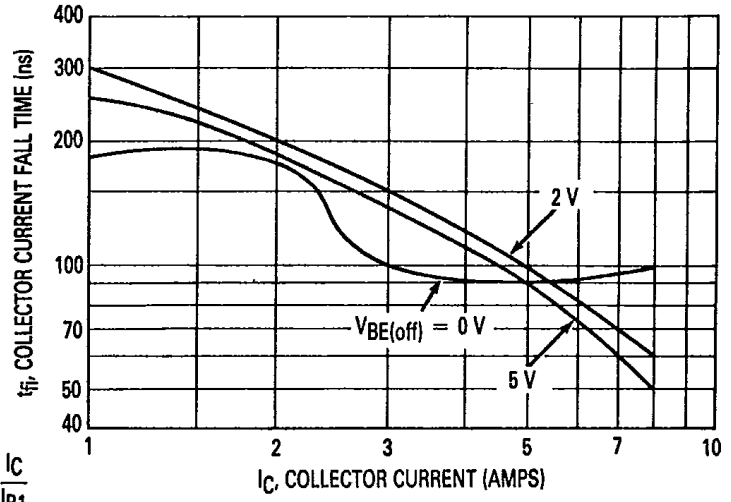


Figure 9. Collector Current Fall Time

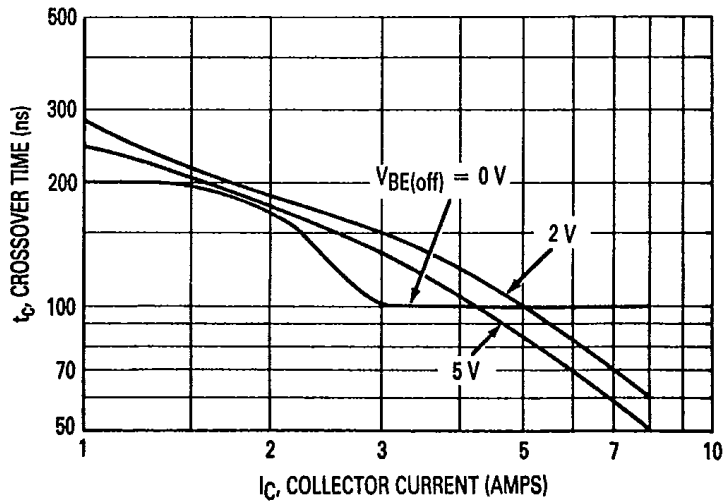


Figure 11. Crossover Time


$$T_1 \approx \frac{L_{\text{coil}} (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

Rg₁ selected for desired Ig₁

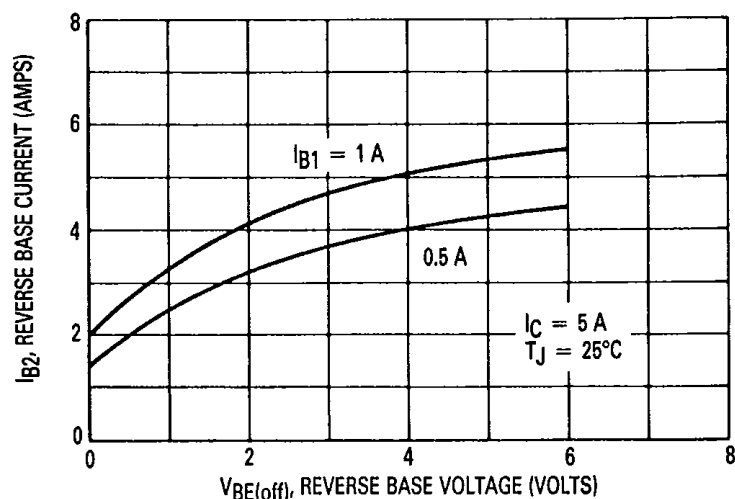
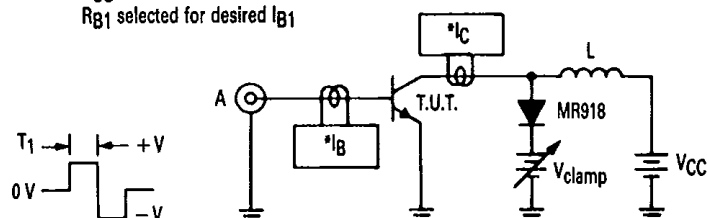
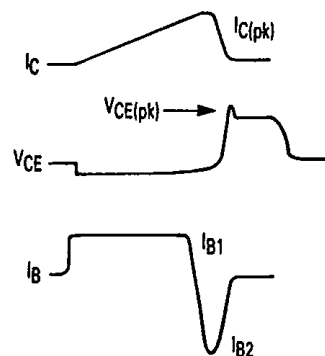
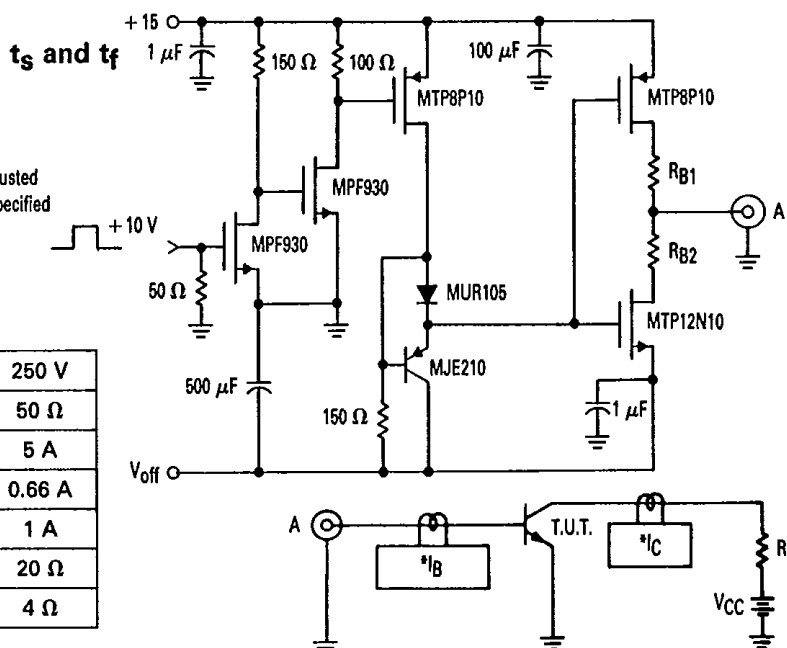


Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching



VCC	250 V
R _L	50 Ω
I _C	5 A
I _{B1}	0.66 A
I _{B2}	1 A
R _{B1}	20 Ω
R _{B2}	4 Ω

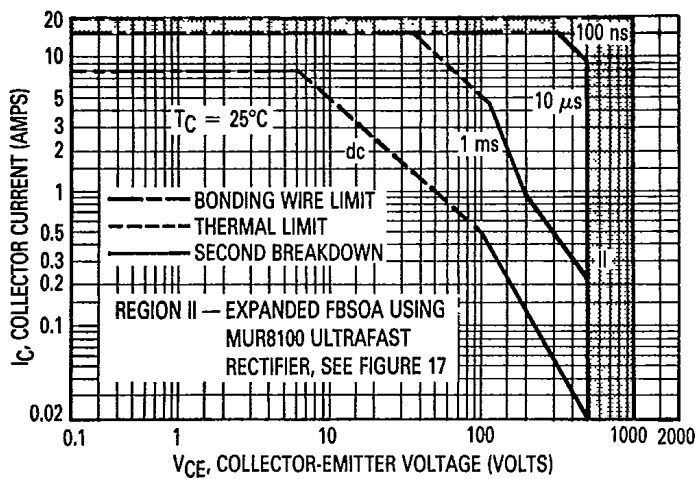


Figure 14. Maximum Rated Forward Biased Safe Operating Area

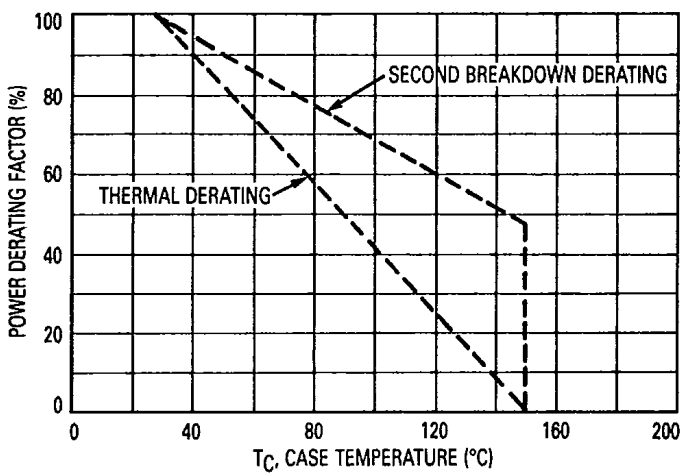


Figure 16. Power Derating

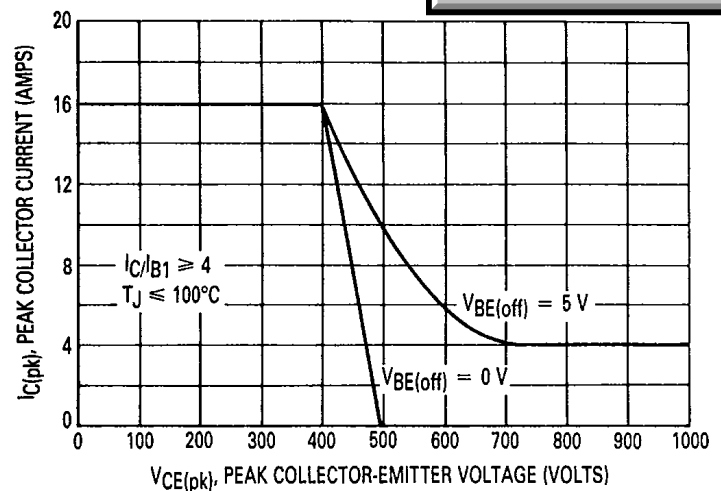


Figure 15. Maximum Reverse Biased Safe Operating Area

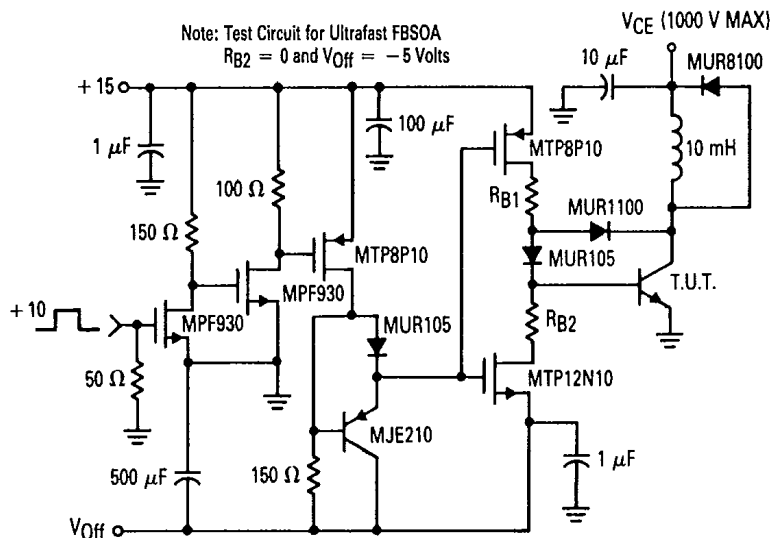


Figure 17. Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 16.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{(BR)CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{(BR)CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875 and article reprint AR317).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

4. OPERATION ABOVE $V_{(BR)CEO(sus)}$ —

When bipolar transistors are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1.0 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

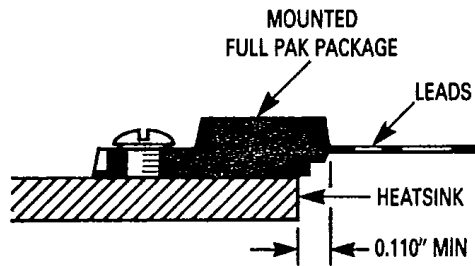


Figure 18. Screw or Clip Mounting Position for Isolation Test Number 1

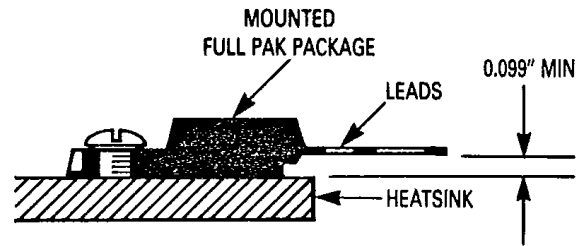
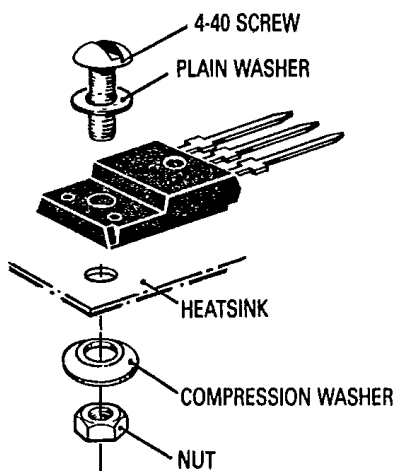


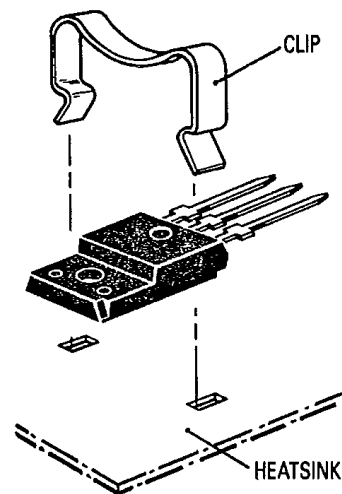
Figure 19. Screw or Clip Mounting Position for Isolation Test Number 2

*Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**



20a. Screw-Mounted Full Pak



20b. Clip-Mounted Full Pak

Figure 20. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in • lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in • lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in • lbs without adversely affecting the package. However, in order to positively insure the package integrity of the Full Pak, Motorola does not recommend exceeding 10 in • lbs of mounting torque under any mounting conditions.

**For more information about mounting power semiconductors see Application Note AN1040.

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; P.O. Box 80300; Cheung Sha Wan Post Office; Kowloon Hong Kong.

JAPAN: Nippon Motorola Ltd.; 3-20-1 Minamiazabu, Minato-ku, Tokyo 106 Japan.



MOTOROLA