By MJF16002/D

MJF16002

Motorola preferred device

Designer's Data Sheet

NPN Silicon Power Transistor

Switchmode™ Series
For Isolated Package Applications

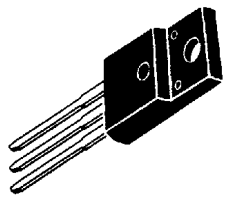
POWER TRANSISTOR
5.0 AMPERES
450 VOLTS
40 WATTS

This transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

Typical Applications: Switching Regulators, Inverters, Solenoids, Relay Drivers, Motor Controls, Deflection Circuits

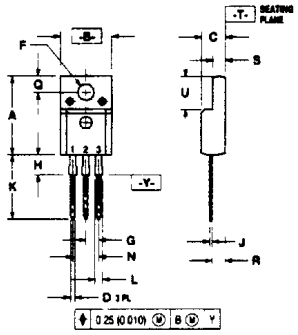
Features:

- Collector-Emitter Voltage — V_{CEV} = 800 Vdc
- Fast Turn-Off Times
  - 100 ns Inductive Fall Time – 100°C (Typ)
  - 120 ns Inductive Crossover Time – 100°C (Typ)
  - 500 ns Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents
- Extremely High RBSOA Capability
- Case 221D is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221D-02
UL RECOGNIZED

OUTLINE DIMENSIONS



STYLE 2
PIN 1 BASE
2 COLLECTOR
3 EMITTER

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982
2 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.78	15.97	0.621	0.629
B	10.01	10.21	0.394	0.402
C	4.60	4.80	0.181	0.189
D	0.67	0.86	0.026	0.034
F	3.08	3.27	0.121	0.129
G	2.54 BSC		0.100 BSC	
H	3.13	3.27	0.123	0.129
J	0.46	0.64	0.018	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.52	0.045	0.060
N	5.08 BSC		0.200 BSC	
Q	3.21	3.40	0.126	0.134
R	2.72	2.81	0.107	0.111
S	2.44	2.64	0.096	0.104
U	6.58	6.78	0.259	0.267

CASE 221D-02
ISOLATED TO-220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-Emitter Voltage		$V_{CEO(sus)}$	450	Vdc
Collector-Emitter Voltage		V_{CEV}	850	Vdc
Emitter-Base Voltage		V_{EB}	6.0	Vdc
RMS Isolation Voltage (for 1 sec, T_A = 25°C, Relative Humidity ≤ 30%)(2)	Test No. 1 Per Fig. 18	V_{ISOL_1}	4500	V
	Test No. 2 Per Fig. 19	V_{ISOL_2}	3500	
	Test No. 3 Per Fig. 20	V_{ISOL_3}	1500	
Collector Current — Continuous — Peak(1)		I_C I_{CM}	5.0 10	Adc
Base Current — Continuous — Peak(1)		I_B I_{BM}	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C* @ T_C = 100°C* Derate above T_C = 25°C		P_D	40 16 0.32	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.125	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.
* Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink, thermal grease applied at a mounting torque of 6 to 8 in-lbs.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS(1)					
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.2 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1.0 2.5 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.4 Adc) (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	200	pF
Collector to Heatsink Capacitance	$C_{c\text{-}hs}$	—	15	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	t_d	—	30	100	ns
Rise Time	t_r	—	100	300	
Storage Time	t_s	—	1000	3000	
Fall Time	t_f	—	60	300	
Storage Time	t_s	—	400	—	
Fall Time	t_f	—	130	—	
Inductive Load (Table 2)					
Storage Time	t_{sv}	—	500	1600	ns
Fall Time	t_{fi}	—	100	200	
Crossover Time	t_c	—	120	250	
Storage Time	t_{sv}	—	600	—	
Fall Time	t_{fi}	—	120	—	
Crossover Time	t_c	—	160	—	

Resistive Load (Table 1): (I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%); (I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω) for t_d, t_r, t_s, t_f; ($V_{BE(off)}$ = 5.0 Vdc) for t_s, t_f.

Inductive Load (Table 2): (I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc); (T_J = 100°C) for t_{sv}, t_{fi}, t_c; (T_J = 150°C) for t_{sv}, t_{fi}, t_c.

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2.0%.

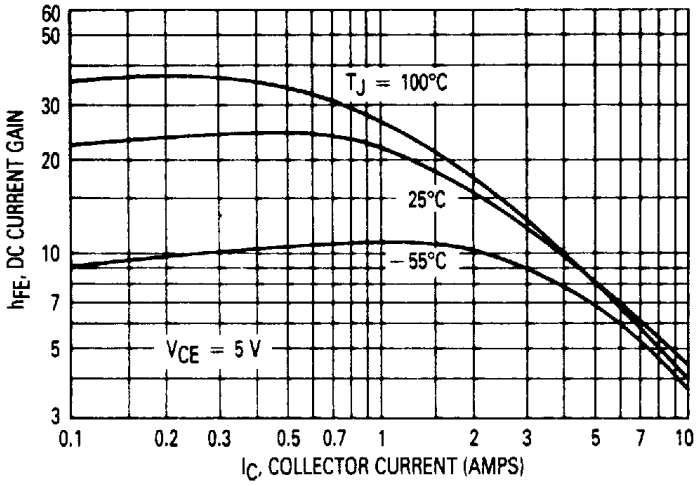


Figure 1. DC Current Gain

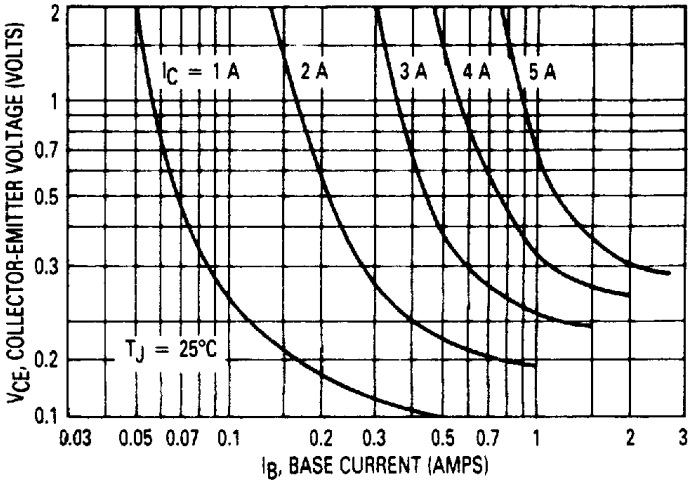


Figure 2. Collector Saturation Region

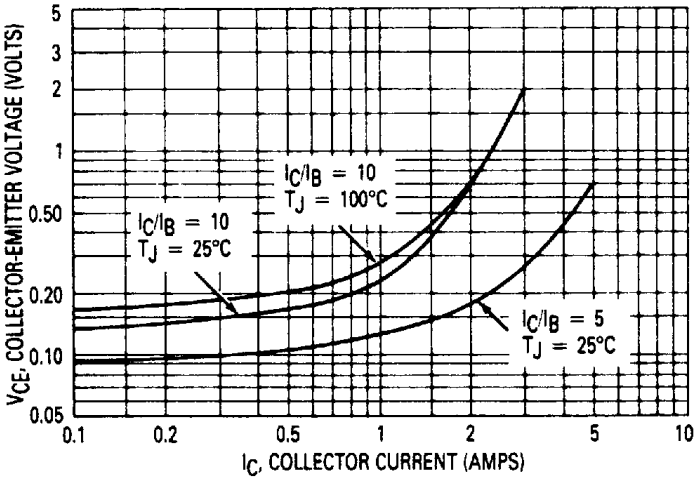


Figure 3. Collector-Emitter Saturation Voltage

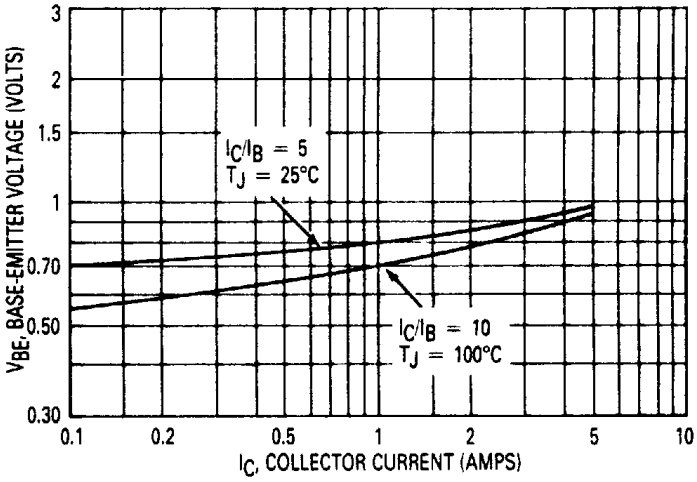


Figure 4. Base-Emitter Voltage

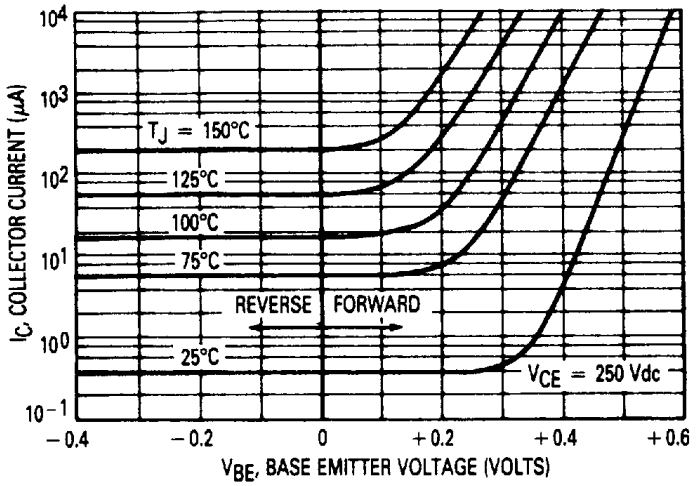


Figure 5. Collector Cutoff Region

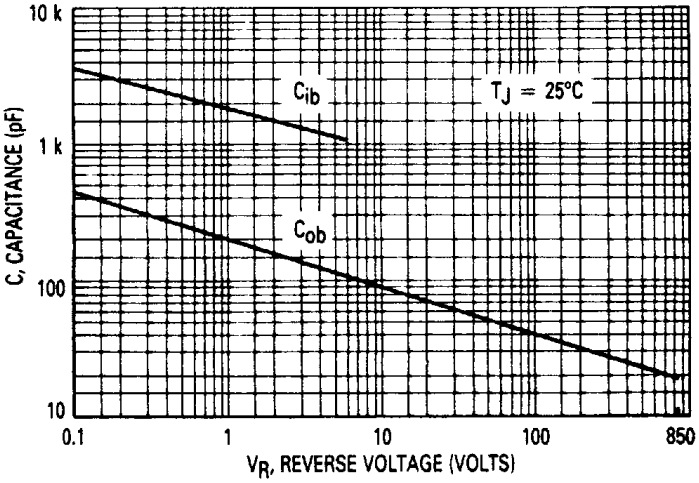


Figure 6. Capacitance

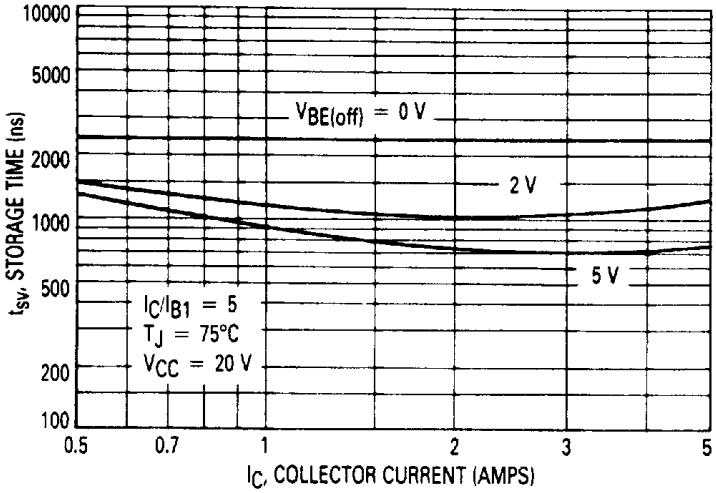


Figure 7. Storage Time

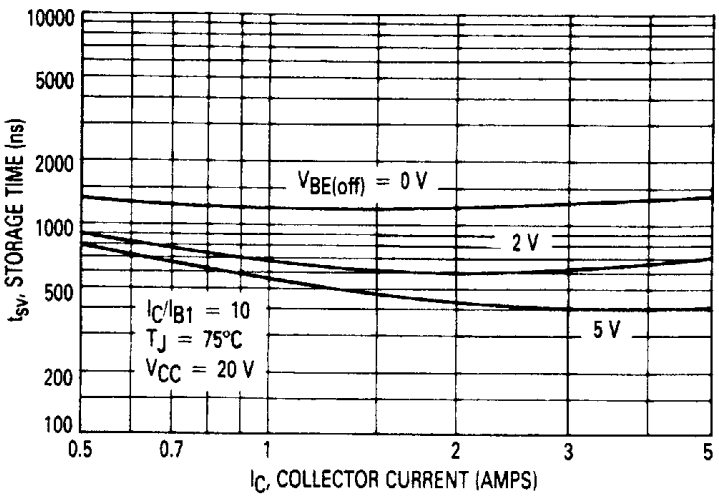


Figure 8. Storage Time

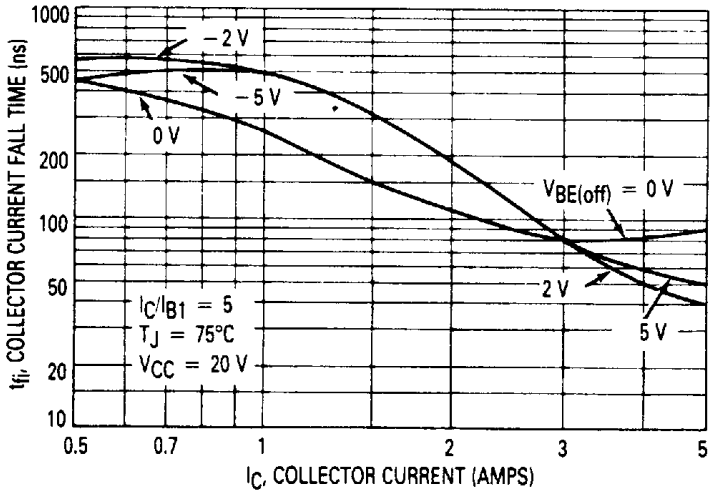


Figure 9. Collector Current Fall Time

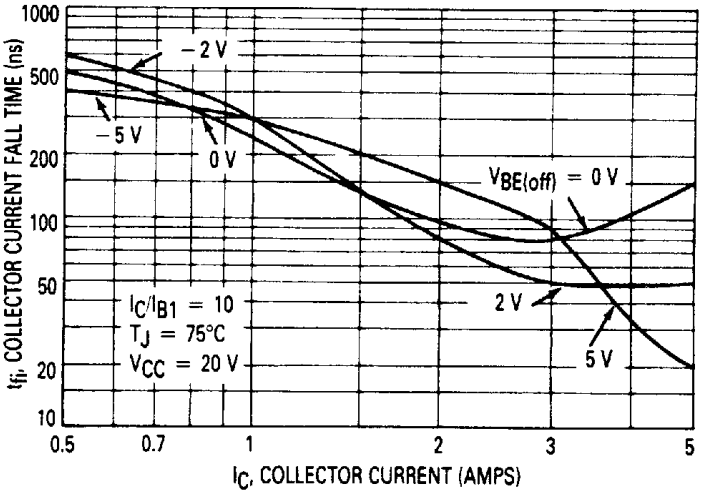


Figure 10. Collector Current Fall Time

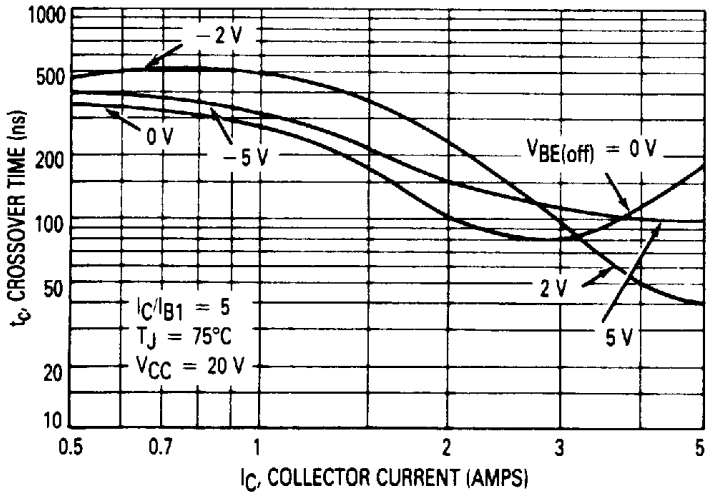


Figure 11. Crossover Time

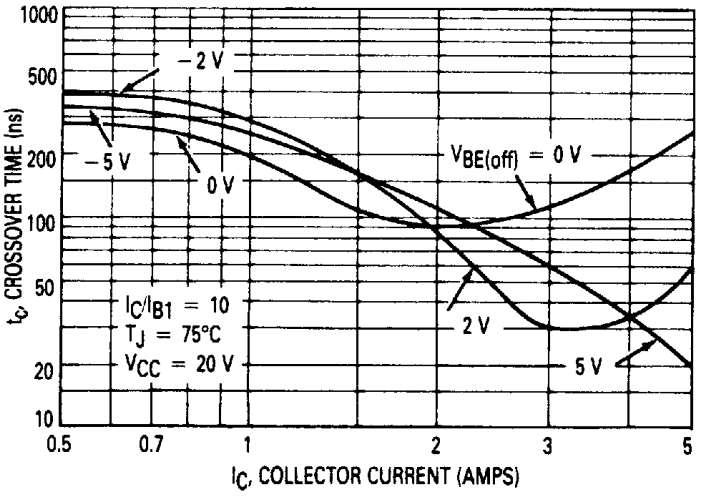


Figure 12. Crossover Time

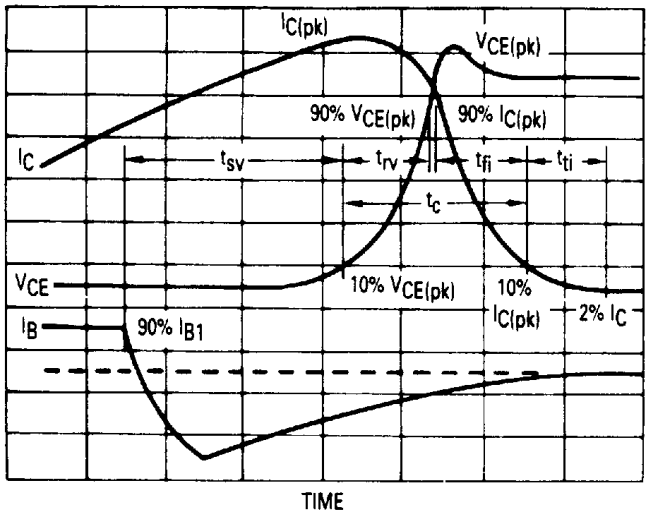


Figure 13. Inductive Switching Measurements

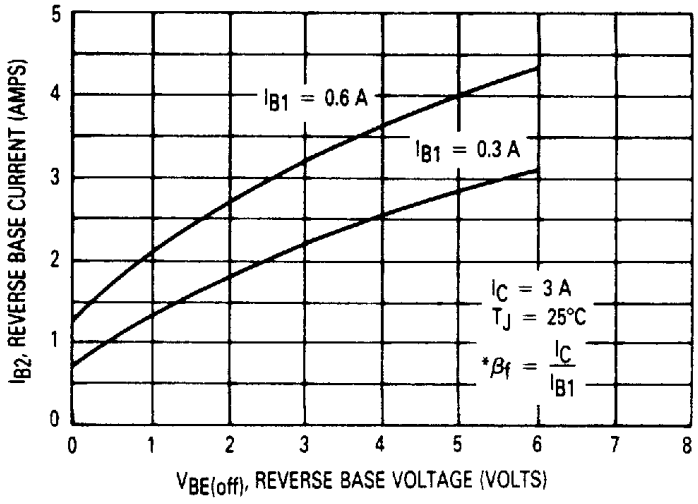
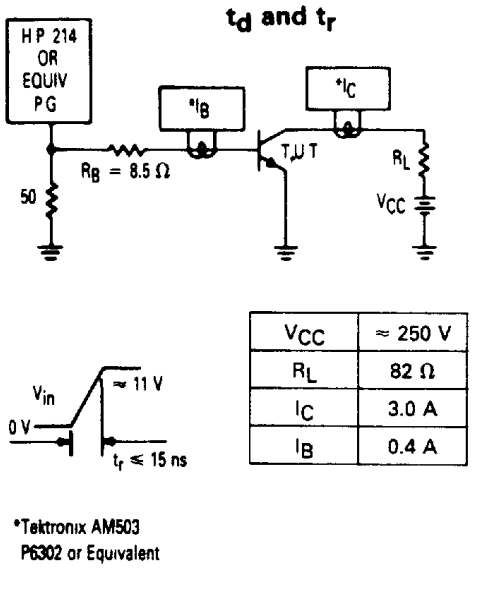


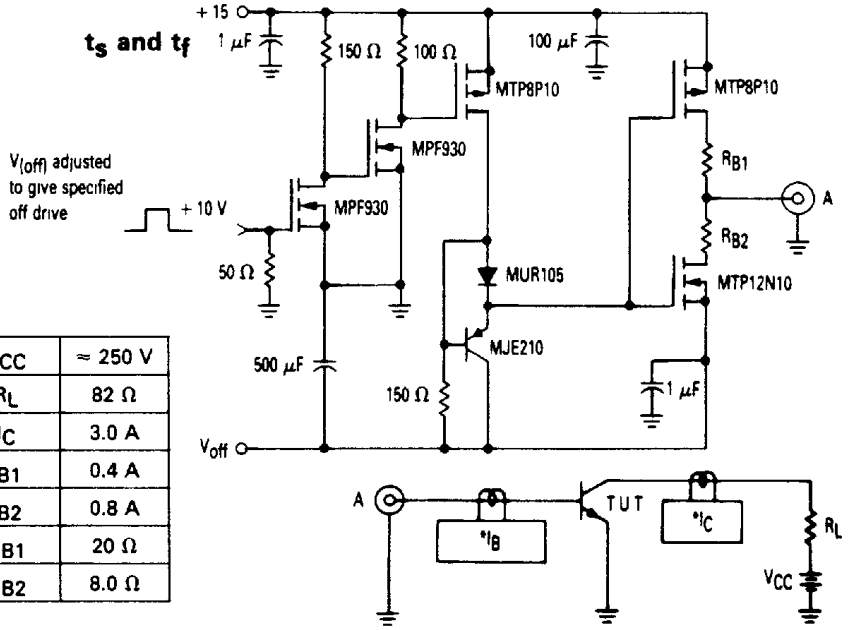
Figure 14. Peak Reverse Base Current

Table 1. Resistive Load Switching



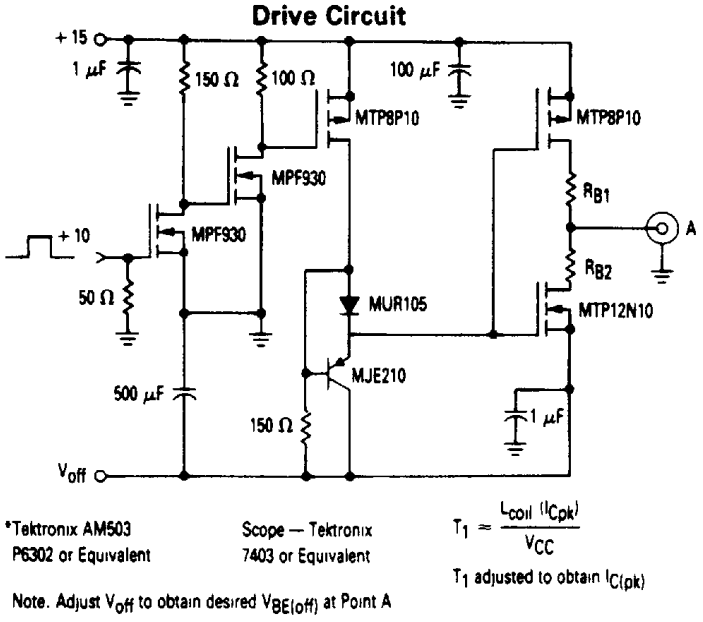
V_{CC}	≈ 250 V
R_L	82 Ω
I_C	3.0 A
I_B	0.4 A

*Tektronix AM503
P6302 or Equivalent



V_{CC}	≈ 250 V
R_L	82 Ω
I_C	3.0 A
I_{B1}	0.4 A
I_{B2}	0.8 A
R_{B1}	20 Ω
R_{B2}	8.0 Ω

Table 2. Inductive Load Switching



*Tektronix AM503
P6302 or Equivalent

Scope — Tektronix
7403 or Equivalent

$T_1 \approx \frac{L_{coil}(I_{C(pk)})}{V_{CC}}$

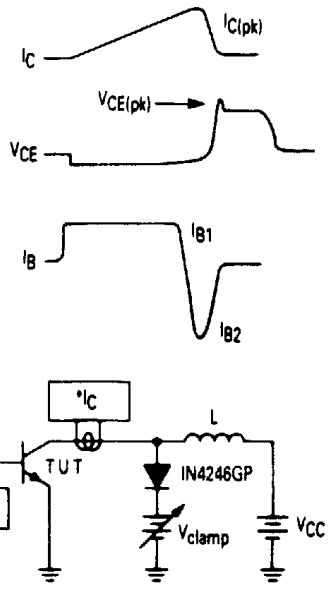
T_1 adjusted to obtain $I_{C(pk)}$

Note. Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A

$V_{(BR)CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts

Inductive Switching
L = 750 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 750 μH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}



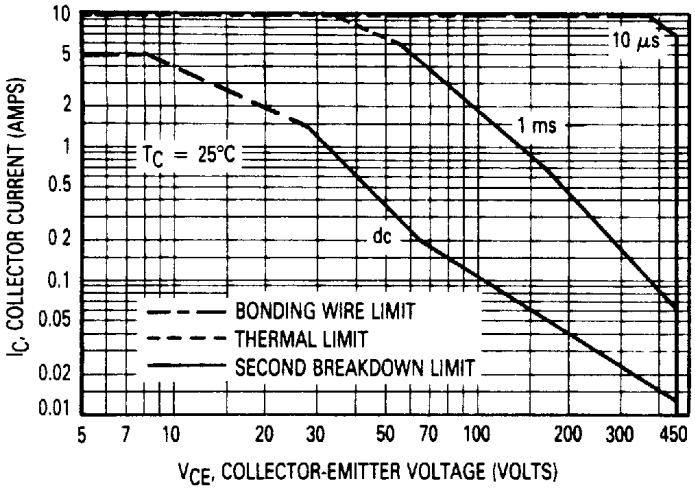


Figure 15. Maximum Rated Forward Bias Safe Operating Area

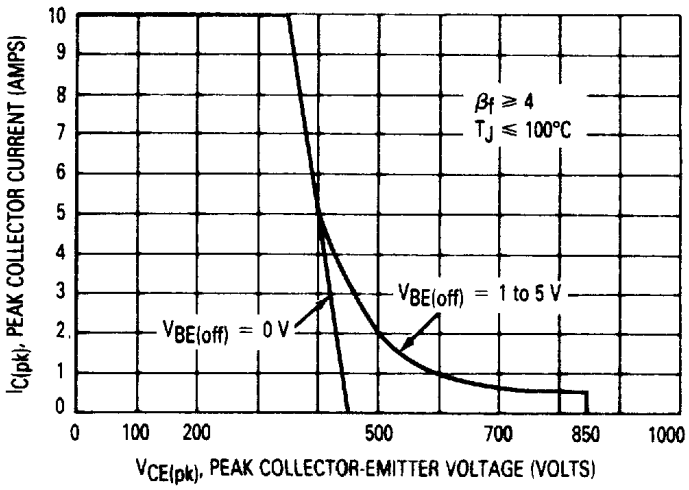


Figure 16. Maximum Rated Reverse Bias Safe Operating Area

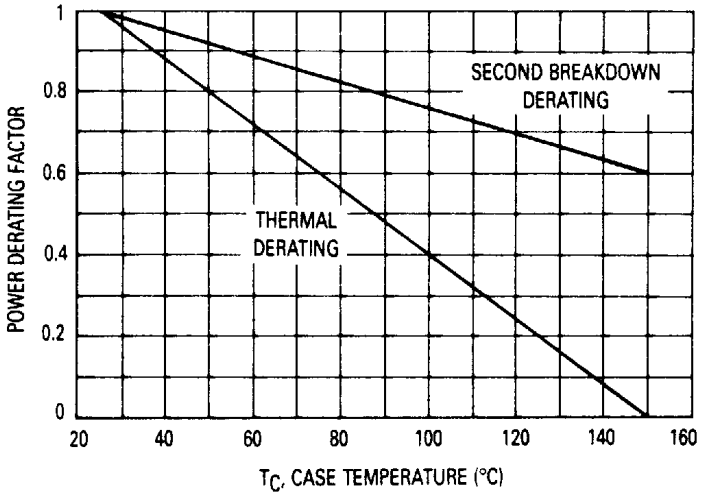


Figure 17. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{(BR)CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{(BR)CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

4. OPERATION ABOVE $V_{(BR)CEO(sus)}$ —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momemtarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1.0 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

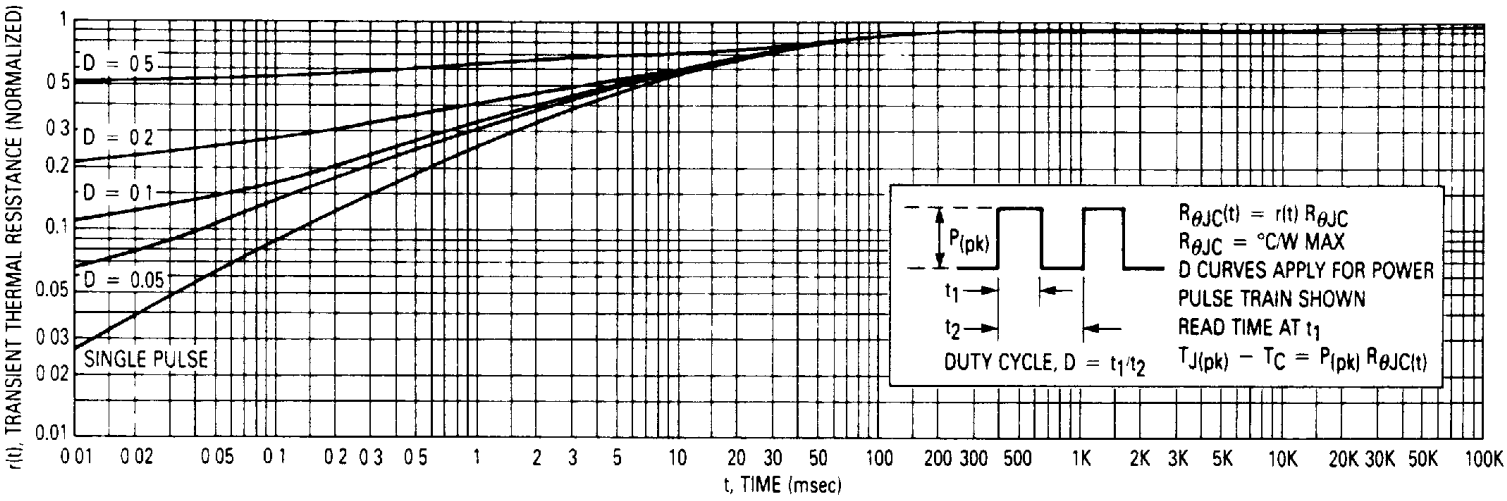


Figure 18. Typical Thermal Response for MJF16002

TEST CONDITIONS FOR ISOLATION TESTS*

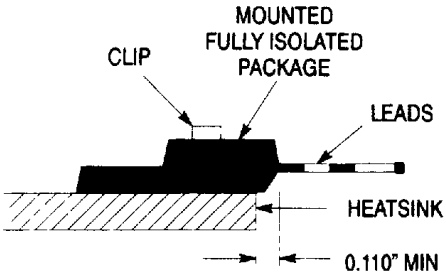


Figure 19. Clip Mounting Position for Isolation Test Number 1

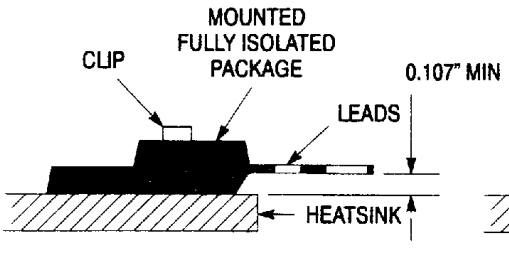


Figure 20. Clip Mounting Position for Isolation Test Number 2

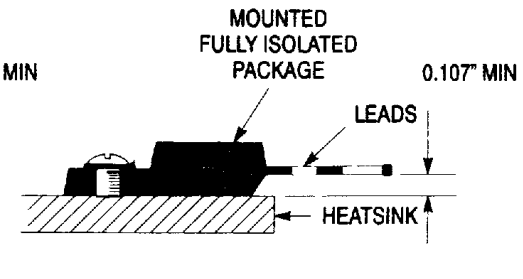


Figure 21. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

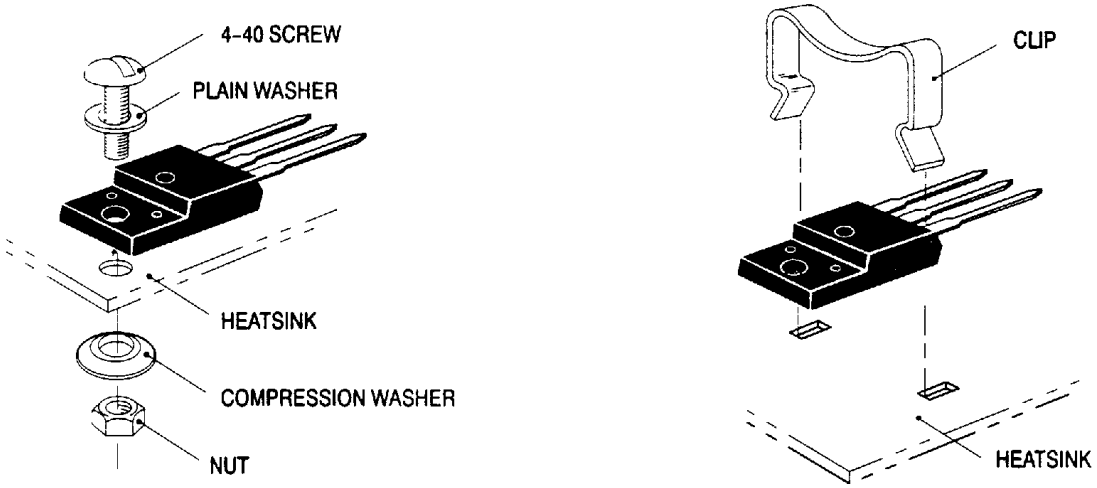


Figure 22. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

**For more information about mounting power semiconductors see Application Note AN1040.

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