

MOTOROLA

SEMICONDUCTOR

TECHNICAL DATA

Designers Data Sheet

SWITCHMODE SERIES NPN SILICON POWER TRANSISTORS

The MJ13330 and MJ13331 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Time

75 ns Inductive Fall Time—25°C (Typ)

150 ns Inductive Crossover Time—25°C (Typ)

900 ns Inductive Storage Time—25°C (Typ)

Operating Temperature Range –65 to +200°C

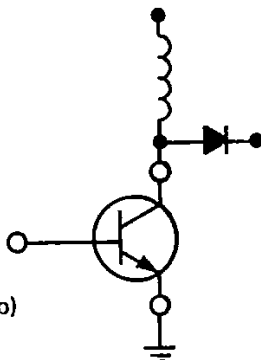
100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

Switching Times with Inductive Loads

Saturation Voltages

Leakage Currents



DataSheet4U.com

MAXIMUM RATINGS

Rating	Symbol	MJ13330	MJ13331	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	400	450	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous	I_C	20		Adc
— Peak (1)	I_{CM}	30		
Base Current — Continuous	I_B	10		Adc
— Peak (1)	I_{BM}	20		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175		Watts
@ $T_C = 100^\circ\text{C}$		100		
Derate above 25°C		1		W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

MJ13330

MJ13331

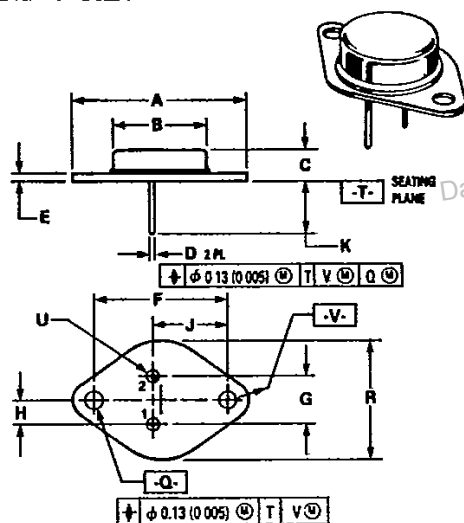
20 AMPERE

NPN SILICON
POWER TRANSISTORS

200 and 250 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION, INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 1.
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 1-06
TO-204AA
(TO-3)

Similar device types with higher V_{CEO} ratings are: MJ13332 (350 V) thru MJ13335 (500 V).

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	200 250	— —	— —	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^{\circ}\text{C}$)	I_{CEV}	— —	— —	0.25 5	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^{\circ}\text{C}$)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current ($V_{EB} = 6\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	0.5	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased	$RBSOA$	See Figure 13			

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 10\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	15 8.0	— —	75 40	—
Collector-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.5\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.8\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{CE(sat)}$	— — —	— — —	1.5 3.5 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 10\text{ Adc}$, $I_B = 1.5\text{ Adc}$) ($I_C = 10\text{ Adc}$, $I_B = 1.8\text{ Adc}$, $T_C = 100^{\circ}\text{C}$)	$V_{BE(sat)}$	— —	— —	1.8 1.8	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 300\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1\text{ MHz}$)	f_T	5	—	40	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 100\text{ kHz}$)	C_{ob}	100	—	400	pF

SWITCHING CHARACTERISTICS

SWITCHING CHARACTERISTICS

DataSheet4U.com

Delay Time

Rise Time

Storage Time

Fall Time

$(V_{CC} = 175\text{ Vdc}, I_C = 10\text{ A}, I_{B1} = 1.5\text{ Adc}, V_{BE(off)} = 5\text{ Vdc}, t_p = 50\text{ }\mu\text{s}, \text{Duty Cycle} \leq 2\%)$

t_d

t_r

t_s

t_f

—

—

—

—

0.08

0.55

0.70

0.11

0.20

1.0

3.5

0.7

μs

μs

μs

μs

Inductive Load, Clamped (Table 1)

Storage Time

Crossover Time

Storage Time

Crossover Time

Fall Time

$(I_C = 10\text{ A(pk)}, V_{clamp} = 200\text{ Vdc}, I_{B1} = 1.8\text{ Adc}, V_{BE(off)} = 5\text{ Vdc}, T_C = 100^{\circ}\text{C})$

$(I_C = 10\text{ A(pk)}, V_{clamp} = 200\text{ Vdc}, I_{B1} = 1.5\text{ Adc}, V_{BE(off)} = 5\text{ Vdc}, T_C = 25^{\circ}\text{C})$

t_{sv}

t_c

t_{sv}

t_c

t_{fi}

—

—

—

—

—

1.35

0.45

0.90

0.15

0.075

4.5

1.8

—

—

—

μs

μs

μs

μs

μs

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

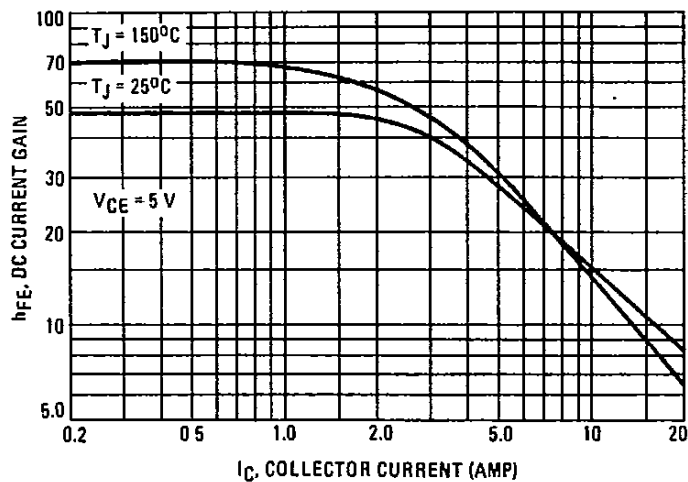


FIGURE 2 – COLLECTOR SATURATION REGION

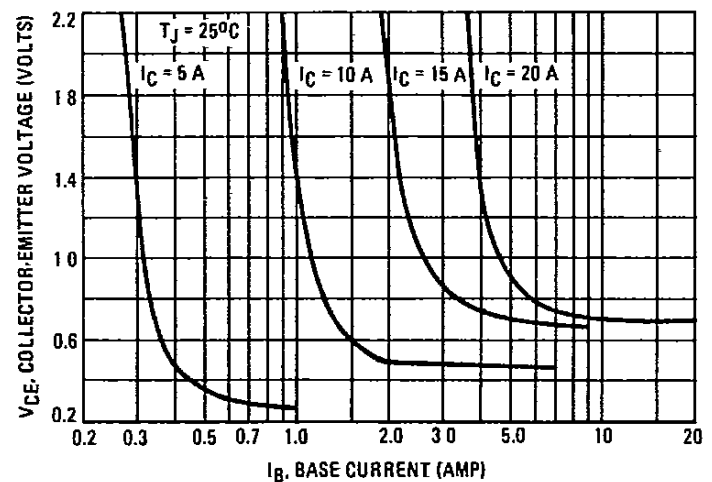


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

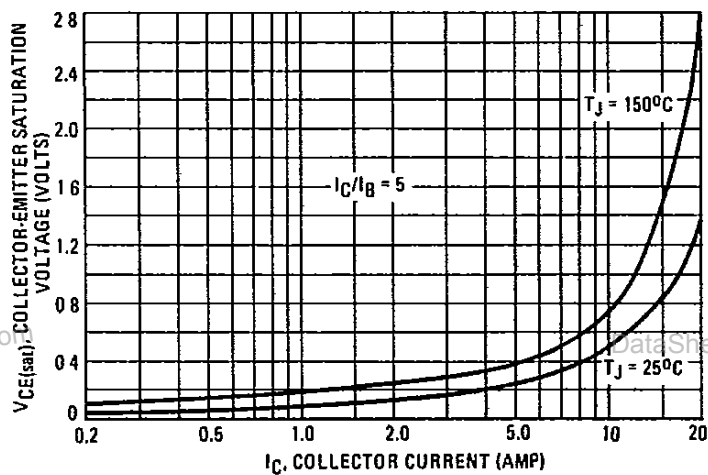


FIGURE 4 – BASE-EMITTER VOLTAGE

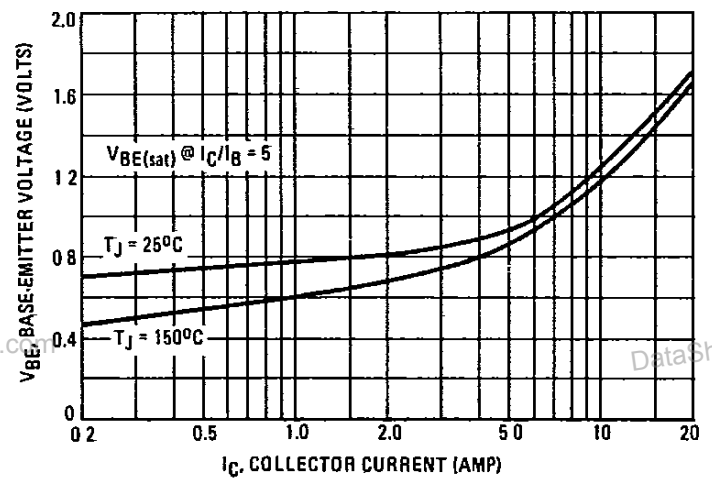


FIGURE 5 – COLLECTOR CUTOFF REGION

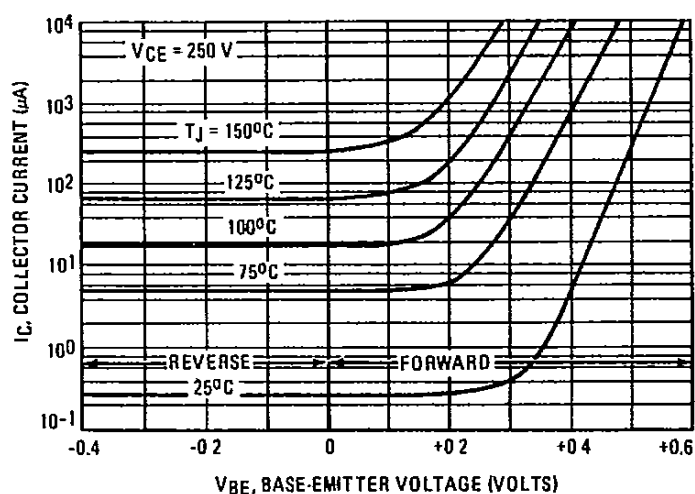
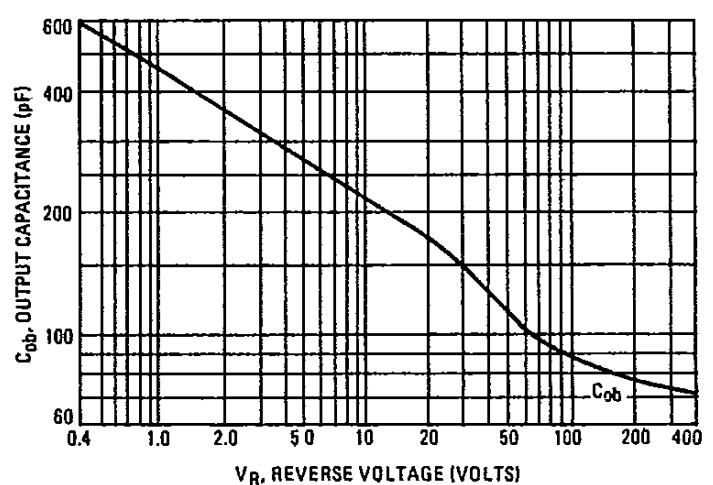
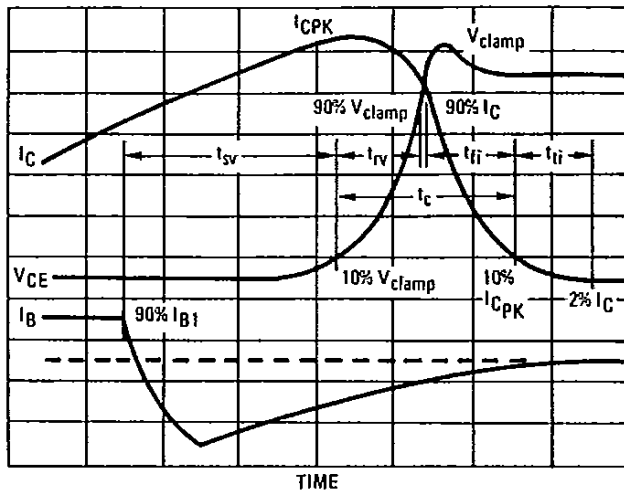
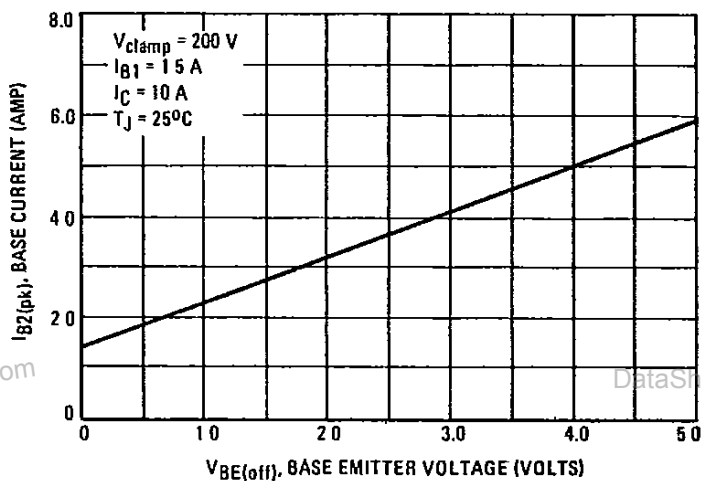


FIGURE 6 – OUTPUT CAPACITANCE



SWITCHING TIMES NOTE

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

FIGURE 8 – REVERSE BASE CURRENT
versus BASE EMITTER VOLTAGE

RESISTIVE SWITCHING

FIGURE 9 – TURN-ON TIME

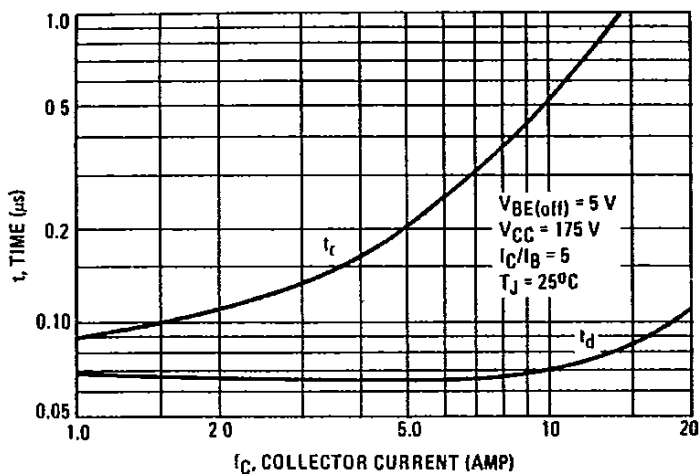
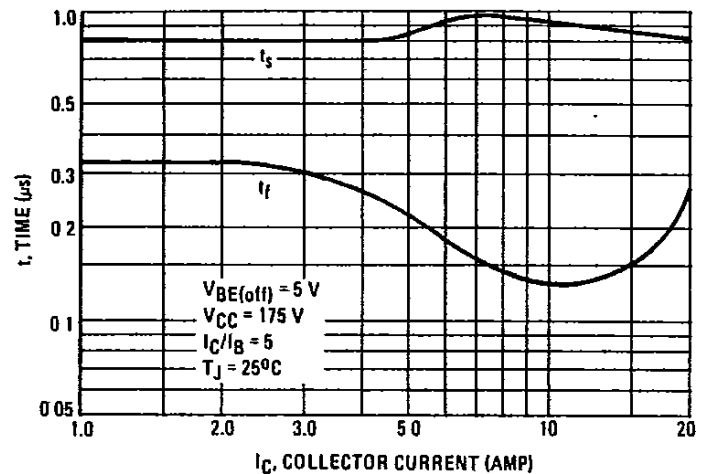


FIGURE 10 – TURN-OFF TIME



In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

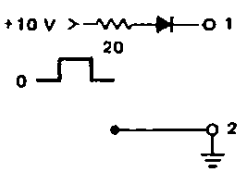
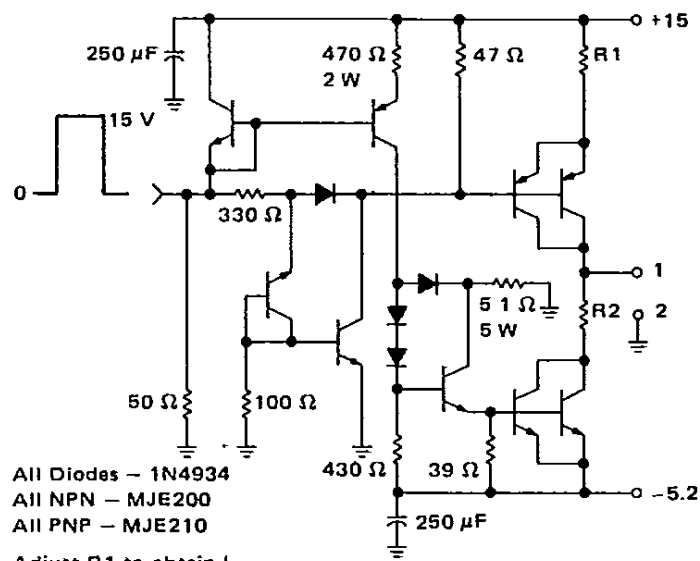
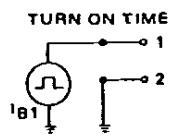
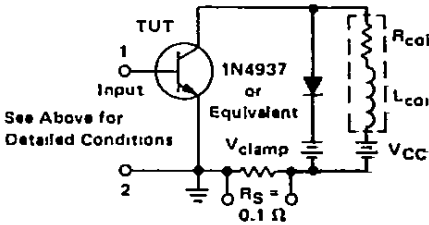
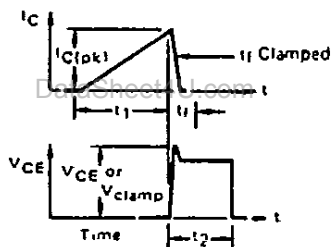
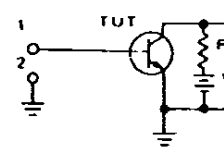
	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain $I_C = 100 \text{ mA}$	 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, $R2 = 0$ For $V_{CEO(sus)}$, $R2 = \infty$	 TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	$L_{coil} = 80 \text{ mH}$ $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = 200 \text{ V}$	$V_{CC} = 175 \text{ V}$ $R_L = 17.5$ Pulse Width $\sim 25 \mu\text{s}$
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above for Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 11 – THERMAL RESPONSE

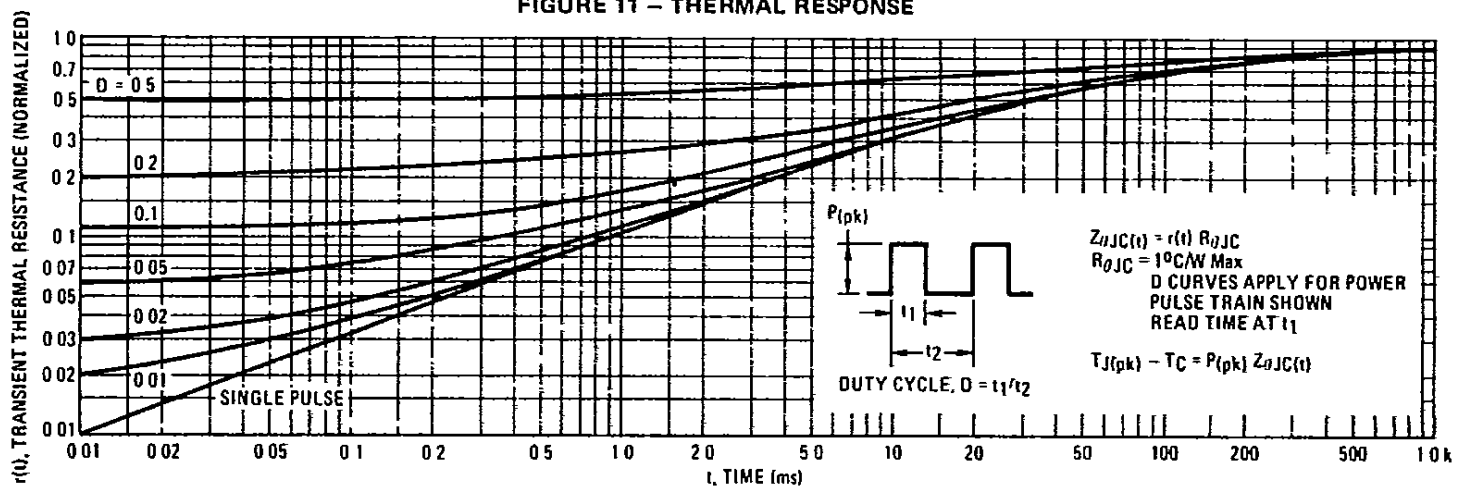


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

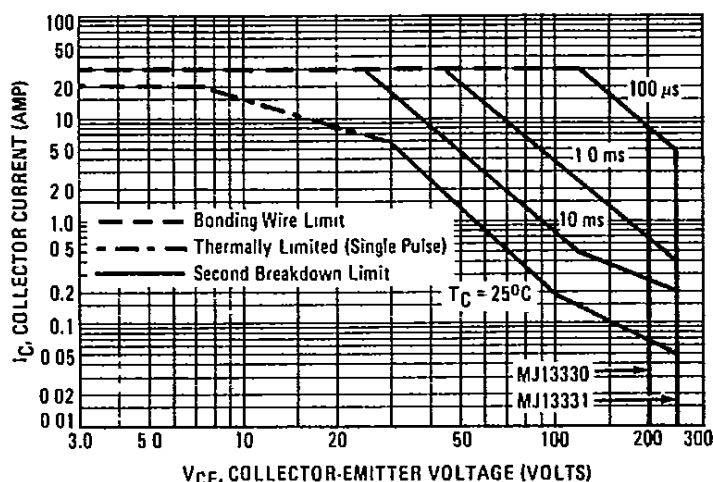
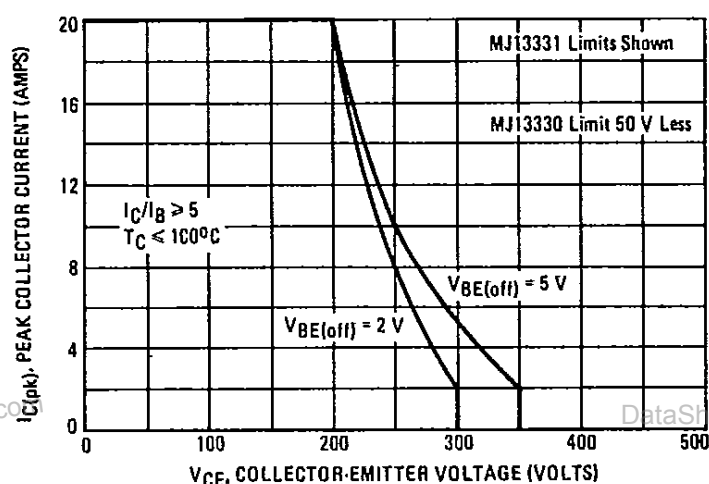


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^\circ\text{C}$; $T_J(pk)$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_J(pk)$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING

