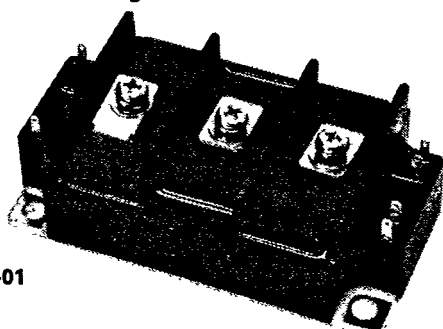


NPN Silicon Power Transistor Module

Energy Management Series

These power transistors are designed for industrial service under practical operating environments found in switching high power inductive loads.

- Energy Efficient Package
- Isolated Mounting Plate (2500 Volts RMS)
- Low Saturation Voltage
- Low Thermal Resistance
- Internal Flyback and Speed-Up Diodes
- High DC Current Gain
- Low Current Terminals Separated from High Current Terminals

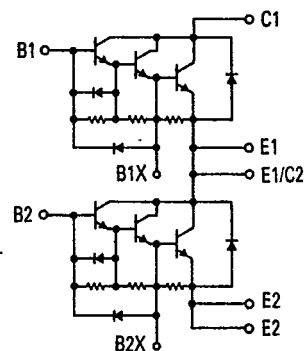


CASE 814-01

MJ100BX120

**DUAL
TRI-STAGE
POWER TRANSISTORS
100 AMPERES
1200 VOLTS
700 WATTS**

EQUIVALENT CIRCUIT



MAXIMUM RATINGS (Per Device and $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage ($I_B = 0$)	$V_{CEO(sus)}$	900	Vdc
Collector-Emitter Voltage ($V_{BE} = -2\text{ V}$)	V_{CEX}	1200	Vdc
Collector-Base Voltage	V_{CB}	1200	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Isolation Voltage (ac for 1 minute)	V_{ISOL}	2500	Vac
Collector Current — Continuous — Peak Nonrepetitive for 1 ms	I_C	100 200	A
Base Current — Continuous	I_B	10	A
Total Device Dissipation Derate above $T_C = 25^\circ\text{C}$	P_D	700 5.59	Watts W/°C
Operating Junction and Storage Temperature Range	T_J T_{stg}	-40 to +150 -40 to +125	°C

MECHANICAL RATINGS

Mounting Torque	—	26	in.-lb.
Terminal Torque	—	26	in.-lb.
Per Unit Weight	—	470	grams

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Maximum Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.179 0.65	°C/W
Transistor C-E Diode			



ELECTRICAL CHARACTERISTICS (Per Device and $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 1 \text{ A}$, $L = 40 \text{ mH}$)	$V_{CEO(sus)}$	900	—	—	Vdc
Collector Cutoff Current ($V_{CB} = \text{Rated } V_{CB}$, $I_E = 0$)	I_{CBO}	—	—	2	mA
Emitter Cutoff Current ($V_{EB} = 7 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	400	mA

SAFE OPERATING AREA

Second Breakdown Collector Current with Base Forward-Biased	FBSOA	See Figure 11
Clamped Inductive SOA with Base Reverse-Biased	RBSOA	See Figure 12

ON CHARACTERISTICS (1)

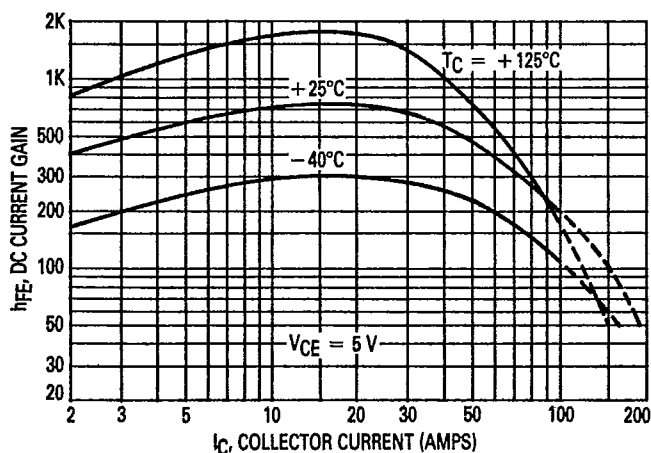
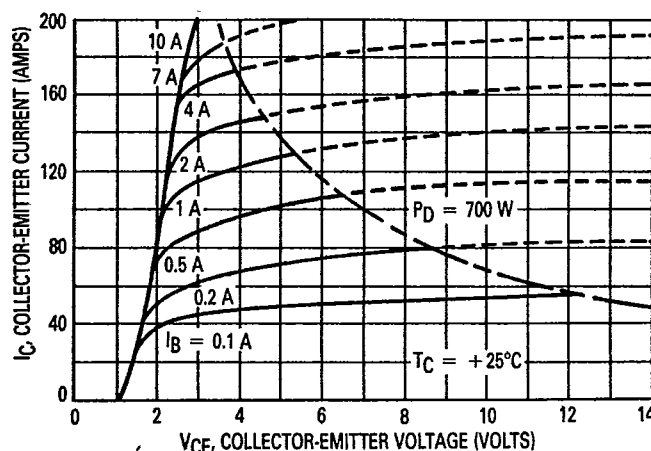
DC Current Gain ($I_C = 100 \text{ A}$, $V_{CE} = 5 \text{ Vdc}$)	h_{FE}	100	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ A}$, $I_B = 2 \text{ A}$)	$V_{CE(sat)}$	—	2	2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 100 \text{ A}$, $I_B = 2 \text{ A}$)	$V_{BE(sat)}$	—	2.8	3.2	Vdc

SWITCHING CHARACTERISTICS

Resistive Load					
Turn-On Time	$V_{CC} = 600 \text{ Vdc}$, $I_C = 100 \text{ A}$, $I_{B1} = 2 \text{ A}$, $t_p = 50 \mu\text{s}$, $I_{B2} = 6 \text{ A}$ Duty Cycle $\leq 0.5\%$	t_{on}	—	0.9	2
Storage Time		t_s	—	10	14
Fall Time		t_f	—	2	3

C-E DIODE CHARACTERISTICS

Forward Voltage (1) ($I_F = 100 \text{ A}$)	V_F	—	—	1.8	Vdc
Reverse Recovery Time ($I_F = 100 \text{ A}$, $V_{EB} = 3 \text{ V}$, $di/dt = 100 \text{ A}/\mu\text{s}$)	t_{rr}	—	—	1.5	μs

(1) Pulse Test: Pulse width of $300 \mu\text{s}$, duty cycle $\leq 2\%$.**Figure 1. Typical DC Current Gain (Per Device)****Figure 2. Typical Collector Saturation Region (Per Device)**

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COLLECTOR SATURATION REGION
(PER DEVICE)

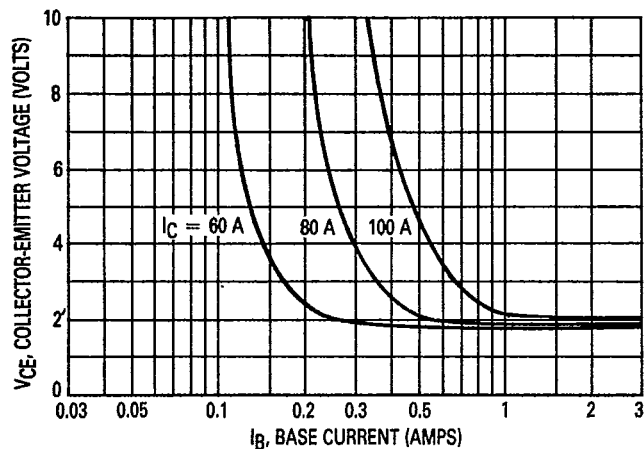


Figure 3. $T_C = +25^\circ\text{C}$

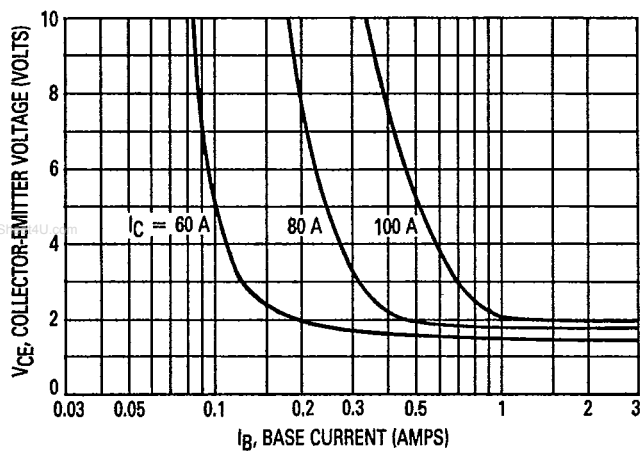


Figure 4. $T_C = +125^\circ\text{C}$

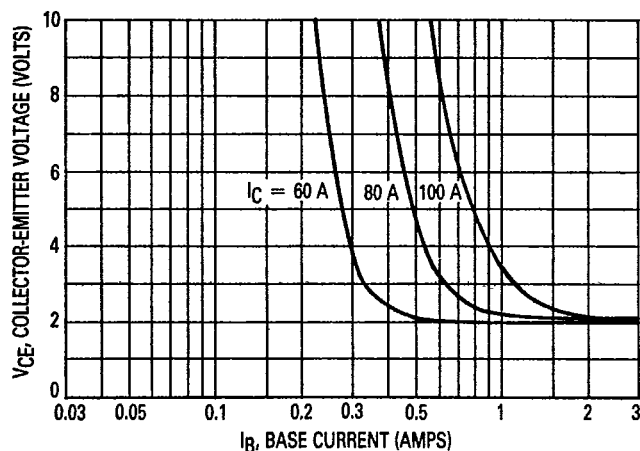


Figure 5. $T_C = -40^\circ\text{C}$

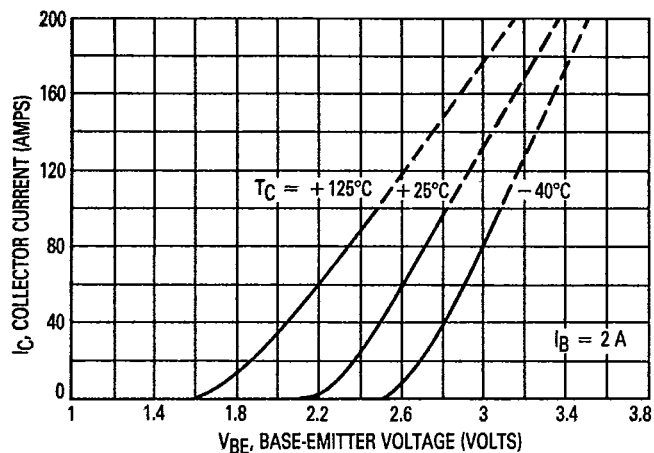


Figure 6. Typical Base-Emitter Saturation Region
(Per Device)

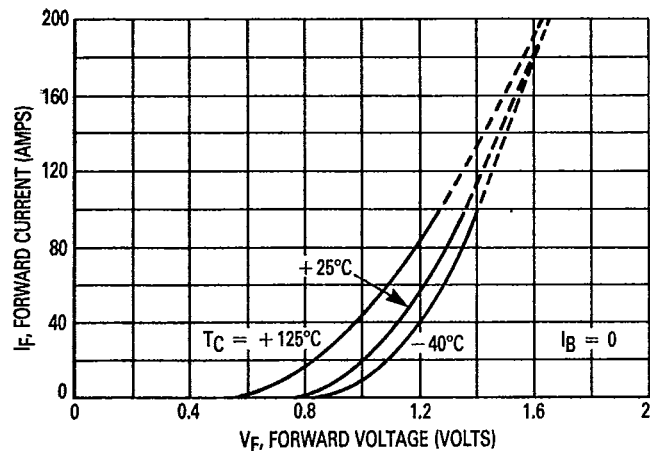


Figure 7. Typical Collector-Emitter Diode Forward
Characteristics (Per Device)

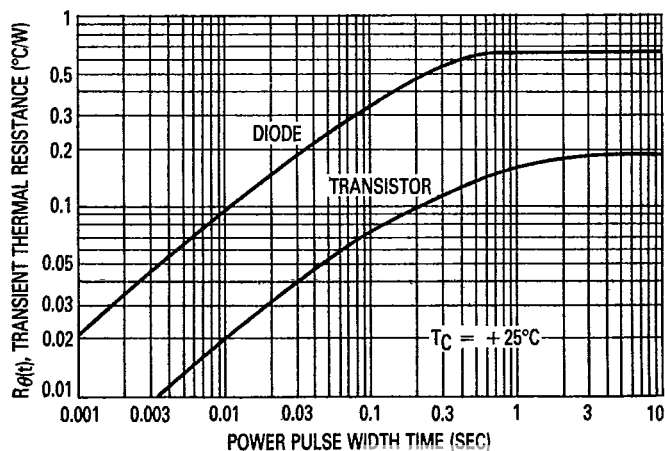


Figure 8. Transient Thermal Response

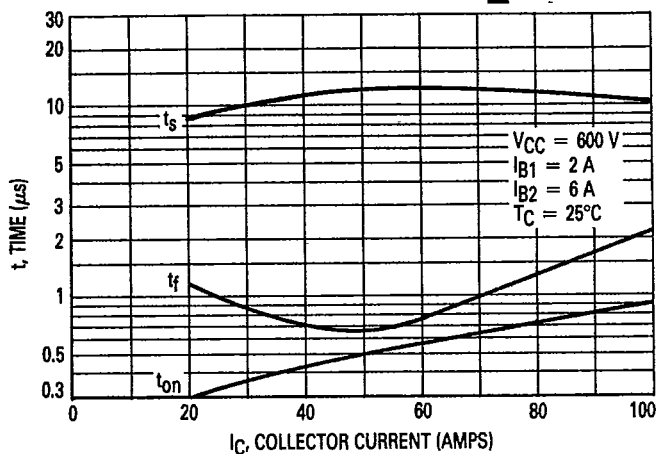


Figure 9. Typical Resistive Switching Times (Per Device)

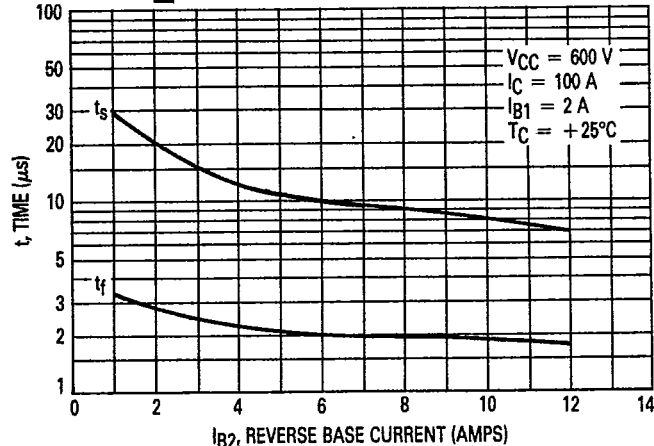
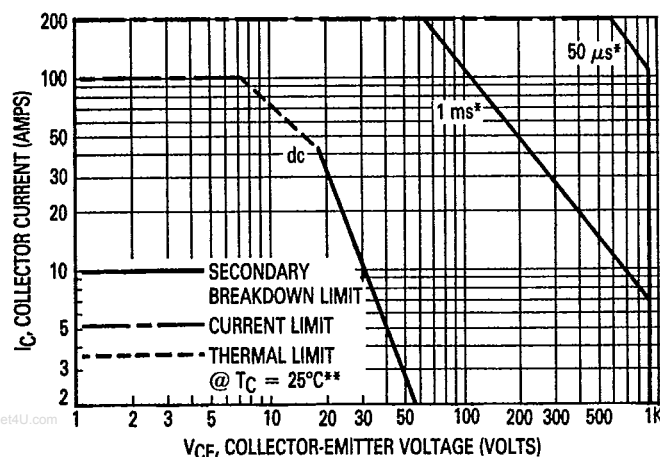


Figure 10. Typical Resistive Turn-Off Times versus Reverse Bias (Per Device)



*Single Non-Repetitive Pulse

**Curves Must Be Derated Linearly with Increased Temperature

Figure 11. Forward Bias Safe Operating Area (Per Device)

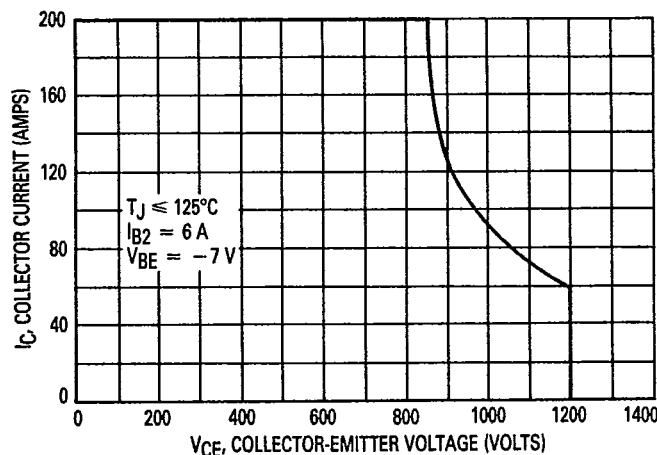
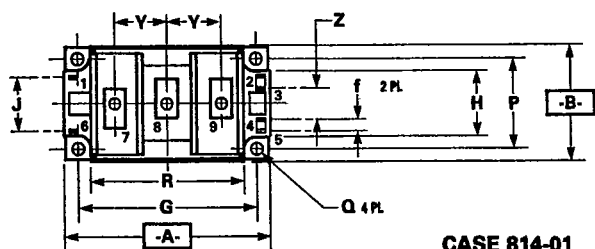


Figure 12. Reverse Bias Safe Operating Area (Per Device)

OUTLINE DIMENSIONS



CASE 814-01

NOTES:

1. POSITIONAL TOLERANCE FOR Q DIMENSION (4 PL): $\pm 0.36 (0.014) \text{ (M)} \times \text{A} \text{ (B)} \text{ (C)}$
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. TERMINALS 1, 2, 3, 4, 5 AND 6 ARE FAST-ON-TAB # 110.
5. TERMINALS 7, 8, AND 9 USE M5 SCREWS.

STYLE 1:

1. BASE 2X
2. BASE 2
3. EMITTER 2
4. EMITTER 1
5. BASE 1
6. BASE 1X
7. COLLECTOR 2/EMITTER 1
8. EMITTER 2
9. COLLECTOR 1

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	107.2	108.8	4.221	4.283
B	61.2	62.8	2.410	2.472
C	22.0	25.0	0.867	0.984
D	2.5	3.5	0.099	0.137
E	24.5	25.5	0.965	1.003
F	21.0	22.0	0.827	0.866
G	93.0 BSC		3.661 BSC	
H	34.2	35.8	1.347	1.409
J	28.5	29.5	1.122	1.161
K	7.4	8.6	0.292	0.338
L	—	38.0	—	1.496
N	53.2	54.8	2.095	2.157
P	48.0 BSC		1.890 BSC	
Q	6.2	6.8	0.244	0.267
R	79.2	80.8	3.119	3.181
T	105.2	106.8	4.142	4.204
V	59.2	60.8	2.331	2.393
W	3.5	4.5	0.138	0.177
Y	27.5	28.5	1.083	1.122
Z	16.5	17.5	0.650	0.688
e	48.5	49.5	1.910	1.948
f	5.5	6.5	0.217	0.255

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