



## MIC4930

### Hyper Speed Control™ 3A Buck Regulator

#### General Description

The MIC4930 is a high-efficiency, 3A synchronous buck regulator with ultra-fast transient response perfectly suited for supplying processor core and I/O voltages from a 5V or 3.3V bus. The MIC4930 provides a switching frequency up to 3.3MHz while achieving peak efficiencies up to 95%. An additional benefit of high-frequency operation is very low output ripple voltage throughout the entire load range with the use of a small output capacitor. The MIC4930 is designed for use with a very small inductor, down to 1μH, and an output ceramic capacitor as small as 10μF without the need for external ripple injection. A wide range of output capacitor types and values can also be accommodated.

The MIC4930 supports safe start-up into a pre-biased output.

The MIC4930 is available in a 10-pin 3mm × 4mm DFN package with an operating junction temperature range from -40°C to +125°C. The MIC4930 is pin-to-pin compatible with the 5A-rated MIC4950YFL.

Datasheets and support documentation are available on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

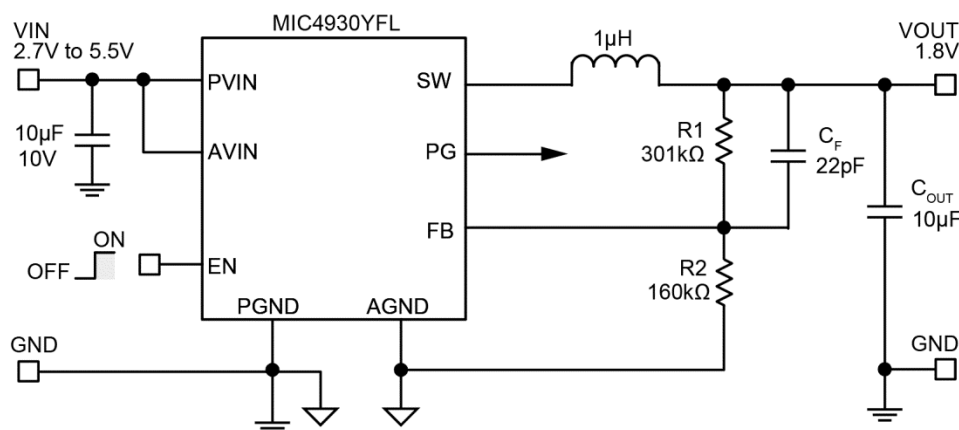
#### Features

- Input voltage: 2.7V to 5.5V
- 3A output current
- Up to 95% efficiency
- Up to 3.3MHz operation
- Safe start-up into a pre-biased output
- Power Good output
- Ultra-fast transient response
- Low output voltage ripple
- Low  $R_{DS(ON)}$  integrated MOSFET switches
- 0.01μA shutdown current
- Thermal shutdown and current limit protection
- Output voltage as low as 0.7V
- 3mm × 4mm DFN-10L
- -40°C to +125°C junction temperature range

#### Applications

- DTVs
- Set-top boxes
- Printers
- DVD players
- Distributed power supplies

#### Typical Application



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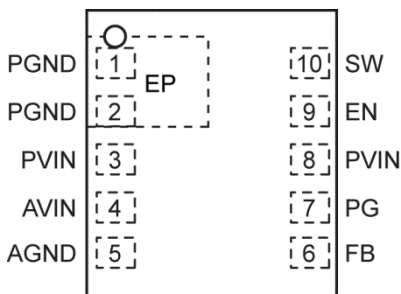
## Ordering Information

Part Number <sup>(1)</sup>	Top Mark	Temperature Range	Package <sup>(2)</sup>	Lead Finish
MIC4930YFL	MIC4930	$-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$	10-pin 3mm x 4mm DFN	Pb-Free

**Note:**

- Other options are available. Contact Micrel for details.
- DFN is a GREEN, RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen free.

## Pin Configuration



3mm x 4mm DFN (FL)  
(Top View)

## Pin Description

Pin Number	Pin Name	Pin Function
1, 2, EP	PGND	Power ground.
3, 8	PVIN	Power input voltage: Connect a 10 $\mu$ F ceramic capacitor between PVIN and PGND for input decoupling. Pins 3 and 8 are internally connected inside the package.
4	AVIN	Analog input voltage: Connect a 1 $\mu$ F ceramic capacitor between AVIN and AGND to decouple the noise for the internal reference and error comparator.
5	AGND	Analog ground input: Connect to a quiet ground plane for best operation. Do not route power switching currents on the AGND net. Connect AGND and PGND nets together at a single point.
6	FB	Feedback (input): Connect an external divider between VOUT and AGND to program the output voltage.
7	PG	Power Good (output): Open-drain output. A pull-up resistor from this pin to a voltage source is required to detect an output power-is-good condition.
9	EN	Enable (input): Logic high enables operation of the regulator. Logic low will shut down the device. Do not leave floating.
10	SW	Switch (output): Internal power MOSFET output switches.

**Absolute Maximum Ratings<sup>(3)</sup>**

PVIN, AVIN Supply Voltage ( $V_{IN}$ )	–0.3V to +6V
SW Output Switch Voltage ( $V_{SW}$ )	–0.3V to $V_{IN}$
EN, PG ( $V_{EN}$ , $V_{PG}$ )	–0.3V to $V_{IN}$
FB Feedback Input Voltage ( $V_{FB}$ )	–0.3V to $V_{IN}$
Storage Temperature ( $T_s$ )	–65°C to +150°C
ESD Rating <sup>(5)</sup>	2kV, HBM

**Operating Ratings<sup>(4)</sup>**

Supply Voltage ( $V_{IN}$ )	+2.7V to +5.5V
Enable Input Voltage ( $V_{EN}$ )	0V to $V_{IN}$
Junction Temperature Range ( $T_J$ )	–40°C ≤ $T_J$ ≤ +125°C
Thermal Resistance	
DFN-10 ( $\theta_{JA}$ )	35°C/W

**Electrical Characteristics<sup>(6)</sup>**

$V_{IN} = V_{EN} = 3.3V$ ;  $L = 1.0\mu H$ ;  $T_A = 25^\circ C$ ;  $C_{IN} = 10\mu H$ ,  $C_{OUT} = 10\mu H$  unless otherwise specified.

**Bold** values indicate –40°C ≤  $T_J$  ≤ +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IN}$	Supply voltage range		<b>2.7</b>		<b>5.5</b>	V
$V_{UVLO}$	Undervoltage lockout threshold	(turn-on)	<b>2.41</b>	2.5	<b>2.61</b>	V
$V_{UVLOH}$	Undervoltage lockout hysteresis			400		mV
$I_Q$	Quiescent current	$I_{OUT} = 0mA$ , $FB > 1.2 \times V_{FB(Nominal)}$		0.8	<b>2</b>	mA
$I_{SD}$	Shutdown current	$V_{EN} = 0V$		0.01	<b>2</b>	μA
$V_{FB}$	Feedback voltage		<b>0.609</b>	0.625	<b>0.640</b>	V
$I_{LIMIT}$	Current limit	$FB = 0.9V \times V_{FB(Nominal)}$	3.5	5.75	8	A
LINEREG	Output voltage line regulation	$V_{IN} = 2.7V$ to $3.5V$ , $V_{OUTNOM} = 1.8V$ , $I_{LOAD} = 20mA$		1		%V
		$V_{IN} = 4.5V$ to $5.5V$ if $V_{OUTNOM} \geq 2.5V$ , $I_{LOAD} = 20mA$				
LOADREG	Output voltage load regulation	$20mA < I_{LOAD} < 500mA$ , $V_{IN} = 3.6V$ if $V_{OUTNOM} < 2.5V$		0.3		%
		$20mA < I_{LOAD} < 500mA$ , $V_{IN} = 5.0V$ if $V_{OUTNOM} \geq 2.5V$				
		$20mA < I_{LOAD} < 3A$ , $V_{IN} = 3.6V$ if $V_{OUTNOM} < 2.5V$		1		%
		$20mA < I_{LOAD} < 3mA$ , $V_{IN} = 5.0V$ if $V_{OUTNOM} \geq 2.5V$				
$R_{DS(on)-P}$	PWM switch ON resistance	$I_{SW} = 1A$ P-Channel MOSFET		30		mΩ
$R_{DS(on)-N}$		$I_{SW} = 1A$ N-Channel MOSFET		25		

## Electrical Characteristics Continued<sup>(6)</sup>

$V_{IN} = V_{EN} = 3.3V$ ;  $L = 1.0\mu H$ ;  $T_A = 25^\circ C$ ,  $C_{IN} = 10\mu H$ ,  $C_{OUT} = 10\mu H$  unless otherwise specified.

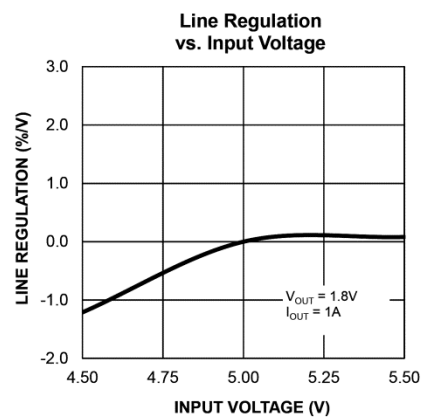
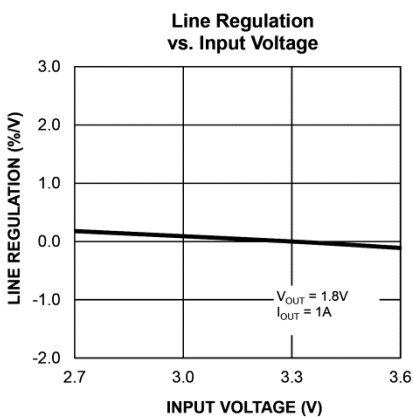
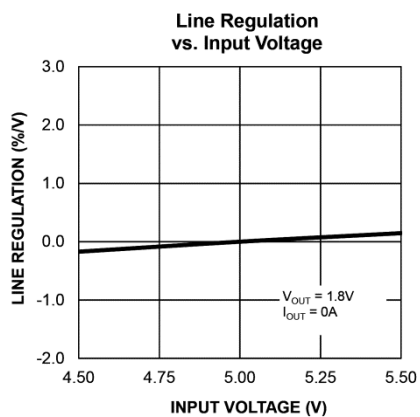
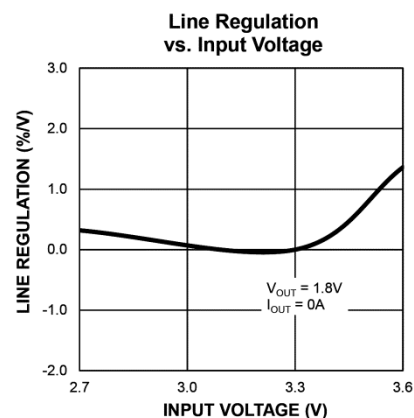
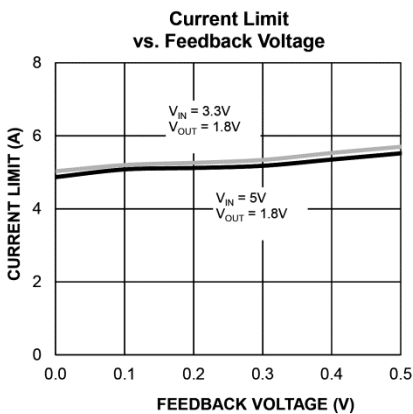
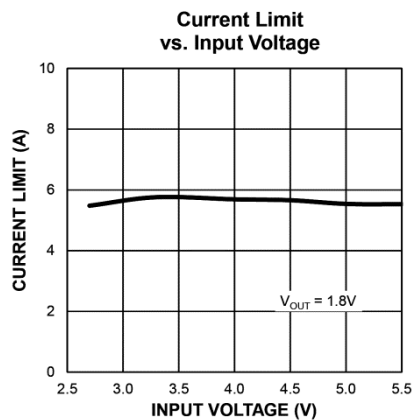
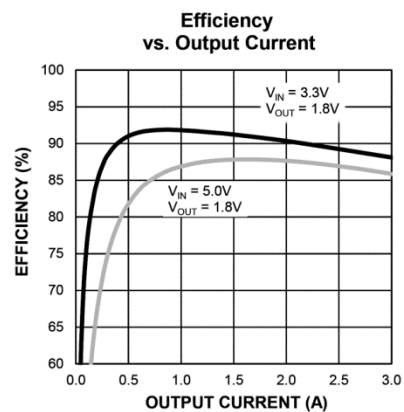
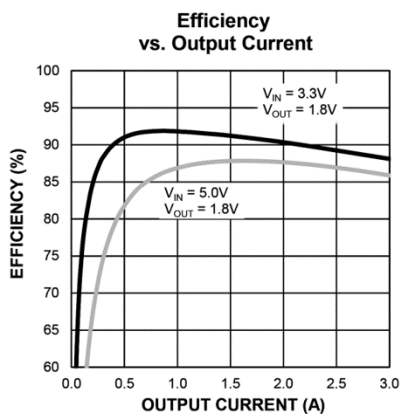
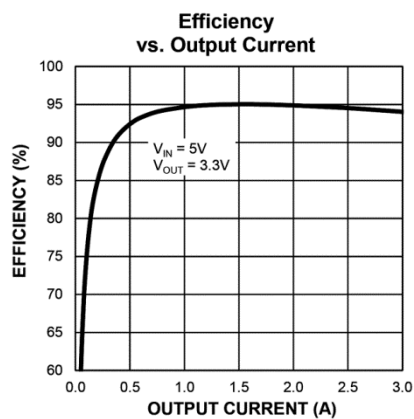
**Bold** values indicate  $-40^\circ C \leq T_J \leq +85^\circ C$ , unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{ON}$	Maximum turn-on time	$V_{IN} = 4.5V$ , $V_{FB} = 0.5V$		665		ns
		$V_{IN} = 3.0V$ , $V_{FB} = 0.5V$		1000		
		$V_{IN} = 2.7V$ , $V_{FB} = 0.5V$		1120		
$t_{OFF}$	Minimum turn-off time	$V_{IN} = 3.0V$ , $V_{FB} = 0.5V$		176		ns
$t_{SOFT-ON}$	Soft-start time	$V_{OUT} = 90\%$ of $V_{OUTNOM}$		500		$\mu s$
$V_{EN}$	Enable threshold	Turn-on	<b>0.5</b>	0.8	<b>1.2</b>	V
$I_{EN}$	Enable input current			0.1	<b>1</b>	$\mu A$
$V_{OUTPG}$	Power Good threshold	Rising	<b>82</b>	88	<b>94</b>	%
$V_{OUTPGH}$	Power Good hysteresis			7		%
$T_{SD}$	Overtemperature shutdown			150		$^\circ C$
$T_{SDH}$	Overtemperature shutdown hysteresis			20		$^\circ C$

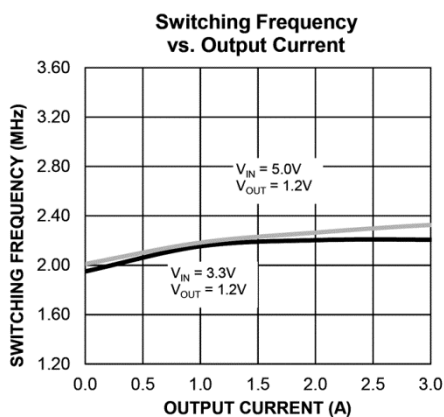
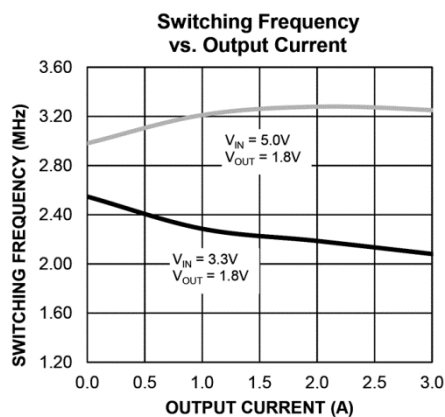
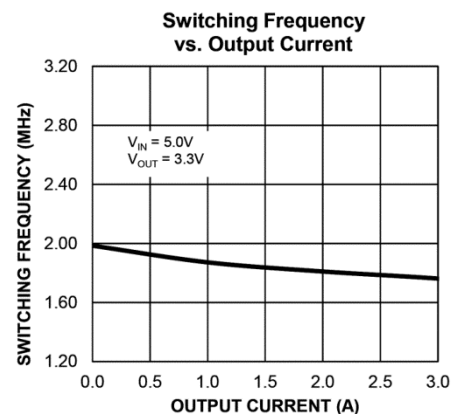
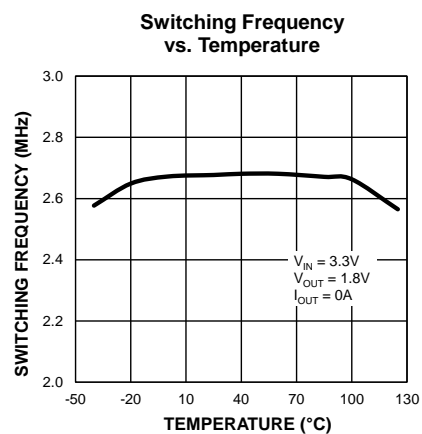
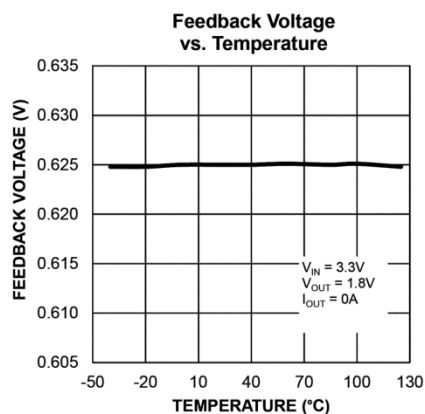
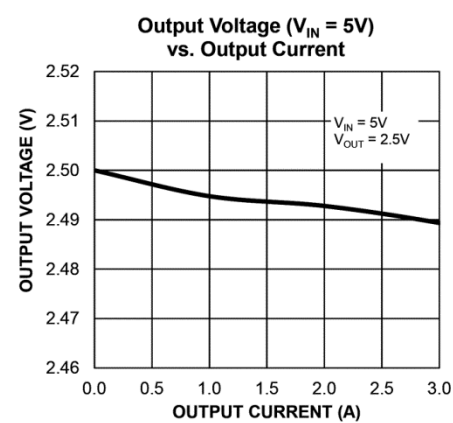
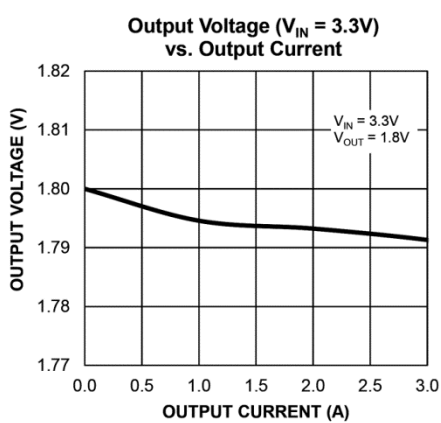
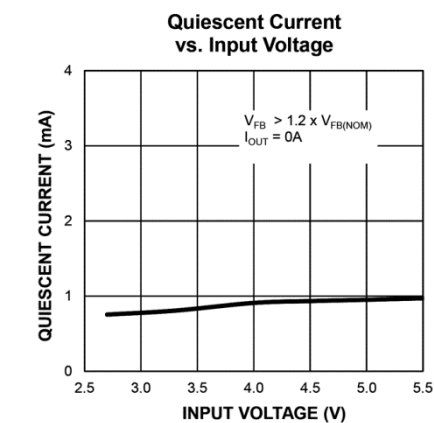
### Notes:

- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- Devices are ESD sensitive. Handling precautions are recommended. Human body model,  $1.5k\Omega$  in series with  $100pF$ .
- Specification for packaged product only.

## Typical Characteristics

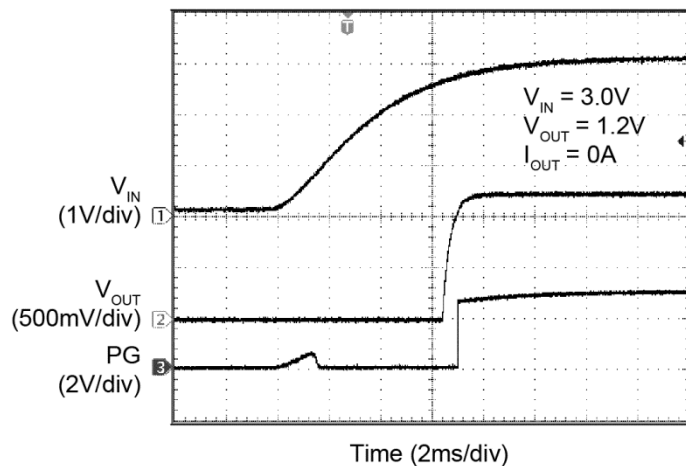


## Typical Characteristics (Continued)

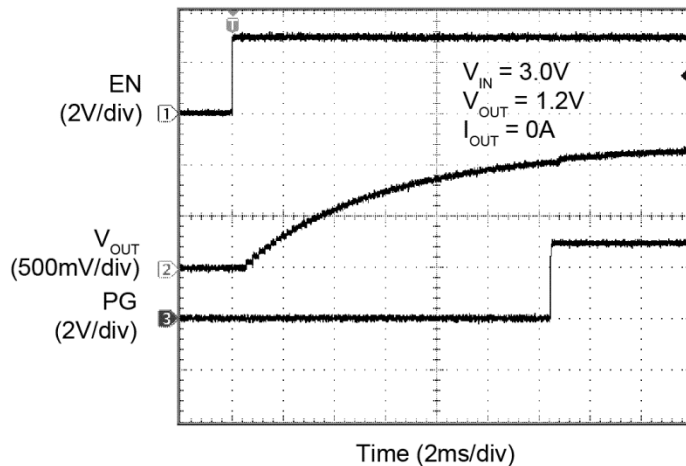


## Functional Characteristics

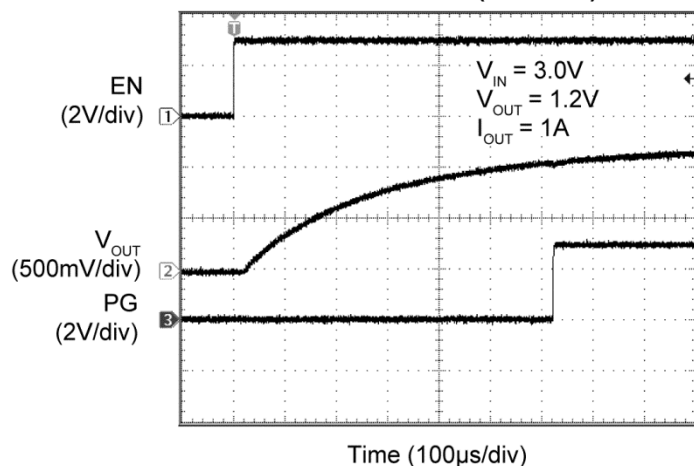
### VIN Soft Turn-On



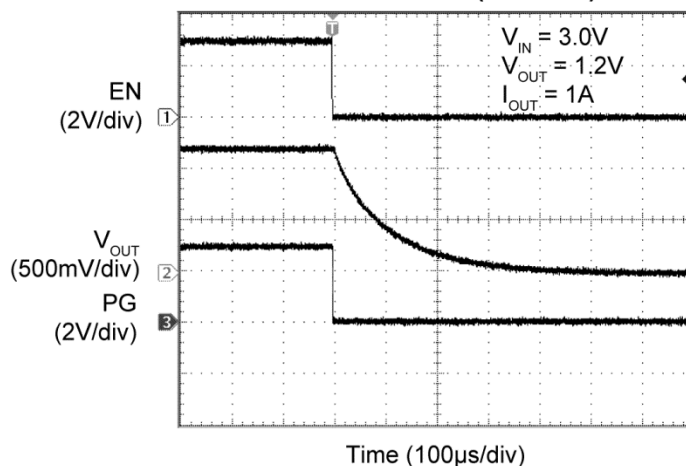
### Enable Turn-On (No Load)



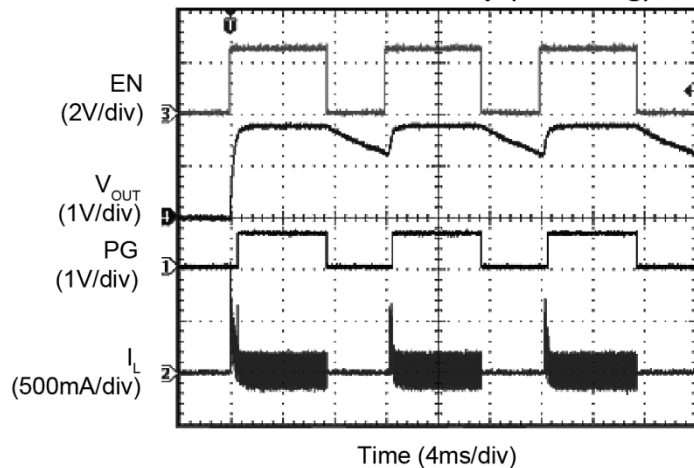
### Enable Turn-On (1A Load)



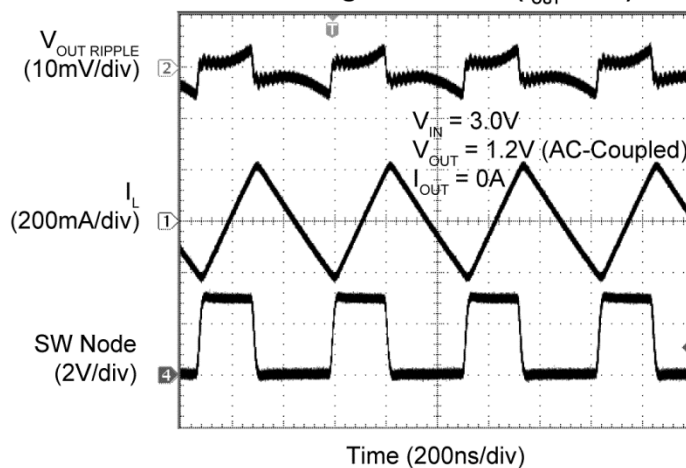
### Enable Turn-Off (1A Load)



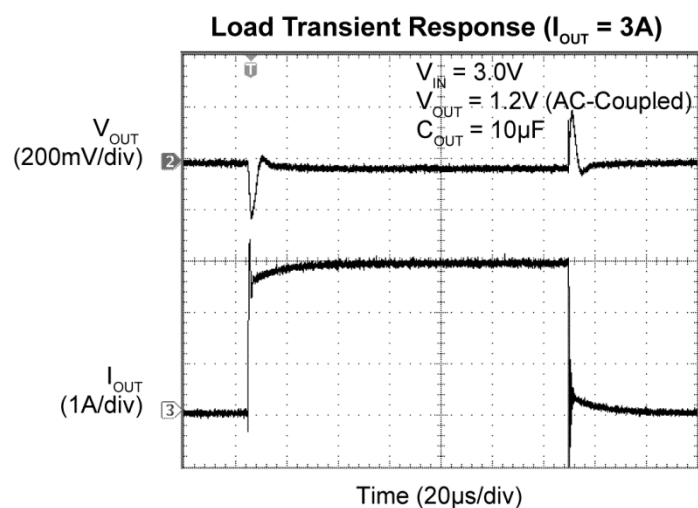
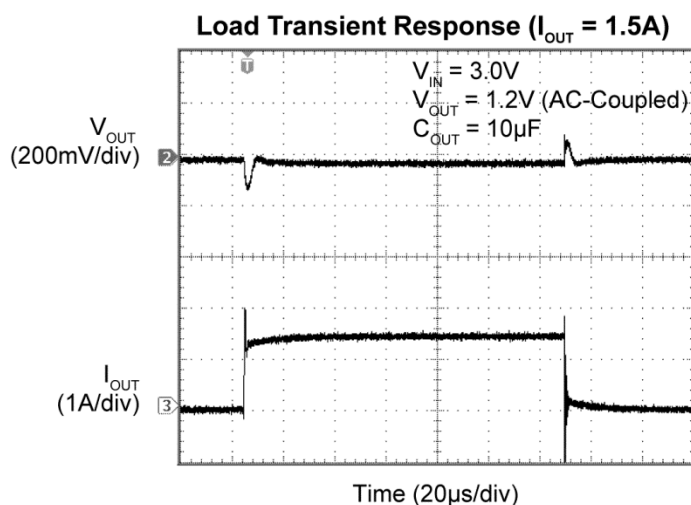
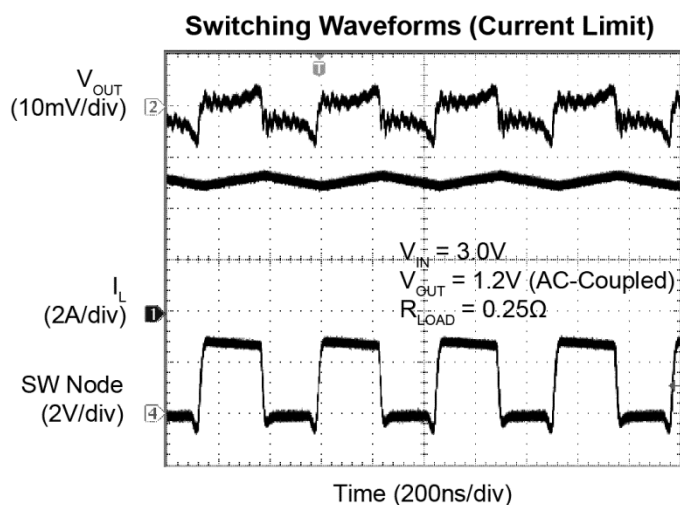
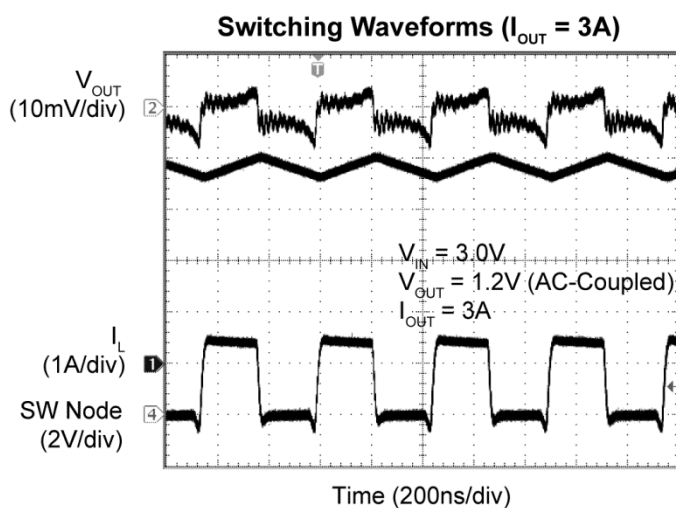
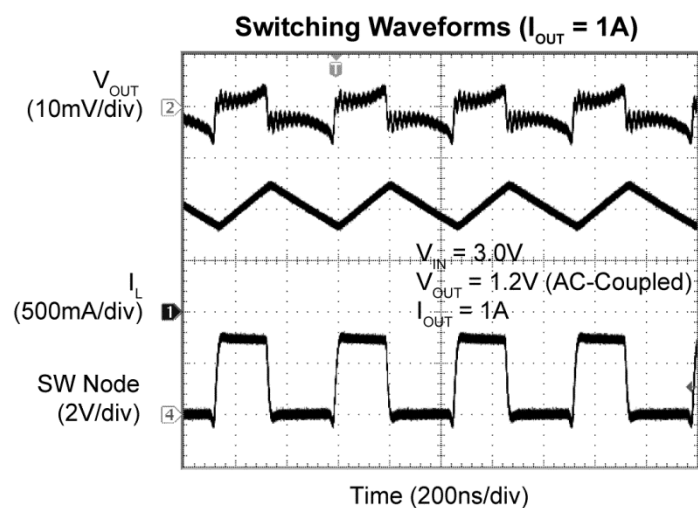
### 1.4V Pre-Bias Start-Up (EN Rising)



### Switching Waveforms ( $I_{OUT} = 0A$ )

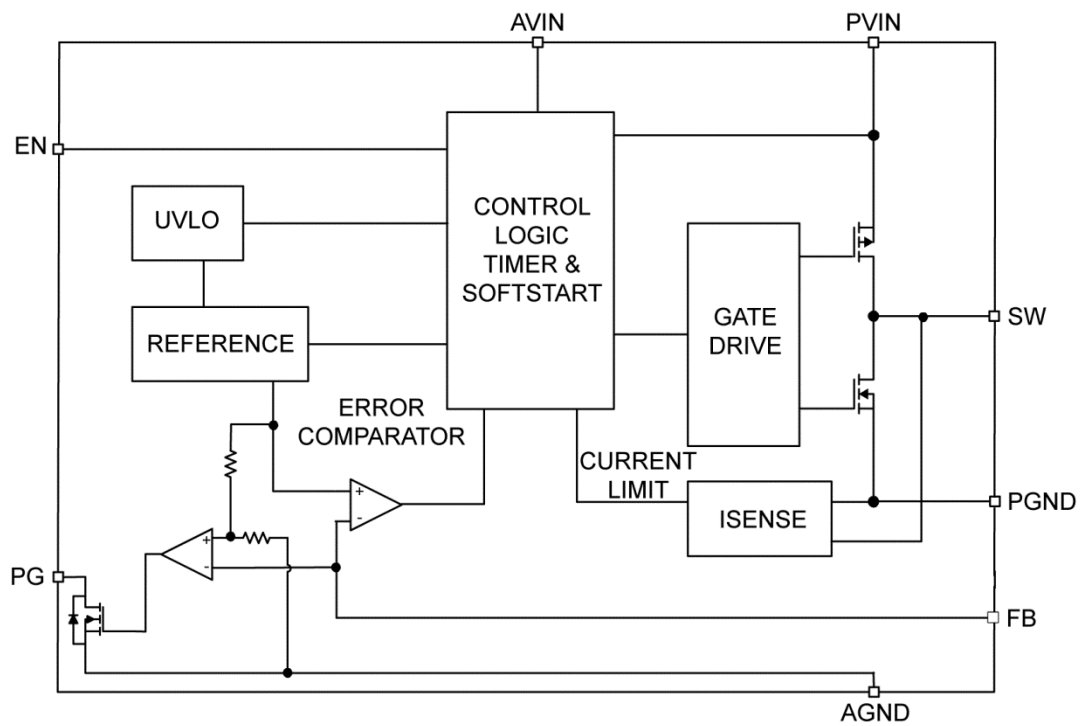


## Functional Characteristics (Continued)





## Functional Block Diagram



## Functional Description

### PVIN

The power input (PVIN) pin provides power to the internal MOSFETs for the switch mode regulator section of the MIC4930. The input supply operating range is from 2.7V to 5.5V. A low-ESR ceramic capacitor of at least 10μF is required to bypass from PVIN to (power) GND. See the Application Information section for further details.

### AVIN

The analog power input (AVIN) pin provides power to the internal control and analog supply circuitry. Careful layout should be considered to ensure that high-frequency switching noise caused by PVIN is reduced before reaching AVIN. Always place a 1μF minimum ceramic capacitor very close to the IC between the AVIN and AGND pins. For additional high-frequency switching noise attenuation, RC filtering can be used ( $R = 10\Omega$ ).

### EN

A logic high signal on the enable (EN) pin activates the output of the switch. A logic low on EN deactivates the output and reduces the supply current to a nominal 0.01μA. Do not leave this pin floating.

### SW

The switch (SW) pin connects directly to one side of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load and output capacitor. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes whenever possible to avoid unwanted injection of noise.

### PGND

The power ground (PGND) pin is the ground return terminal for the high current in the switching node SW. The current loop for the PGND should be as short as possible and kept separate from the AGND net whenever applicable.

### AGND

The analog ground (AGND) pin is the ground return terminal for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the Layout Recommendations for further details.

### PG

The power-is-good (PG) pin is an open-drain output that indicates logic high when the output voltage is typically above 88% of its steady-state voltage. A pull-up resistor of 10kΩ or greater should be connected from PG to VOUT.

### FB

To program the output voltage, an external resistive divider network is connected to this pin from the output voltage to AGND, as shown in the Typical Application circuit on page 1, and is compared to the internal 0.625V reference within the regulation loop. The following formula is used to program the output voltage.

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) \quad \text{Eq. 1}$$

Recommended feedback resistor values:

V <sub>OUT</sub>	R1	R2
1.0V	120k	180k
1.2V	274k	294k
1.5V	316k	226k
1.8V	301k	160k
2.5V	316k	105k
3.3V	309k	71.5k

The feed-forward capacitor ( $C_F$  in the Typical Application diagram) is typically in the range of 22pF to 39pF. The MIC4930 features an internal ripple injection network, whose current is injected into the FB node and integrated by  $C_F$ . Thus, the waveform at FB is approximately a triangular ripple. The size of  $C_F$  dictates the amount of ripple amplitude at the FB node. Smaller values of  $C_F$  yield higher FB ripple amplitudes and better stability, but also somewhat degrade line regulation and transient response.

### Hyper Speed Control™

MIC4930 uses an ON- and OFF-time proprietary ripple-based control loop that features three different timers:

- Minimum ON Time
- Maximum ON Time
- Minimum OFF Time

When the required duty cycle is very low, the required OFF time is typically far from the minimum OFF time limit (about 176ns typically). In this case, the MIC4930 operates by delivering a determined ON time at each switching cycle, depending on the input voltage. A new ON time is invoked by the error comparator when the FB voltage falls below the regulation threshold. In this mode, the MIC4930 operates as an adaptive constant-ON-time ripple controller with nearly constant switching frequency. Regulation takes place by controlling the valley of the FB ripple waveform.

When higher duty cycles are required, regulation can no longer be maintained by decreasing the OFF time below

the minimum OFF time limit. When this limit is reached, the OFF time is no longer reduced, and the MIC4930 smoothly transitions to an ON-time modulation mode. In the ON-time modulation region, frequency reduces with the increase of the required ON-time / duty cycle, and regulation finally takes place on the peak of the FB ripple waveform.

Note that because of the shift of the regulation threshold between different modes, line regulation might suffer when the input voltage and/or duty cycle variations force the MIC4930 to switch from one regulation mode to the other. In applications where wide input voltage variations are expected, ensure that the line regulation is adequate for the intended application.

## Application Information

The MIC4930 is a highly efficient, 3A synchronous buck regulator ideally suited for supplying processor core and I/O voltages from a 5V or 3.3V bus.

### Input Capacitor

A 10 $\mu$ F ceramic capacitor or greater should be placed close to the PVIN pin and PGND pin for bypassing. A X5R or X7R temperature rating is recommended for the input capacitor. Take into account C vs. bias effect in order to estimate the effective capacitance and the input ripple at the V<sub>IN</sub> voltage.

### Output Capacitor

The MIC4930 is designed for use with a 10 $\mu$ F or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response. A low equivalent series resistance (ESR) ceramic output capacitor is recommended based upon performance, size, and cost. Ceramic capacitors with X5R or X7R temperature ratings are recommended.

### Inductor Selection

When selecting an inductor, it is important to consider the following factors:

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)
- Core losses

The MIC4930 is designed for use with a 1 $\mu$ H to 2.2 $\mu$ H inductor. For faster transient response, a 1 $\mu$ H inductor will yield the best result. For lower output ripple, a 2.2 $\mu$ H inductor is recommended.

Inductor current ratings are generally given in two methods: permissible DC current, and saturation current. Permissible DC current can be rated for a 20°C to 40°C temperature rise. Saturation current can be rated for a 10% to 30% loss in inductance. Ensure that the nominal current of the application is well within the permissible DC current ratings of the inductor, also depending on the allowed temperature rise. Note that the inductor permissible DC current rating typically does not include inductor core losses. These are a very important contribution to the total inductor core loss and temperature increase in high-frequency DC-to-DC converters, since core losses increase with at least the square of the excitation frequency. For more accurate core loss estimation, it is recommended to refer to manufacturers' datasheets or websites.

When saturation current is specified, make sure that there is enough design margin, so that the peak current does not cause the inductor to enter saturation.

Also pay attention to the inductor saturation characteristic in current limit. The inductor should not heavily saturate even in current limit operation, otherwise the current might instantaneously run away and reach potentially destructive levels. Typically, ferrite-core inductors exhibit an abrupt saturation characteristic, while powdered-iron or composite inductors have a soft-saturation characteristic.

Peak current can be calculated by using Equation 2.

$$I_{PEAK} = \left[ I_{OUT} + V_{OUT} \left( \frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right] \quad \text{Eq. 2}$$

As shown by the calculation above, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or inductance, the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the typical application circuit and Bill of Materials for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations subsection.

### Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied (see Typical Characteristics section).

$$\text{Efficiency\%} = \left( \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100 \quad \text{Eq. 3}$$

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of  $I^2R$ . Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET  $R_{DS(on)}$  multiplied by the switch current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. The device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at high frequency and the switching transitions make up the switching losses.

At the higher currents for which the MIC4930 is designed, efficiency loss is dominated by MOSFET  $R_{DS(on)}$  and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, thereby reducing the internal  $R_{DS(on)}$ . This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In that case,

inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as in:

$$P_{DCR} = I_{OUT}^2 \times DCR \quad \text{Eq. 4}$$

From that, the loss in efficiency due to inductor DCR and core losses ( $P_{CORE}$ ) can be calculated as in Equation 5.

$$\text{Efficiency Loss (\%)} = \left[ 1 - \left( \frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{DCR} + P_{CORE}} \right) \right] \times 100 \quad \text{Eq. 5}$$

### External Ripple Injection

The MIC4930 control loop is ripple-based, and relies on an internal ripple injection network to generate enough ripple amplitude at the FB pin when negligible output voltage ripple is present. The internal ripple injection network is typically sufficient when recommended R1-R2 and  $C_F$  values are used. The FB ripple amplitude should fall in the 20mV to 100mV range.

If significantly lower divider resistors and/or higher  $C_F$  values are used, the amount of internal ripple injection may not be sufficient for stable operation. In this case, external ripple injection is needed. This is accomplished by connecting a series  $R_{inj}$ - $C_{inj}$  circuit between the SW and the FB pins, as shown in Figure 1.

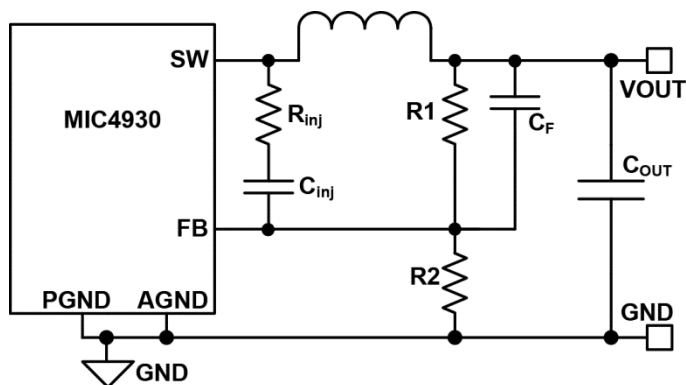


Figure 1. External Ripple Injection

The injected ripple is

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \quad \text{Eq. 6}$$

with  $K_{div}$  given by

$$K_{div} = \frac{R1/R2}{R_{inj} + R1/R2} \quad \text{Eq. 7}$$

and

$V_{IN}$  = Power stage input voltage

$D = V_{OUT}/V_{IN}$  = Duty cycle

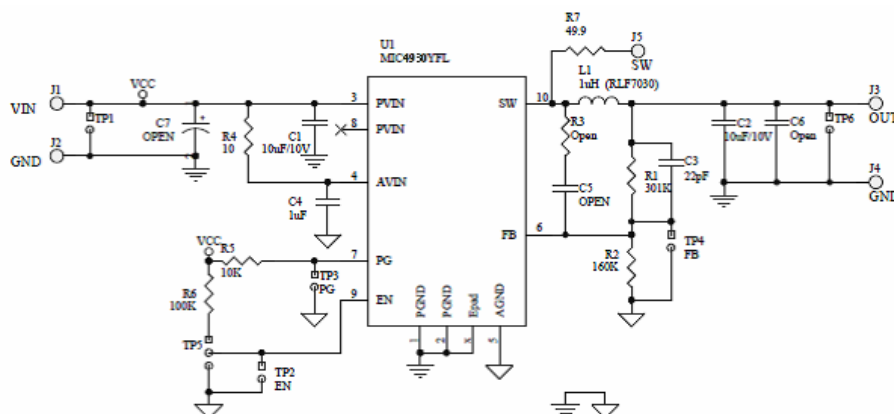
$f_{SW}$  = Switching frequency

$\tau = (R1//R2//R_{inj}) \times C_F$

In Equations 6 and 7, it is assumed that the time constant associated with  $C_F$  must be greater than the switching period.

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1 \quad \text{Eq. 8}$$

## Evaluation Board Circuit



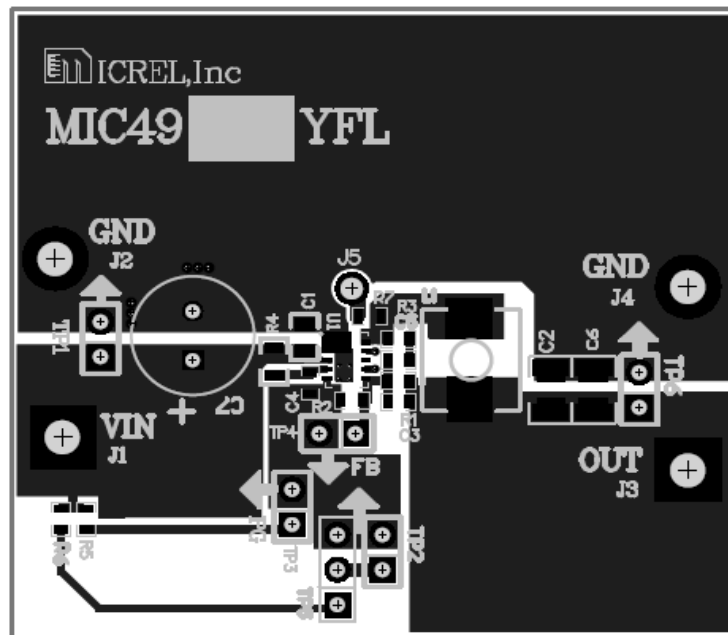
## Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1,	C2012X5R1A106M125AB	TDK <sup>(7)</sup>	Ceramic capacitor, 10µF, 10V X5R, Size 0805	2
C2	GRM219R61A106ME44	Murata <sup>(8)</sup>		
C3	C1608C0G1H220J080AA	TDK	Ceramic capacitor, 22pF, 50V, C0G, Size 0603	1
	GRM1885C1H220JA01	Murata		
C4	C1608X5R1A105M080AC	TDK	Ceramic capacitor, 1µF, 10V, X5R, Size 0603	1
	GRM185R61A105ME26	Murata		
C5			DNP, Size 0603	0
C6			DNP, Size 1210	0
C7			DNP, Radial, 8mm diameter polarized capacitor	0
L1	RLF7030T-1R0N6R4	TDK	1µH, 6.4A, 7.3mΩ, L7.3mm × W6.8mm × H3.2mm	1
	CLF6045T-1R0N	TDK	1µH, 4.5A, 11mΩ, L6.2mm × W5.9mm × H4.5mm	
	VLP6045LT-1R0N	TDK	1µH, 6.5A, 13mΩ, L6.8mm × W6.8mm × H4.5mm	
	CDRH5D28RH125NP-1R0PC	Sumida <sup>(9)</sup>	1µH, 4.1A, 13.5mΩ, L6.3mm × W6.2mm × H3.0mm	
R1	CRCW06033013FK	Vishay <sup>(10)</sup>	Resistor, 301kΩ, Size0603	1
R2	CRCW06031603FK	Vishay	Resistor, 160kΩ, Size 0603	1
R3			DNP, Size 0603	0
R4	CRCW060310R0FK	Vishay	Resistor, 10Ω, Size 0603	1
R5	CRCW06031002FK	Vishay	Resistor, 10kΩ, Size 0603	1
R6	CRCW06031003FK	Vishay	Resistor, 100kΩ, Size 0603	1
R7	CRCW060349R9FK	Vishay	Resistor, 49.9Ω, Size 0603, for monitoring SW node only	1
U1	MIC4930YFL	Micrel, Inc. <sup>(11)</sup>	Hyper Speed Control™ 3A Buck Regulator	1

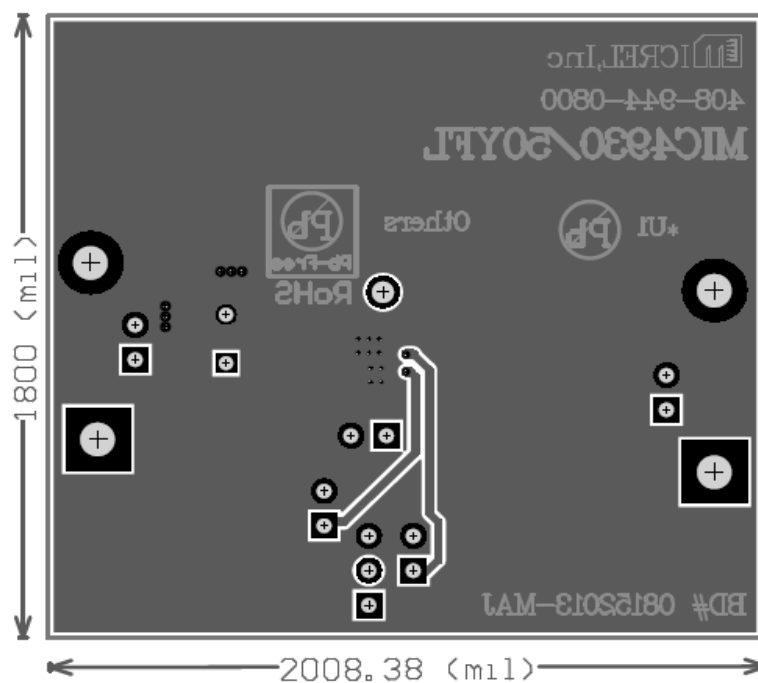
### Notes:

7. TDK: [www.tdk.com](http://www.tdk.com).
8. Murata: [www.murata.com](http://www.murata.com).
9. Sumida: [www.sumida.com](http://www.sumida.com).
10. Vishay: [www.vishay.com](http://www.vishay.com).
11. Micrel, Inc.: [www.micrel.com](http://www.micrel.com).

## PCB Layout Recommendations

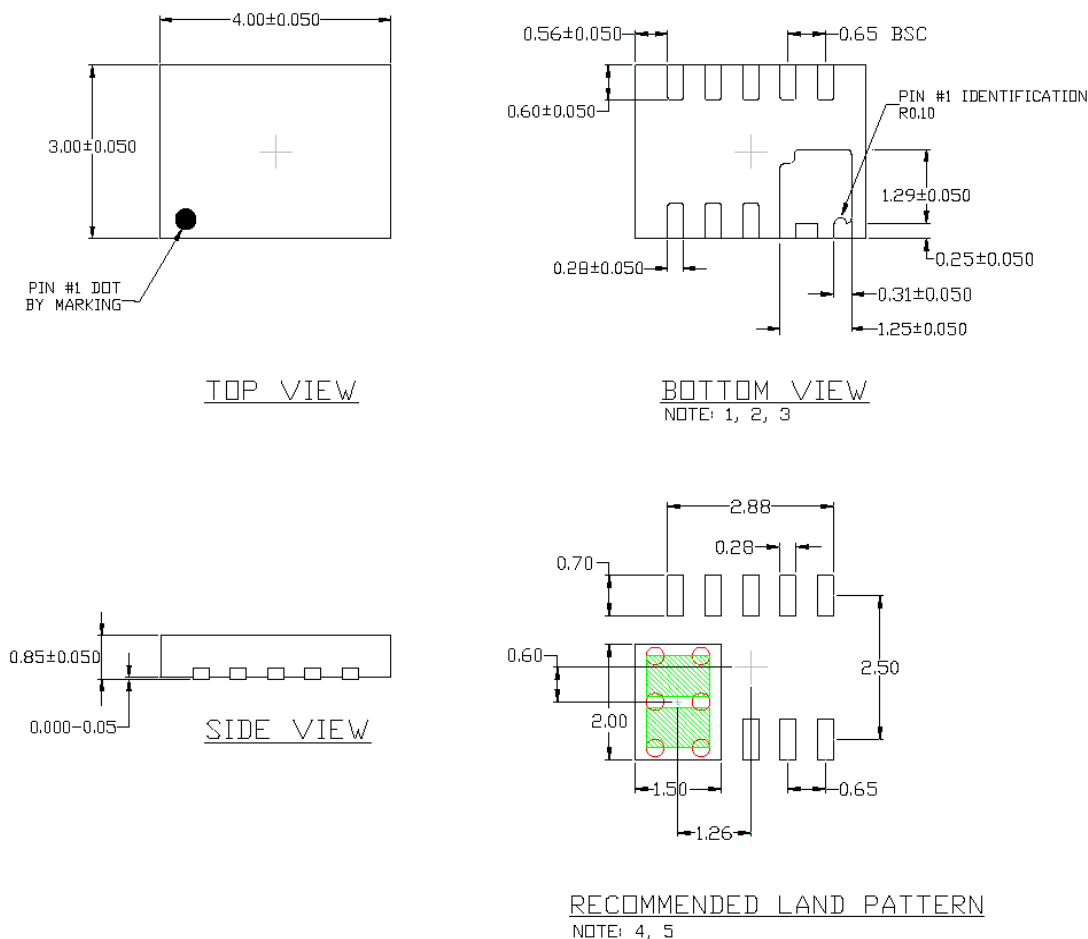


Top Layer



Bottom Layer

## Package Information<sup>(12)</sup>



## NOTE:

1. MAX PACKAGE WARPAGE IS 0.05MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. GREEN RECTANGLES (SHADED AREA) REPRESENT STENCIL OPENING ON EXPOSED AREA. SIZE IS 0.85X0.87 MM, 1.07 MM PITCH SPACING
5. RED CIRCLES REPRESENT THERMAL VIAS & SHOULD BE CONNECTED TO GND FOR MAX PERFORMANCE. 0.30 - 0.35 MM RECOMMENDED DIAMETER, 0.80MM PITCH SPACING

### 10-Pin DFN 3mm x 4mm (FL)

**Note:**

12. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).



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