MIC2829

3G/4G HEDGE/LTE PMIC with Six Buck Converters, Eleven LDOs and SIM Card Level Translation

General Description

The MIC2829 is a highly integrated Power Management Integrated Circuit (PMIC) designed for 3G/4G (HEDGE/LTE and WiMAX) USB wireless applications. It is a complete power management solution which provides power to processors, dual standard RF (such as HEDGE/LTE or WiMAX) transceivers and power amplifiers, memory, USB-PHY associated I/O interfaces and other system requirements.

The MIC2829 incorporates six DC/DC buck converters, eleven LDOs and digital level shifters for SIM Card support inside a single package. Four of the six integrated DC/DC buck converters incorporate HyperLight Load™ (HLL) technology. Each of these buck regulators operate at high switching speed in PWM mode (4MHz/2.5MHz) and maintain high efficiency in light load conditions. The high speed PWM operation allows the use of very small inductors and capacitors minimizing board area while the HLL mode enables 87% efficiency at 1mA. HyperLight Load™ technology also has unmatched load transient response to support advance portable processor requirements.

The remaining two DC/DC buck converters support 100% duty cycle operation and can deliver greater than 96% efficiency. This allows pre-regulation of system LDOs for high efficiency power system partitioning.

The MIC2829 has eleven low dropout regulators (LDOs). Five general purpose LDOs provide low dropout, excellent output accuracy of ±3% and only require 40µA of ground current for each to operate. The remaining six are high performance Low Noise Regulators (LNRs) which provide high PSRR and low output noise for sensitive RF subsystems. Each LNR requires only 20µA of ground current to operate. The MIC2829 also has three high speed level shifters for digital SIM Card signal translation and a 50mA SIM power supply.

The MIC2829 is available in a 76-pin 5.5mm x 5.5mm LGA and an 85-pin 5.5mm x 5.5mm FBGA package. The operating junction temperature range for both packages is from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's website at: www.micrel.com.

Features

- Input voltage range: 2.7V to 5.5V

Six DC Step-Down Regulators

- Four HyperLight Load™ step-down regulators
  - Low quiescent current – typical 40µA
  - DC1: 4MHz / 1000mA
  - DC2: 4MHz / 300mA (with voltage scaling)
  - DC3: 2.5MHz / 600mA
  - DC4: 4MHz / 600mA (with adjustable delay POR)
- Two PWM step-down regulators
  - DC5 and DC6: Fixed 2MHz / 800mA
  - 100% duty cycle

Eleven Low Dropout Regulators (LDOs)

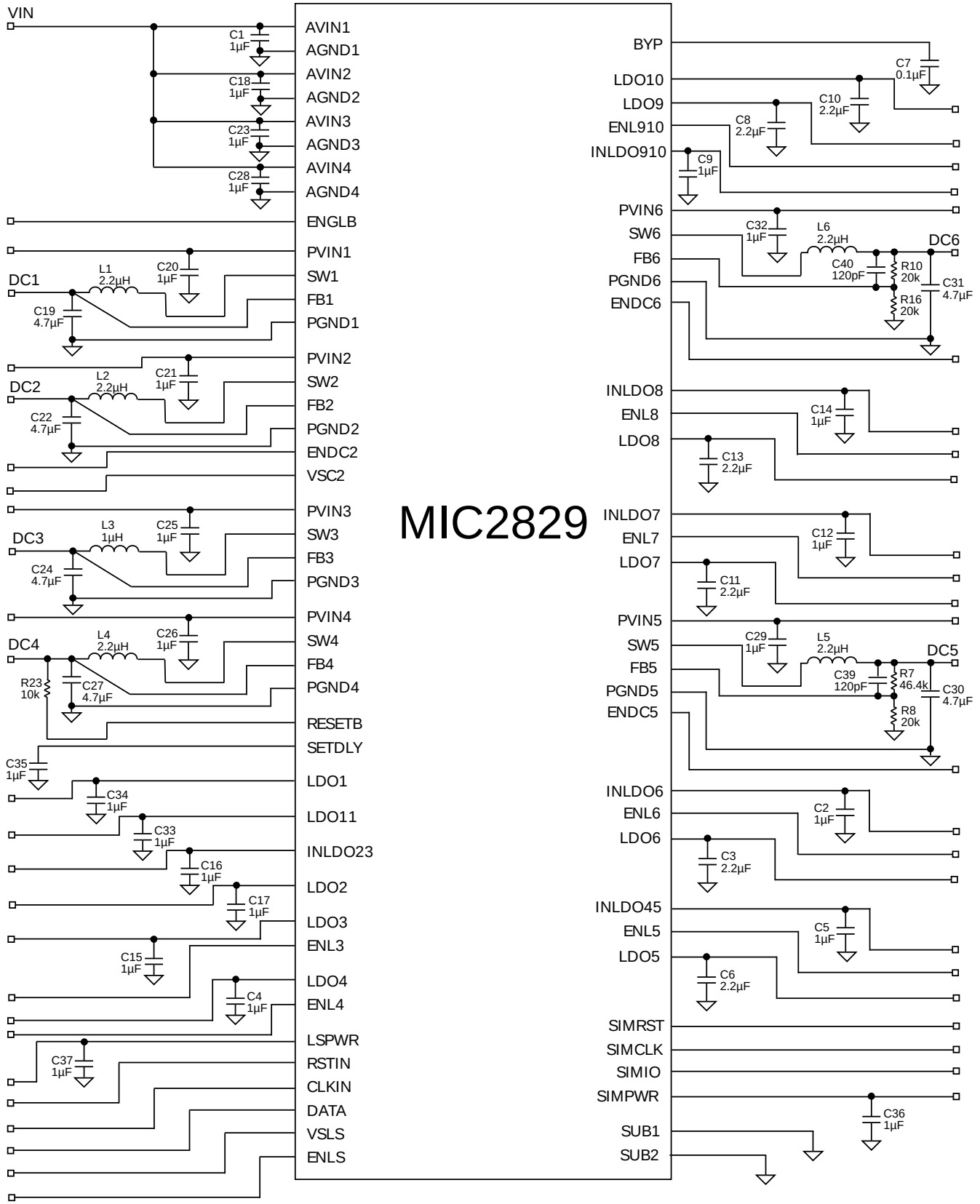
- Five general purpose 200mA LDOs (LDO1-4, LDO11)
  - LDO3: 38mV dropout at 100mA
  - LDO2 and LDO4: 80mV dropout at 100mA
  - LDO1 and LDO11: 115mV dropout at 100mA
  - Output accuracy ± 3%
  - 40µA ground current
- Six high performance 200mA LNRs (LDO5-10)
  - High PSRR 70dB at 1kHz
  - Low noise: 20µV_{RMS}
  - 40mV dropout at 100mA
  - Output accuracy ± 3%
  - 20µA ground current
- SIM card level translator
- SIM card power supply (50mA)
- Thermal shutdown and current limit protection
- UVLO – under voltage lockout protection
- 76-pin 5.5mm x 5.5mm LGA package
- 85-pin 5.5mm x 5.5mm FBGA package
- –40°C to +125°C operating junction temperature range

Applications

- 4G LTE USB modems
- 3G/4G (HEDGE/LTE) wireless chipsets
- WiMAX modems
- Express card modems
- UMPC/notebook PC wireless data communications
- Portable applications

HyperLight Load is a trademark of Micrel, Inc.

Typical Application



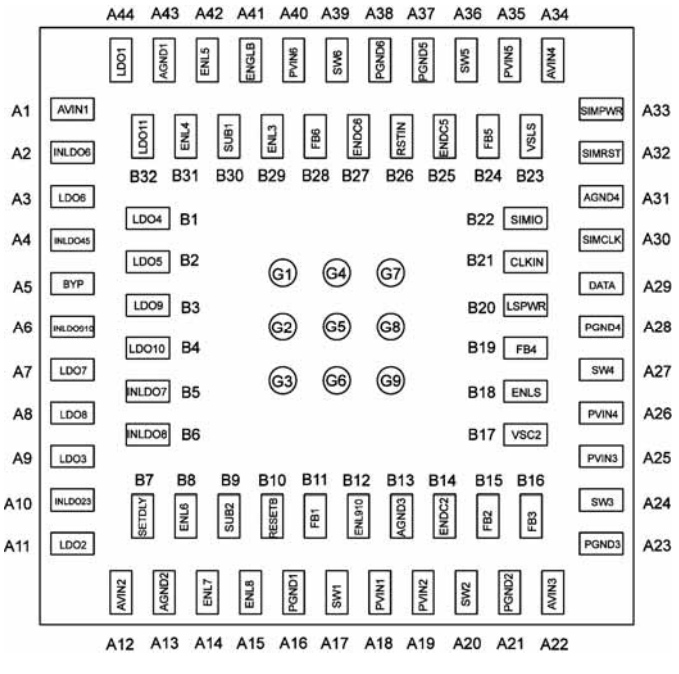
Ordering Information

Part Number	Marking Code	Junction Temperature Range	Package	Lead Finish
MIC2829-A0YAL	MIC2829-A0	-40°C to +125°C	76-Pin 5.5mm x 5.5mm LGA	Pb-Free
MIC2829-B0YAB[1]	MIC2829-B0	-40°C to +125°C	85-Pin 5.5mm x 5.5mm FBGA	Pb-Free

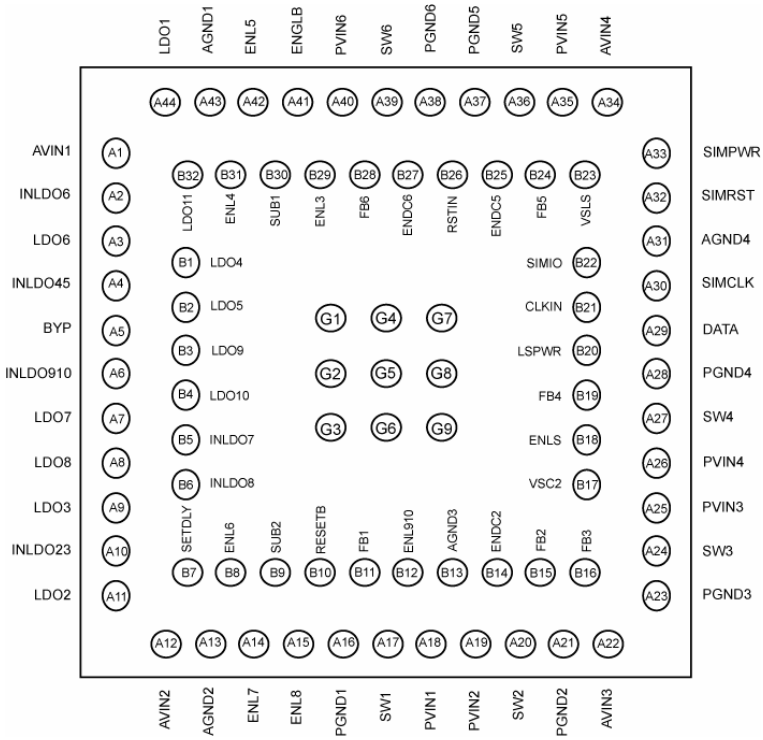
Output	Output Voltage (A0 Option)	Output Voltage (B0 Option)
DC1	1.2V	1.15V
DC2	1.0V / 1.2V	1.0V / 1.2V
DC3	3.0V	3.0V
DC4	1.8V	1.8V
DC5	ADJ	ADJ
DC6	ADJ	ADJ
LDO1	3.3V	3.3V
LDO2	2.5V	2.5V
LDO3	2.8V	2.8V
LDO4	2.85V	2.85V
LNR5	2.8V	2.8V
LNR6	2.5V	2.5V
LNR7	1.8V	1.8V
LNR8	1.5V	1.35V
LNR9	1.2V	1.2V
LNR10	1.2V	1.2V
LDO11	2.8V	2.8V

Note:
1. Contact Micrel Marketing for details.

Pin Configuration



76-Pin 5.5mm x 5.5mm LGA Package (AL)
(Top View)



85-Pin 5.5mm x 5.5mm FBGA Package (AB)
(Top View)

Pin Description

Pin # A	Pin # B	Pin # G	Pin name	Description
A1			AVIN1	Analog supply to chip. All AVIN pins should be tied together.
A2			INLDO6	Supply input to LNR6.
A3			LDO6	LNR6 output.
	B1		LDO4	LDO4 output.
A4			INLDO45	Supply input to LDO4 and LNR5.
	B2		LDO5	LNR5 output.
A5			BYP	Reference bypass pin. Connect a 0.1µF capacitor-to-ground.
	B3		LDO9	LNR9 output.
A6			INLDO910	Supply input to LNR9 and LNR10.
	B4		LDO10	LNR10 output.
A7			LDO7	LNR7 output.
	B5		INLDO7	Supply input to LNR7.
A8			LDO8	LNR8 output.
	B6		INLDO8	Supply input to LNR8.
A9			LDO3	LDO3 output.
A10			INLDO23	Supply input to LDO2 and LDO3.
A11			LDO2	LDO2 output.
A12			AVIN2	Analog supply to chip. All AVIN pins should be tied together.

Pin # A	Pin # B	Pin # G	Pin name	Description
	B7		SETDLY	Set delay pin for RESETB output (1sec/µF).
A13			AGND2	Analog ground. Connect all AGND pins together.
	B8		ENL6	Enable LNR6. Do not leave floating.
A14			ENL7	Enable LNR7. Do not leave floating.
	B9		SUB2	Guard ring ground connection. Connect to AGND1 and AGND2.
A15			ENL8	Enable LNR8. Do not leave floating.
	B10		RESETB	Open drain RESETB output (POR function).
A16			PGND1	Power ground of DC1.
	B11		FB1	Output sense pin of DC1.
A17			SW1	Switch output of DC1.
	B12		ENL910	Enable LNR9 and LNR 10. Do not leave floating.
A18			PVIN1	Power input of DC1.
	B13		AGND3	Analog ground. Connect all AGND pins together.
A19			PVIN2	Power input of DC2.
	B14		ENDC2	Enable DC2. Do not leave floating.
A20			SW2	Switch output of DC2.
	B15		FB2	Output sense pin of DC2.
A21			PGND2	Power ground of DC2.
	B16		FB3	Output sense pin of DC3.
A22			AVIN3	Analog supply to chip. All AVIN pins should be tied together.
A23			PGND3	Power ground of DC3.
A24			SW3	Switch output of DC3.
A25			PVIN3	Power input of DC3.
	B17		VSC2	Voltage Scaling pin DC2 (High sets 1.2V, Low sets 1.0V). Do not leave floating.
A26			PVIN4	Power input of DC4.
	B18		ENLS	Enable level shifter. Do not leave floating.
A27			SW4	Switch output of DC4.
	B19		FB4	Output sense pin of DC4.
A28			PGND4	Power ground of DC4.
	B20		LSPWR	Power input for level shifter input (1.8V).
A29			DATA	Digital data for SIM card.
	B21		CLKIN	Digital input clock for SIM card.
A30			SIMCLK	Level shifted Clock to SIM card.
	B22		SIMIO	Level shifted digital input/output to SIM card.
A31			AGND4	Analog ground. Connect all AGND pins together.
A32			SIMRST	Level shifted reset to SIM card.
A33			SIMPWR	Power supply to SIM card
A34			AVIN4	Analog supply to chip. All AVIN pins should be tied together.
	B23		VSLS	Level shift voltage select for SIM card. Do not leave floating.
A35			PVIN5	Power input of DC5.
	B24		FB5	Output sense pin of DC5 (Adjustable regulator).
A36			SW5	Switch output of DC5.

Pin # A	Pin # B	Pin # G	Pin name	Description
	B25		ENDC5	Enable DC5. Do not leave floating.
A37			PGND5	Power ground of DC5.
	B26		RSTIN	Digital reset input for SIM card.
A38			PGND6	Power ground of DC6.
	B27		ENDC6	Enable DC6. Do not leave floating.
A39			SW6	Switch output of DC6.
	B28		FB6	Output sense pin of DC6 (Adjustable regulator).
A40			PVIN6	Power input of DC6.
	B29		ENL3	Enable LDO3. Do not leave floating.
A41			ENGLB	Global enable for DC1, DC3, DC4 and LDO1, LDO2, LDO11. Do not leave floating.
	B30		SUB1	Guard ring ground connection. Connect to AGND1 and AGND2.
A42			ENL5	Enable LNR5. Do not leave floating.
	B31		ENL4	Enable LDO4. Do not leave floating.
A43			AGND1	Analog ground. Connect all AGND pins together.
	B32		LDO11	LDO11 output.
A44			LDO1	LDO1 output.
		G1	Thermal Via	Thermal via. Connect to ground.
		G2	Thermal Via	Thermal via. Connect to ground.
		G3	Thermal Via	Thermal via. Connect to ground.
		G4	Thermal Via	Thermal via. Connect to ground.
		G5	Thermal Via	Thermal via. Connect to ground.
		G6	Thermal Via	Thermal via. Connect to ground.
		G7	Thermal Via	Thermal via. Connect to ground.
		G8	Thermal Via	Thermal via. Connect to ground.
		G9	Thermal Via	Thermal via. Connect to ground.

Absolute Maximum Ratings[1]

All Power Input Supplies……-0.3 to 6V
All Logic Inputs…….....-0.3 to 6V
All Feedback Inputs .....-0.3 to (V_{AVIN} + 0.3V)
Ambient Storage Temperature ……-65°C to +150°C
ESD Rating[3].....ESD Sensitive
ESD Rating (SIMRST, CLK, IO, PWR pins).....8kV to GND

Operating Ratings[2]

Supply and Bias Voltage (V_{PVIN}, V_{AVIN})……..2.7V to 5.5V
Supply Voltage (V_{INLDO}) .. ……1.8V to V_{AVIN}
Supply Voltage (V_{LSPWR}) .....……1.6V to V_{AVIN}
All Logic Inputs .....……0V to V_{AVIN}
All Feedback Inputs .....……0V to V_{AVIN}
Junction Temperature Range (T_J)... ….-40°C ≤ T_J ≤ +125°C
Thermal Resistance
5.5mm x 5.5mm LGA (θ_{JA}).....38.7°C/W
5.5mm x 5.5mm FBGA (θ_{JA}).....38.7°C/W

Electrical Characteristics – General[4]

T_A = 25°C; $AVIN_X$ = 4.3V unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage Range	**All V_{AVIN} and V_{PVIN}**	**2.7**		**5.5**	V
Shutdown Current	V_{IN} = 5.0V All outputs disabled		1		µA
Enable (ENx) & Voltage Scaling Threshold (VSC2, VSLS)	High			**1.1**	V
	Low	**0.2**			V
Enable & Voltage Scaling Input Current	$V_{IL} \leq$ 0.2V			2	µA
	$V_{IH} \geq$ 1.1V			2	µA
Over-Temperature Shutdown Threshold			150		°C
Over-Temperature Hysteresis			10		°C
Under-voltage Lockout	V_{AVIN} rising	2.4	2.55	2.7	V
Auto-Discharge NFET Resistance[5]	When Out_x disabled; I_{OUT} = 3mA.		300		Ω
	When Out_x disabled; I_{OUT} = 3mA. DC5 & 6 pull down on feedback pin.		700		Ω

Electrical Characteristics – Quiescent Current[6]

T_A=25°C, AVINx = PVINx = INLDOx = ENGLB = 4.3V; ENx = 0V ; All I_{OUT} = 0mA unless otherwise noted.

Bold values indicate -40°C ≤ T_J ≤ 125°C.

Parameter	Condition	Min	Typ	Max	Unit
Initial Sequence I_Q	DC1, 3, 4 Non switching, No loads LDO 1, 2, 11 I_{OUT} = 100µA		220		µA
DC2 Additional I_Q	DC2 enabled. ENDC2 = 4.3V $V_{FB} \geq V_{OUTNOM}$ x 1.2 (Non switching)		10		µA
DC 5, 6 Additional I_Q	Per enabled DC. ENDCx = 4.3V $V_{FB} \geq$ 1.2V; I_{OUT} = 0mA (Non switching)		945		µA
LDO 3, 4, LSPWR Additional I_Q	Per enabled LDO. ENLx = 4.3V I_{OUT} =100µA		40		µA
LNR 5 – 10 Additional I_Q	Per enabled LNR. ENLx = 4.3V I_{OUT} =100µA		20		µA

Electrical Characteristics – Buck Regulator (DC1 – DC4)

T_A=25°C, AVINx = VSC2 = ENGLB = ENDC2 = 4.3V, L3 = 1.0µH, L1, 2, 4 = 2.2µH, C_{OUT} = 4.7µF, I_{OUT} = 20mA, unless noted. **Bold** values indicate -40°C ≤ T_J ≤ 125°C.

Parameter	Condition	Min	Typ	Max	Unit
Switch Current Limit	V_{OUT} = V_{OUTNOM} x 0.9, DC1	**1**	1.4		A
	V_{OUT} = V_{OUTNOM} x 0.9, DC3 & 4	**0.65**	1.5		
	V_{OUT} = V_{OUTNOM} x 0.9, DC2	**0.33**	1.1		
Output Voltage Accuracy		-3		3	%
Line Regulation	4.3V ≤ AVIN ≤ 5.5V, Iout = 20mA		0.4		%/V
Load Regulation	150mA ≤ I_{OUT} ≤ 400mA		0.5		%
HLL Buck Switch ON Resistance	$I_{SW1,3}$ = -100mA NMOS, DC1 & 3		0.4		Ω
	I_{SW4} = -100mA NMOS, DC4		0.45		
	I_{SW2} = -100mA NMOS, DC2		0.6		
	I_{SW3} = +100mA PMOS, DC3		0.5		
	$I_{SW1, 4}$ = +100mA PMOS, DC1 & 4		0.6		
	I_{SW2} = +100mA PMOS, DC2		1.1		
Soft Start Time	V_{OUT} = 90%		600		µs
Scale Transition Time DC2	DC2 only. Time to reach 90% target.		100		µs
Frequency	DC1, 2, 4 I_{LOAD} = 120mA		4		MHz
	DC3 I_{LOAD} = 120mA		2.5		
RESETB on DC4					
VTH Falling	Low Threshold, % of nominal DC4 output (Flag ON)	85			%
VTH Rising	High Threshold, % of nominal DC4 output (Flag OFF)			**96**	%
VOL	RESETB logic low voltage; IL = 250µA		0.02	0.05	V
I_{RESETB}	Flag Leakage Current, Flag OFF	-1	0.1	+1	µA
SETDLY input on DC4					
SETDLY Current Source	V_{SETDLY} = 0V	0.75	1.45	1.75	µA
SETDLY Threshold Voltage	RESETB = High		1.241		V

Electrical Characteristics – Buck Regulator (DC5, DC6)

T_A=25°C, AVINx = ENGLB = ENDC5 = ENDC6 = 4.3V, L = 2.2µH, C_{OUT} = 2.2µF, I_{OUT} = 100mA, unless otherwise noted.
Bold values indicate -40°C ≤ T_J ≤ 125°C.

Parameter	Condition	Min	Typ	Max	Unit
Switch Current Limit	V_{FB} = 0.9 V	**0.86**	1.3		A
FB Voltage Accuracy		0.97	1.0	1.03	V
Line Regulation	3.0V ≤ AVIN ≤ 5V , I_{LOAD} = 100mA		0.12		%
Load Regulation	20mA ≤ I_{OUT} ≤ 300mA		0.2		%
Soft Start Time	V_{OUT} = 90%; I_{LOAD} = 5mA		100		µs
DC Switch ON Resistance	I_{SW} = +100mA PMOS		0.4		Ω
	I_{SW} = -100mA NMOS		0.5		Ω
Switching Frequency		1.6	2	2.4	MHz
FB Pin Input Current			1		nA

Electrical Characteristics – Low Dropout Regulators (LDO1 – LDO4, LDO11)

T_A=25°C, AVINx = ENGLB = ENLx = 4.3V, V_{INLDOx} = Vout+1V, C_{OUT} = 1µF, I_{OUT} = 100µA, unless noted.
Bold values indicate -40°C ≤ T_J ≤ 125°C.

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage Range		1.8		**AVIN**	V
Current Limit		**200**			mA
Output Voltage Accuracy		-3		3	%
Dropout Voltage	LDO2, 4; I_{OUT} = 100mA; LDO3; I_{OUT} = 100mA; LDO1, 11; I_{OUT} = 100mA;		80 38 115	**125** **100** **210**	mV
Line Regulation	V_{OUT} + 1V ≤ V_{INLDO} ≤ 5.5V		0.02	**0.2**	%/V
Load Regulation	100µA ≤ I_{OUT} ≤ 100mA		0.4	**2**	%
Output Noise	100Hz to 100kHz; C_{OUT} = 2.2µF		65		µVrms
Ripple Rejection	f = 1kHz, C_{OUT} = 2.2µF		55		dB
Turn On Time	Enable to 90% nominal V_{OUT}		25		µs

Electrical Characteristics – Low Noise Regulators (LNR5 – LNR10)

T_A=25°C, AVINx = ENx= 4.3V, V_{INLDOx} = Vout+1V, C_{OUT} = 2.2µF, I_{OUT} = 100µA, unless noted.
Bold values indicate -40°C ≤ T_J ≤ 125°C.

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage Range	LNR5, 6, 7 LNR8, 9 ,10	1.8 1.7		**AVIN** **AVIN**	V
Current Limit		**200**			mA
Output Voltage Accuracy		-3		3	%
Dropout Voltage	LNR5, 6, 7; I_{OUT} = 100mA; LNR8, 9, 10		40 N/A	**75**	mV
Line Regulation	V_{OUT} + 1V ≤ V_{INLDOx} ≤ V_{AVIN}		0.02	**0.2**	%/V
Load Regulation	100µA ≤ I_{OUT} ≤ 100mA		0.4	2	%
Output Noise	100Hz to 100kHz; C_{OUT} = 2.2µF, C_{BYP} = 0.1µF		20		µVrms
Ripple Rejection	f = 1kHz, C_{OUT} = 2.2µF, C_{BYP} = 0.1µF		70		dB
Turn On Time	Enable to 90% nominal V_{OUT}		100		µs

Electrical Characteristics – SIM power supply and level translator

T_A=25°C, AVINx = ENGLB = ENLS = 4.3V, C_{OUT} = 1.0µF, I_{OUT} = 100µA, unless otherwise noted.
Bold values indicate -40°C ≤ T_J ≤ 125°C.

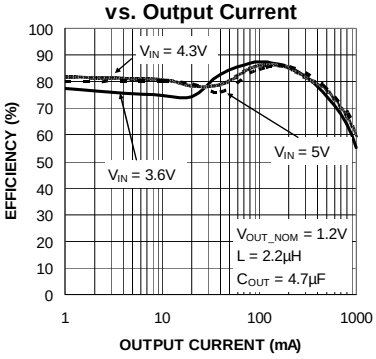
Parameter	Condition	Min	Typ	Max	Unit
Controller Voltage Input		1.62	1.8	1.98	V
Current Limit (SIMPWR)		**60**			mA
Output Voltage Accuracy	3V Output , I_{OUT} = 50mA 1.8V Output, I_{OUT} = 50mA	**2.7** **1.7**	3 1.8	**3.3** **2.0**	V
SIMPWR Turn On Time			500		µs
High Input Threshold	RSTIN, CLKIN (Y = V_{LSPWR})			**0.7*Y**	V
Low Input Threshold	RSTIN, CLKIN (Y = V_{LSPWR})	**0.2*Y**			V
SIMIO (V_{OH})	I_{OH} = 20µA, DATA = V_{LSPWR} (X = V_{SIMPWR})	**0.8*X**			V
SIMIO (V_{OL})	I_{OL} = -1mA, DATA = 0V			**0.4**	V
SIMRST, SIMCLK (V_{OH})	I_{OH} = 20µA, (X = V_{SIMPWR})	**0.9*X**			V
SIMRST, SIMCLK (V_{OL})	I_{OL} = -200µA			**0.4**	V
DATA (V_{OH})	I_{OH} = 20µA, SIMIO = V_{SIMPWR} (Y = V_{LSPWR})	**0.7*Y**			V
DATA (V_{OL})	I_{OL} = -200µA, SIMIO = 0V			**0.4**	V
DATA Pull Up Resistance	Between DATA and LSPWR	13	20	30	kΩ
SIMIO Pull Up Resistance	Between SIMIO and SIMPWR	6.5	10	14	kΩ
SIMCLK Rise/Fall Time	$C_{RSTIN,}$ C_{SMIIO} = 30pF (20-80%)		18		ns
SIMRST, SIMIO Rise/Fall Time	$C_{RSTIN,}$ C_{SMIIO} = 30pF (20-80%)		25		ns

Notes:

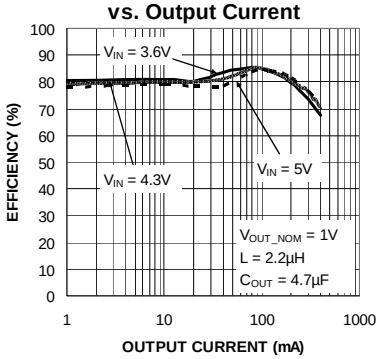
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.
5. All outputs are auto discharged with an internal NMOS when output is disabled.
6. Quiescent current is the total supply current minus any enabled LDO/LNR/LSPWR load current.

Typical Characteristics

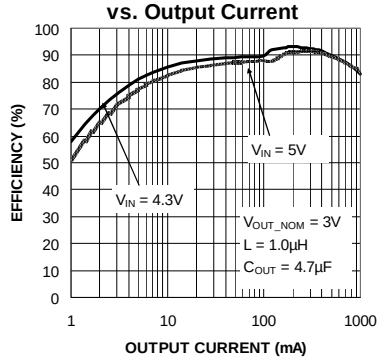
DC1 HLL Buck Efficiency vs. Output Current



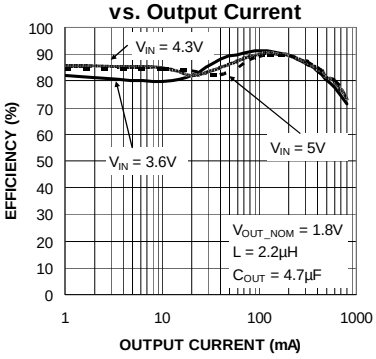
DC2 HLL Buck Efficiency vs. Output Current



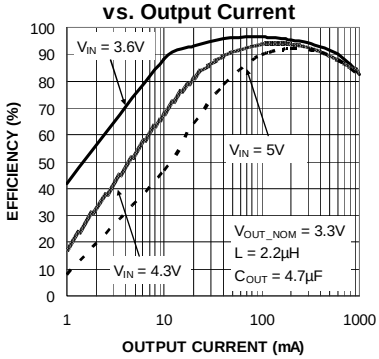
DC3 HLL Buck Efficiency vs. Output Current



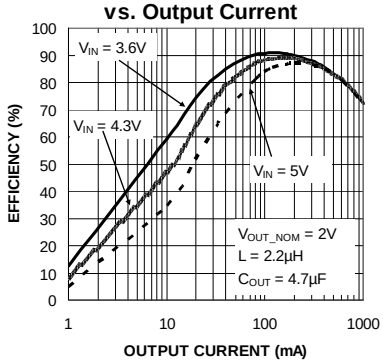
DC4 HLL Buck Efficiency vs. Output Current



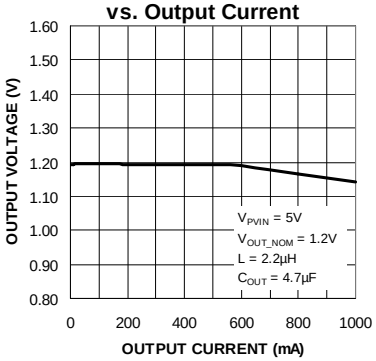
DC5 PWM Buck Efficiency vs. Output Current



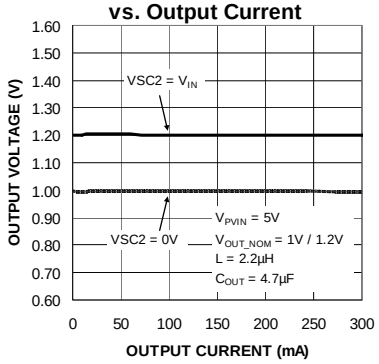
DC6 PWM Buck Efficiency vs. Output Current



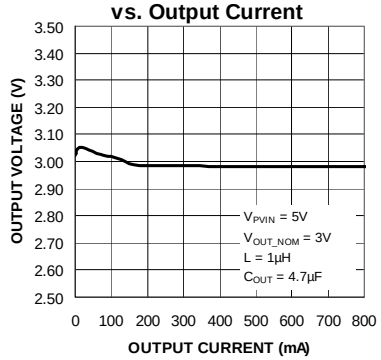
DC1 Output Voltage vs. Output Current



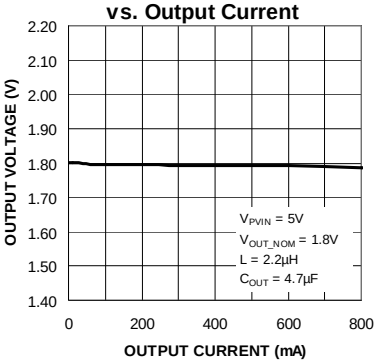
DC2 Output Voltage vs. Output Current



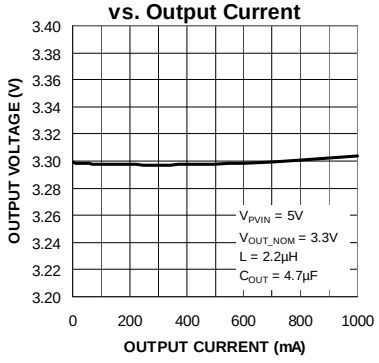
DC3 Output Voltage vs. Output Current



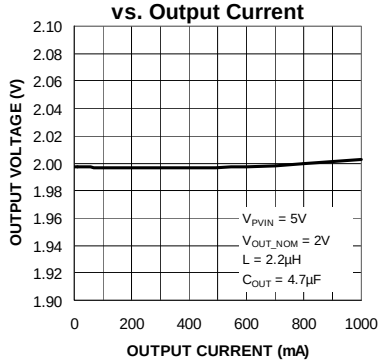
DC4 Output Voltage vs. Output Current



DC5 Output Voltage vs. Output Current

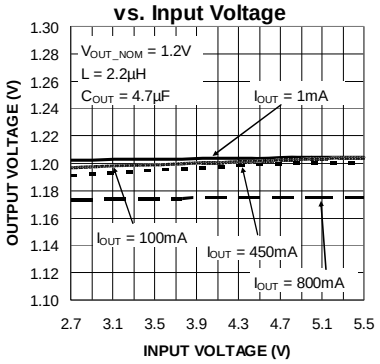


DC6 Output Voltage vs. Output Current

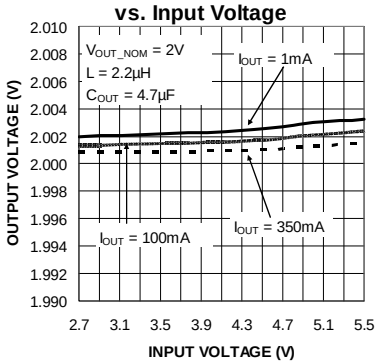


Typical Characteristics (Continued)

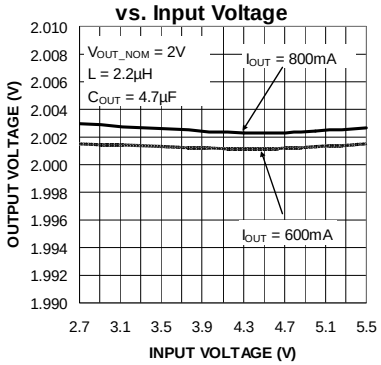
Typical HLL Output Voltage vs. Input Voltage



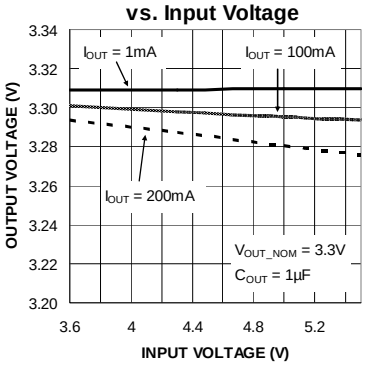
Typical PWM Output Voltage vs. Input Voltage



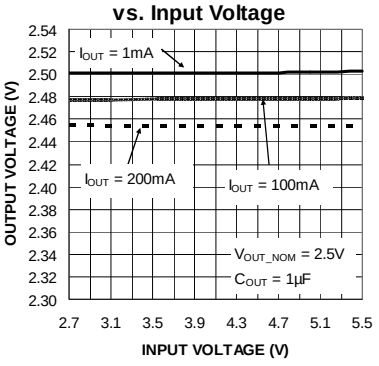
Typical PWM Output Voltage vs. Input Voltage



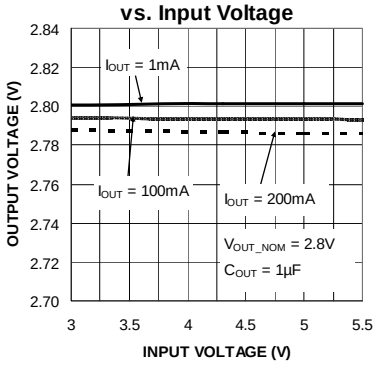
LDO1 Output Voltage vs. Input Voltage



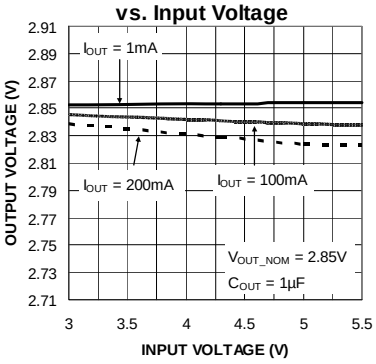
LDO2 Output Voltage vs. Input Voltage



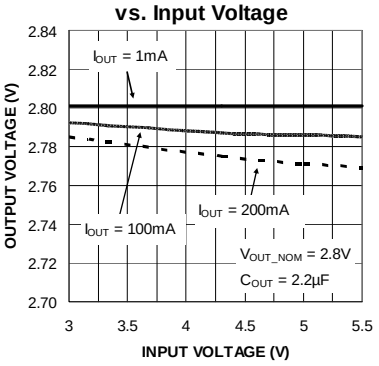
LDO3 Output Voltage vs. Input Voltage



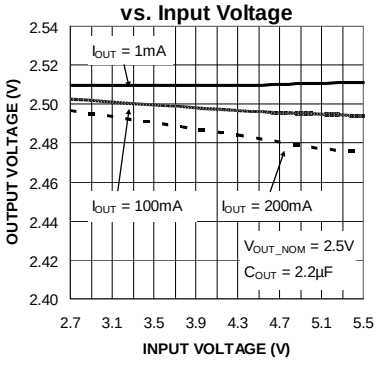
LDO4 Output Voltage vs. Input Voltage



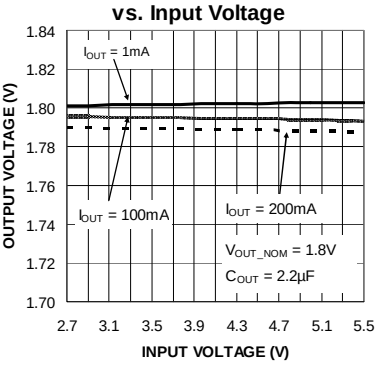
LNR5 Output Voltage vs. Input Voltage



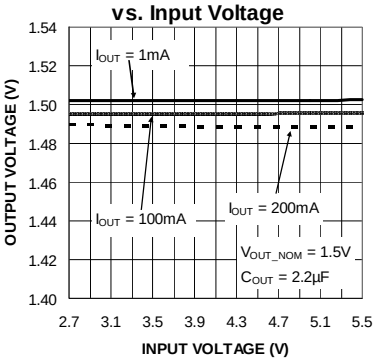
LNR6 Output Voltage vs. Input Voltage



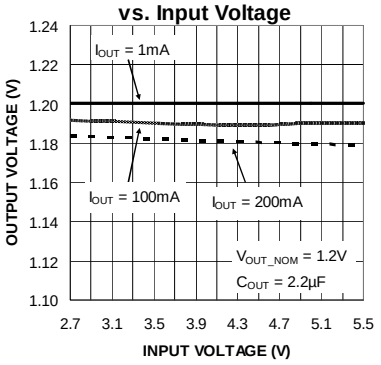
LNR7 Output Voltage vs. Input Voltage



LNR8 Output Voltage vs. Input Voltage

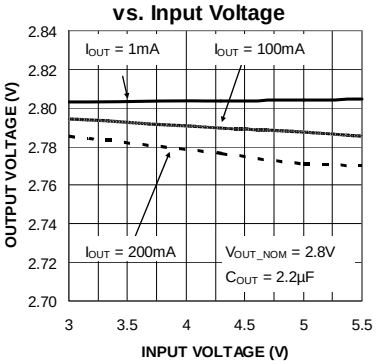


LNR9/10 Output Voltage vs. Input Voltage

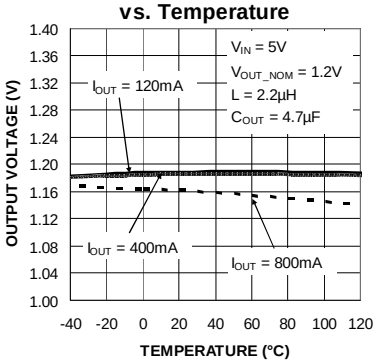


Typical Characteristics (Continued)

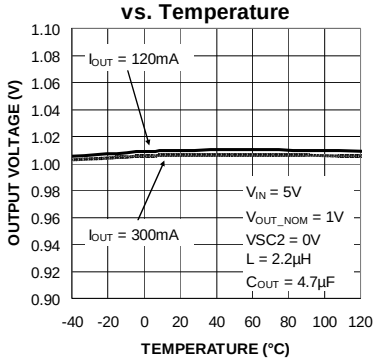
LDO11 Output Voltage vs. Input Voltage



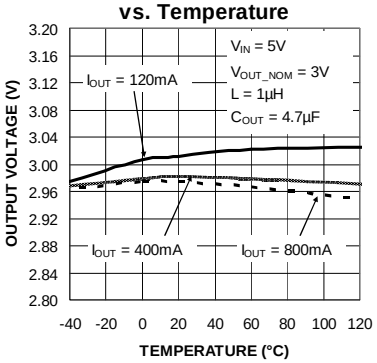
DC1 Output Voltage vs. Temperature



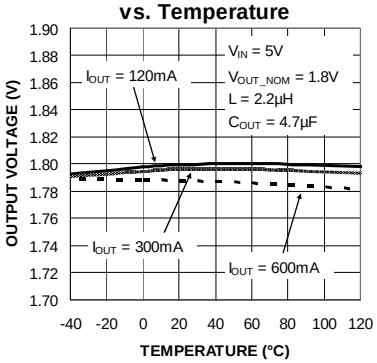
DC2 Output Voltage vs. Temperature



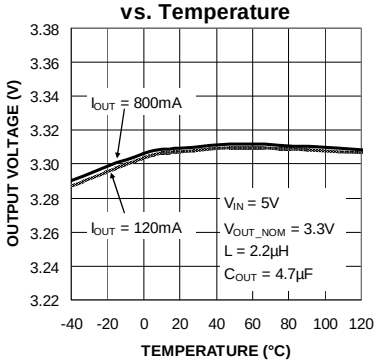
DC3 Output Voltage vs. Temperature



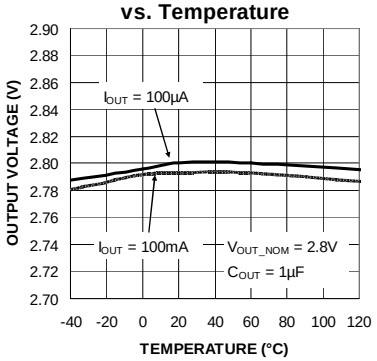
DC4 Output Voltage vs. Temperature



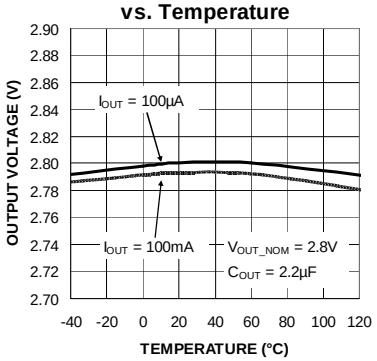
DC5/6 Output Voltage vs. Temperature



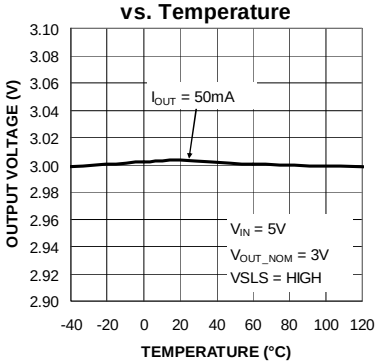
Typical LDO Output Voltage vs. Temperature



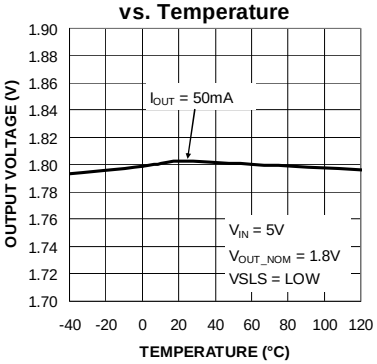
Typical LNR Output Voltage vs. Temperature



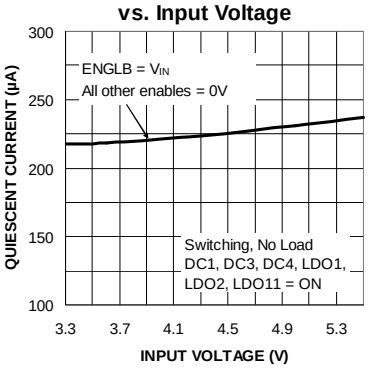
SIMPWR Output Voltage vs. Temperature



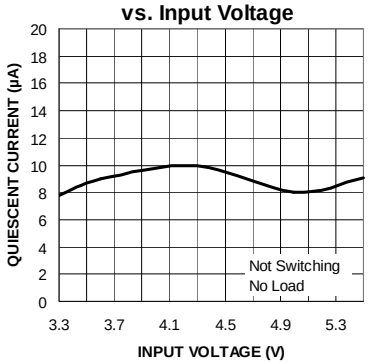
SIMPWR Output Voltage vs. Temperature



ENGLB Quiescent Current vs. Input Voltage

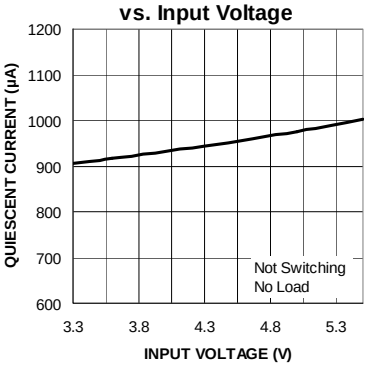


DC2 Quiescent Current vs. Input Voltage

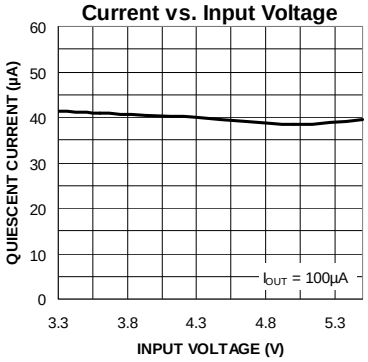


Typical Characteristics (Continued)

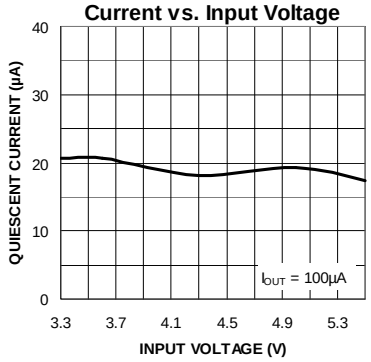
DC5/6 Quiescent Current vs. Input Voltage



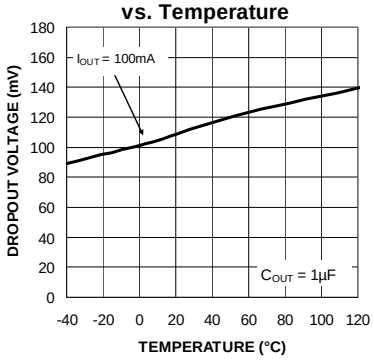
Typical LDO Quiescent Current vs. Input Voltage



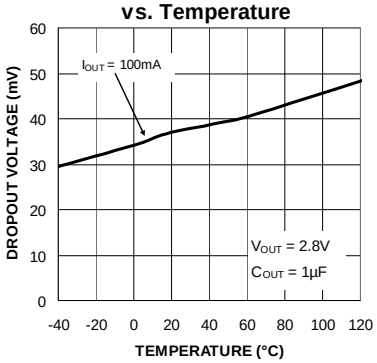
Typical LNR Quiescent Current vs. Input Voltage



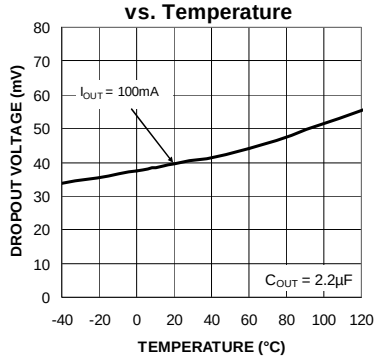
LDO1/11 Dropout vs. Temperature



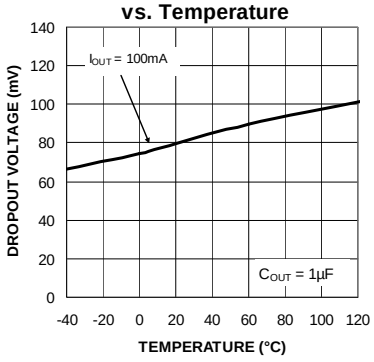
LDO3 Dropout vs. Temperature



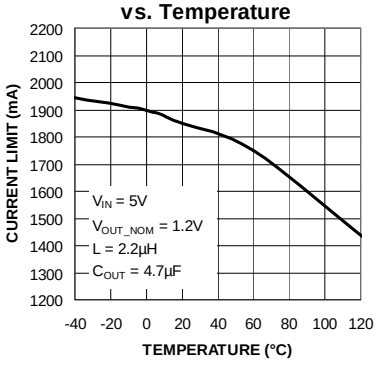
LNR5/6/7 Dropout vs. Temperature



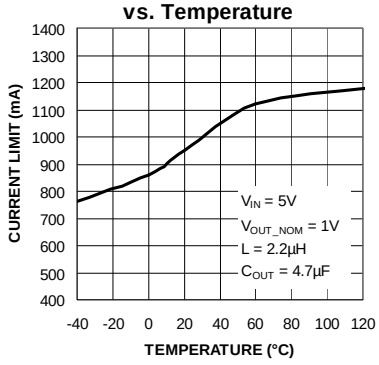
LDO2/4 Dropout vs. Temperature



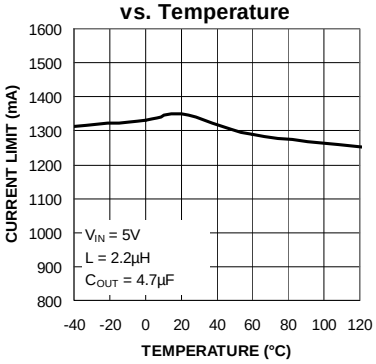
DC1 Current Limit vs. Temperature



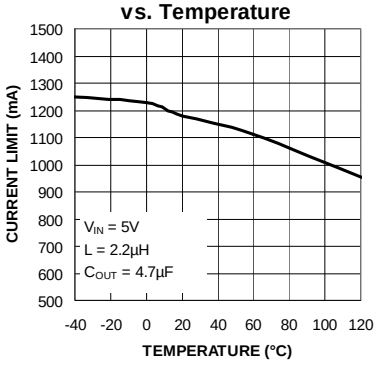
DC2 Current Limit vs. Temperature



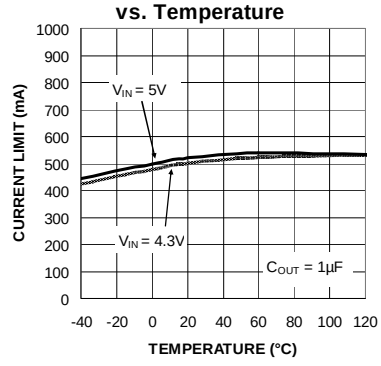
DC3/4 Current Limit vs. Temperature



DC5/6 Current Limit vs. Temperature

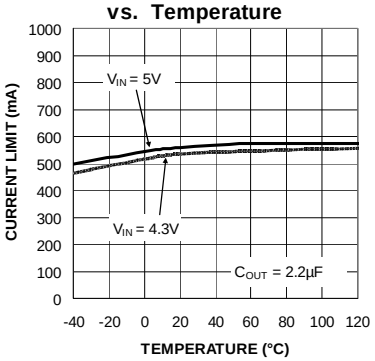


Typical LDO Current Limit vs. Temperature

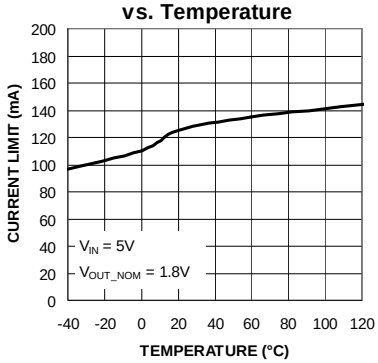


Typical Characteristics (Continued)

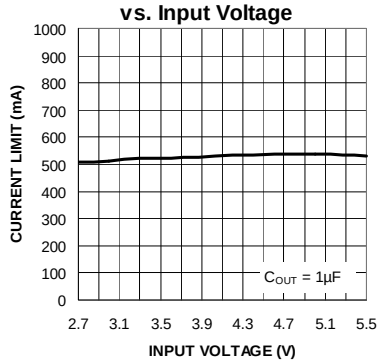
Typical LNR Current Limit vs. Temperature



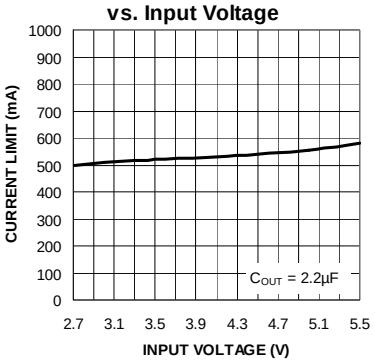
SIMPWR Current Limit vs. Temperature



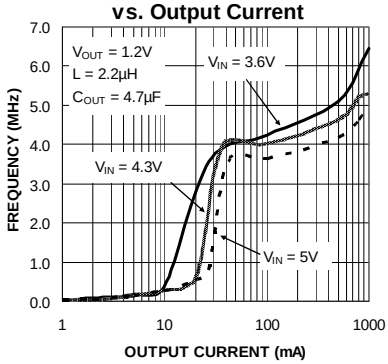
Typical LDO Current Limit vs. Input Voltage



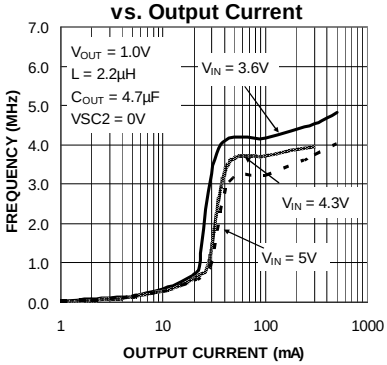
Typical LNR Current Limit vs. Input Voltage



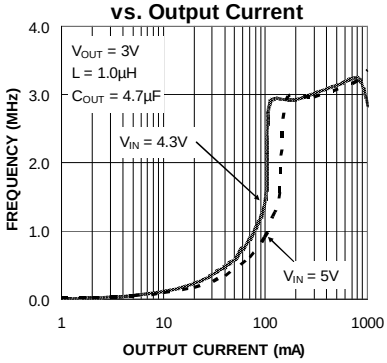
DC1 HLL SW Frequency vs. Output Current



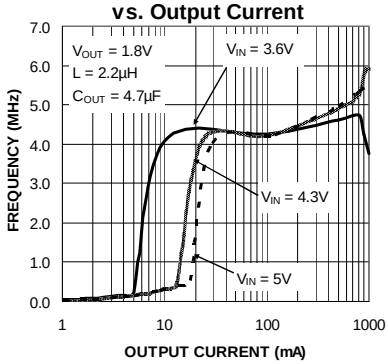
DC2 HLL SW Frequency vs. Output Current



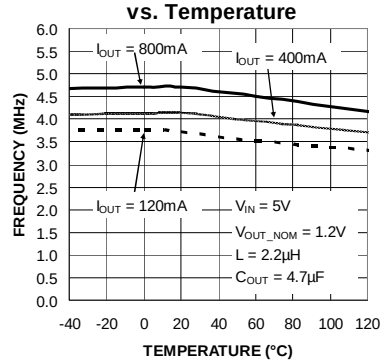
DC3 HLL SW Frequency vs. Output Current



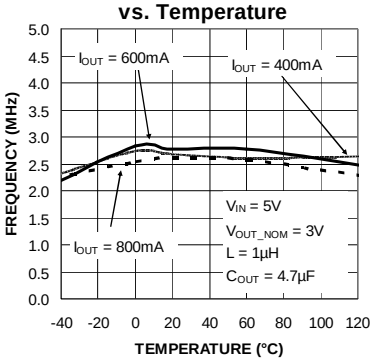
DC4 HLL SW Frequency vs. Output Current



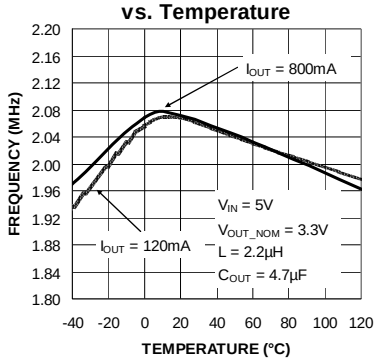
4MHz HLL SW Frequency vs. Temperature



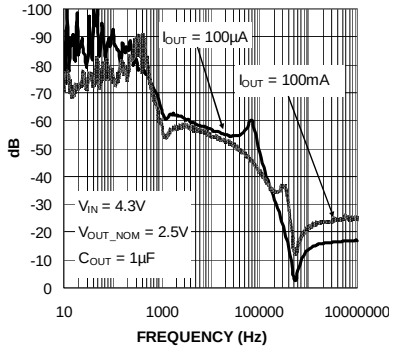
2.5MHz HLL SW Frequency vs. Temperature



DC5/6 PWM SW Frequency vs. Temperature

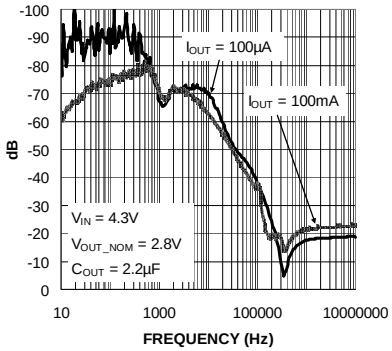


Typical LDO PSRR

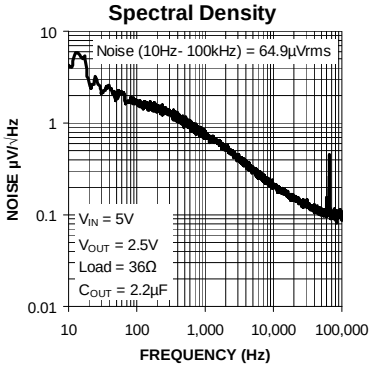


Typical Characteristics (Continued)

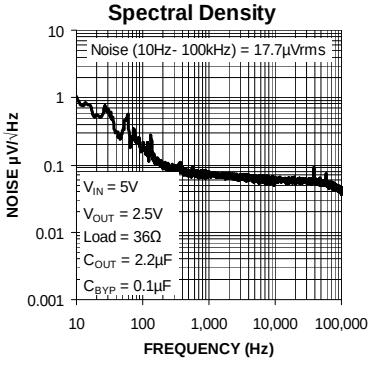
Typical LNR PSRR



Typical LDO Output Noise Spectral Density

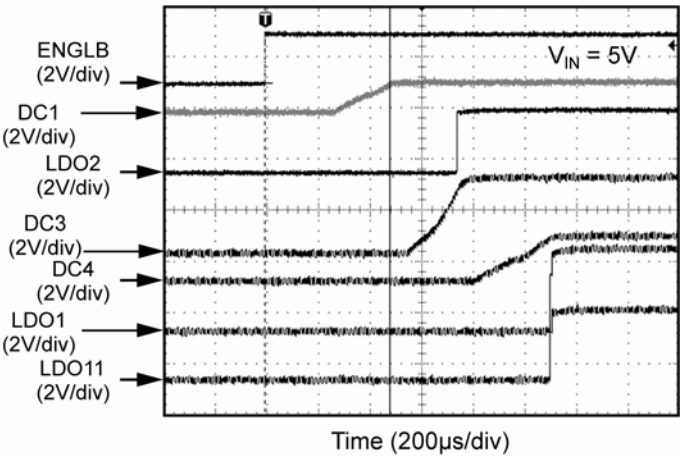


Typical LNR Output Noise Spectral Density

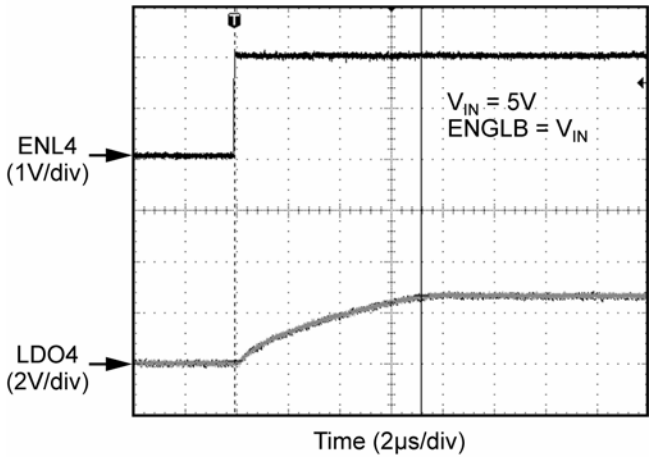


Functional Characteristics

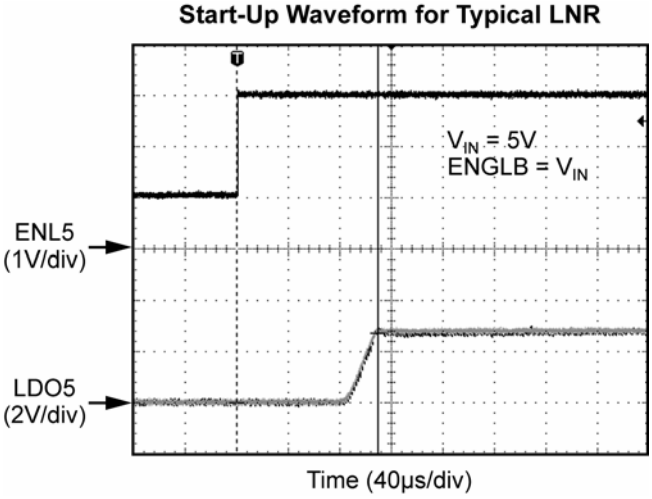
ENGLB Start-Up Sequencing



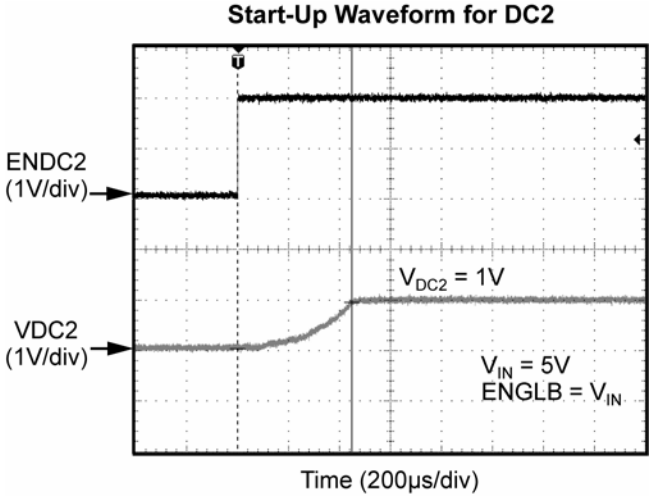
Start-Up Waveform for Typical LDO



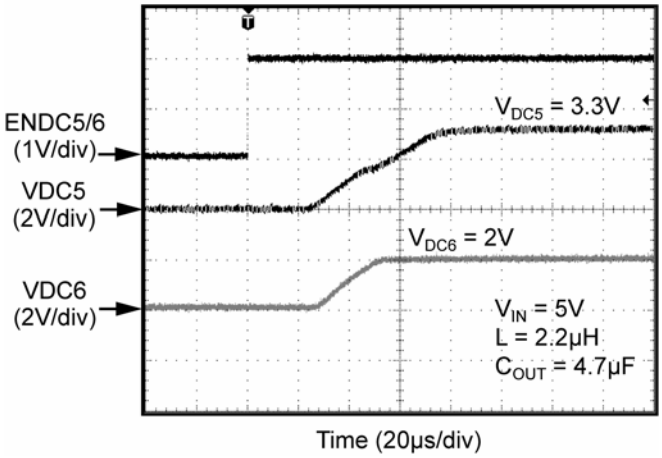
Start-Up Waveform for Typical LNR



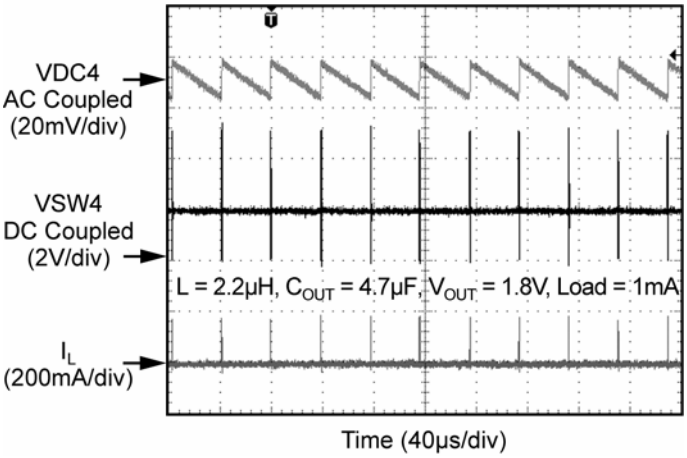
Start-Up Waveform for DC2



Start-Up Waveform for DC5/6

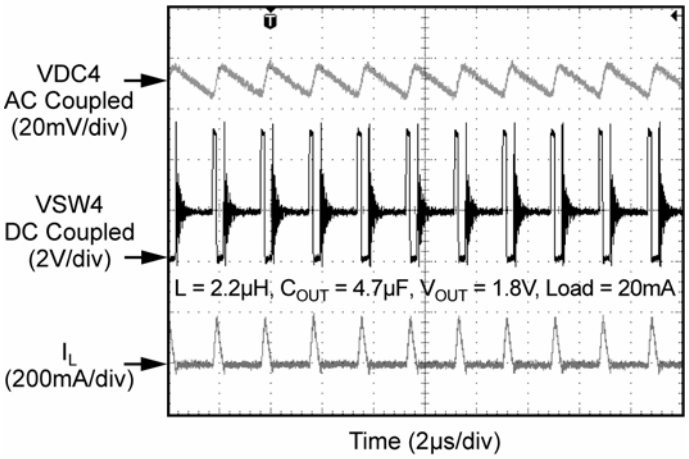


4MHz HLL Switching Waveform at 1mA

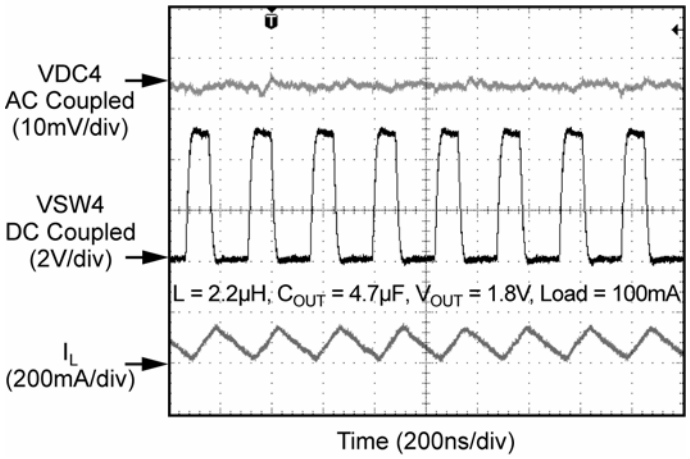


Functional Characteristics (Continued)

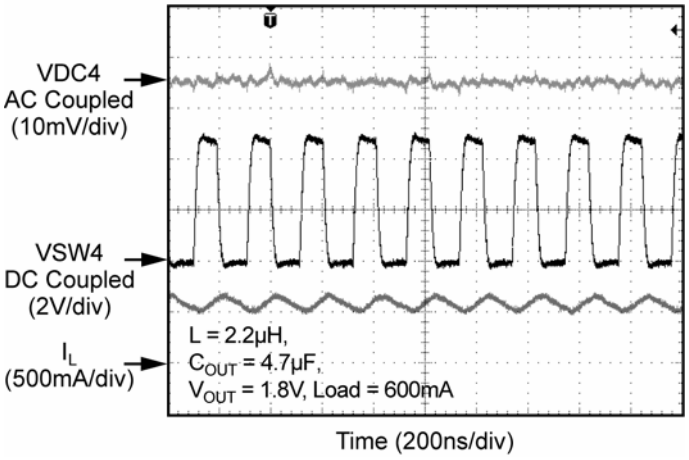
4MHz HLL Switching Waveform at 20mA



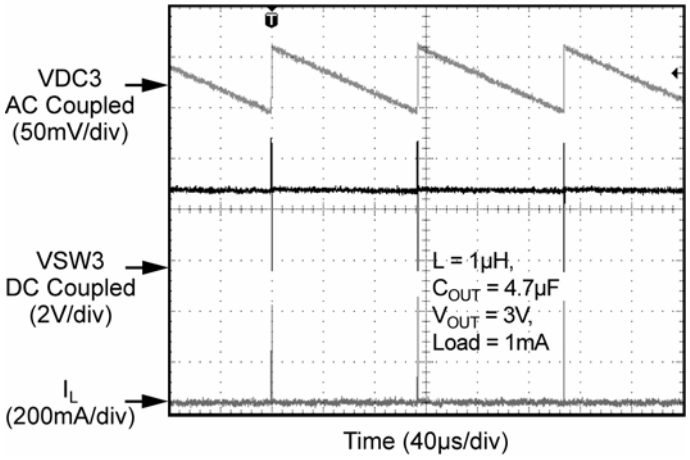
4MHz HLL Switching Waveform at 100mA



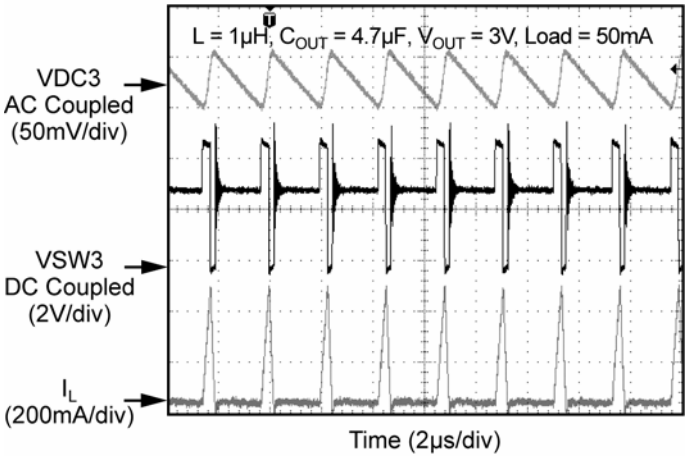
4MHz HLL Switching Waveform at 600mA



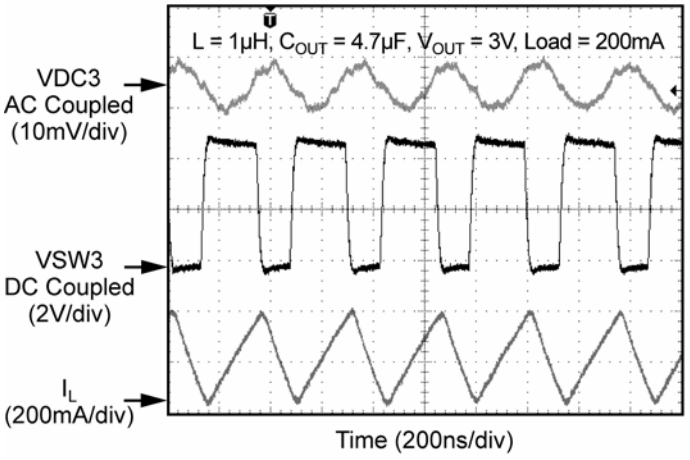
2.5MHz HLL Switching Waveform at 1mA



2.5MHz HLL Switching Waveform at 50mA

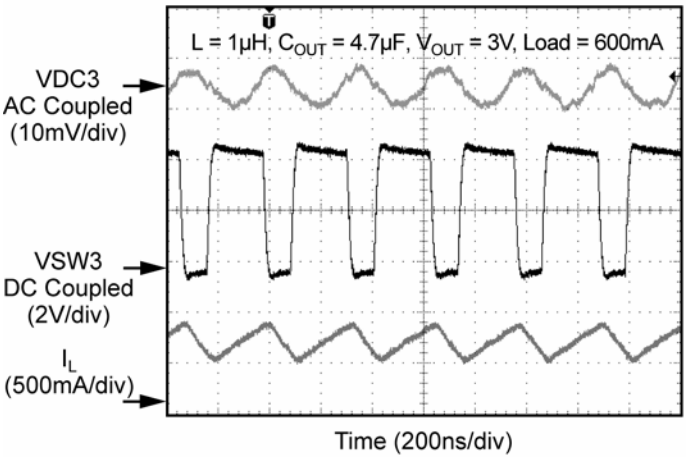


2.5MHz HLL Switching Waveform at 200mA

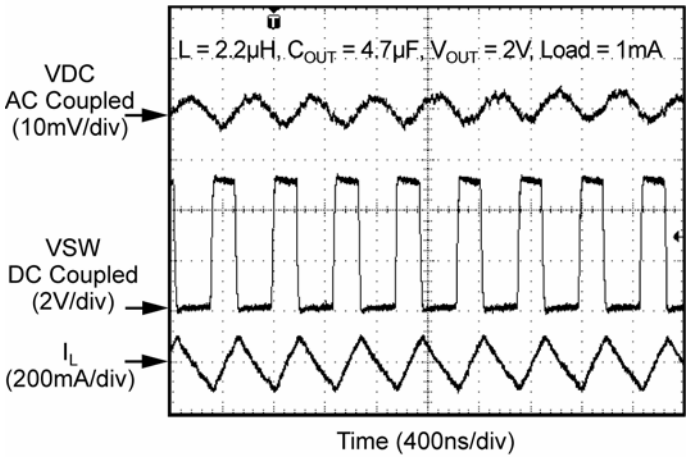


Functional Characteristics (Continued)

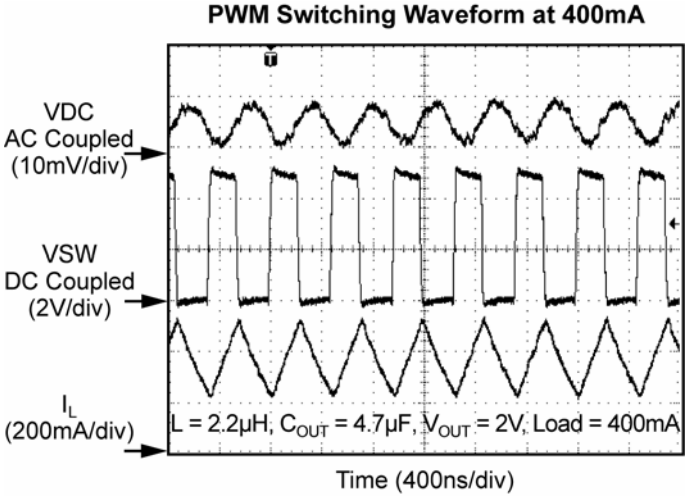
2.5MHz HLL Switching Waveform at 600mA



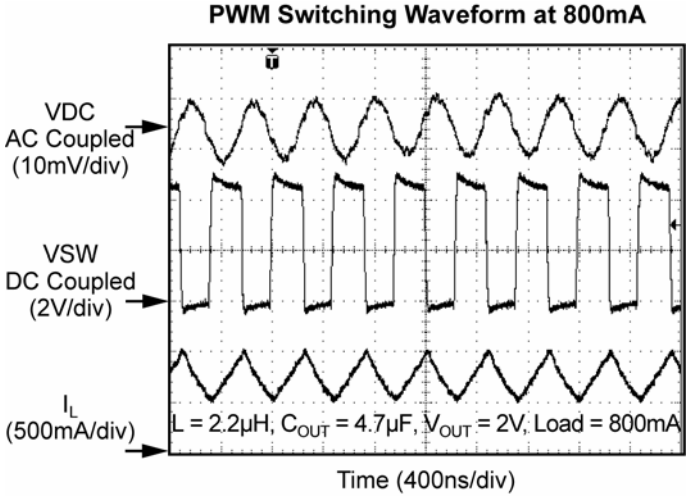
PWM Switching Waveform at 1mA



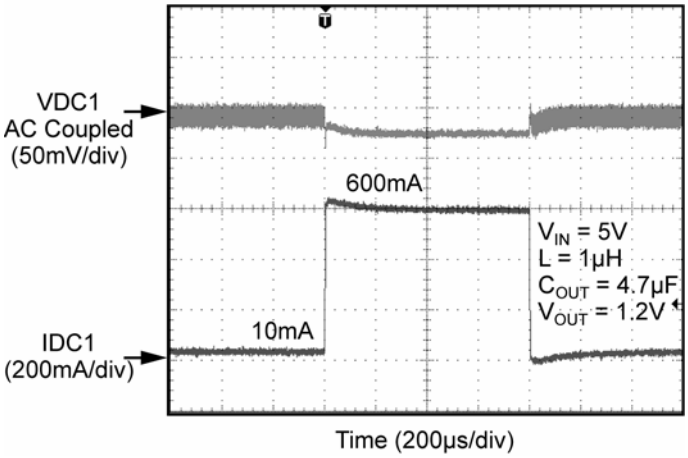
PWM Switching Waveform at 400mA



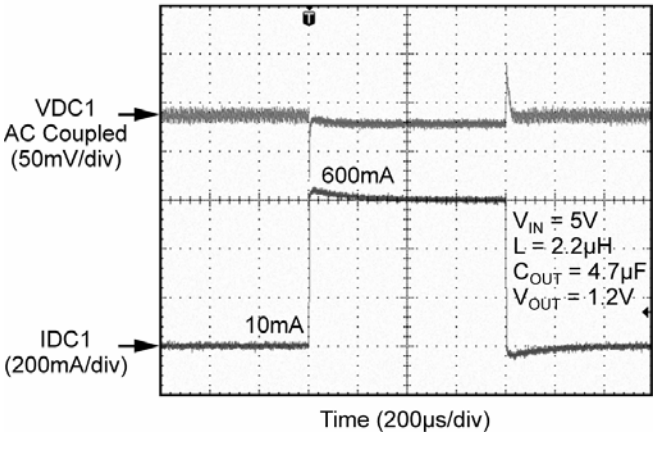
PWM Switching Waveform at 800mA



Load Transient HLL DC1 10mA to 600mA

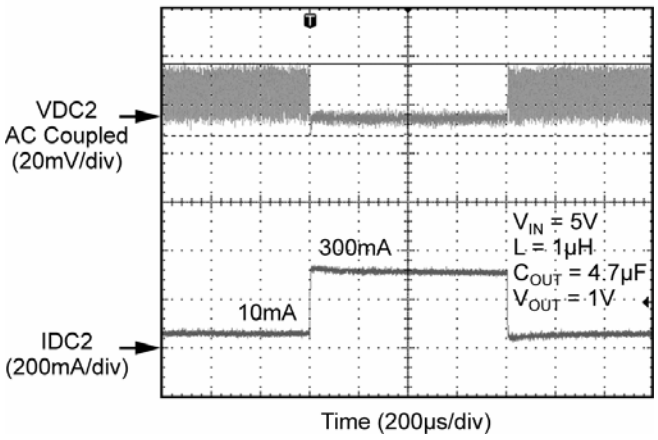


Load Transient HLL DC1 10mA to 600mA

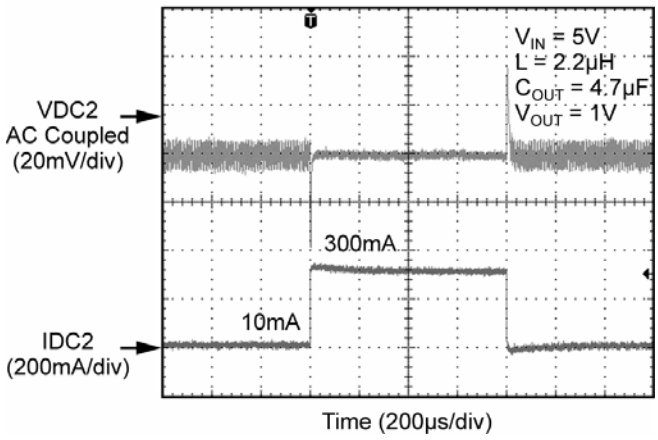


Functional Characteristics (Continued)

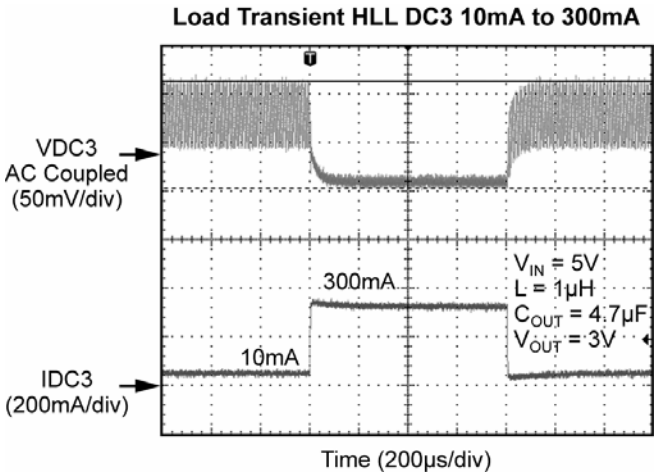
Load Transient HLL DC2 10mA to 300mA



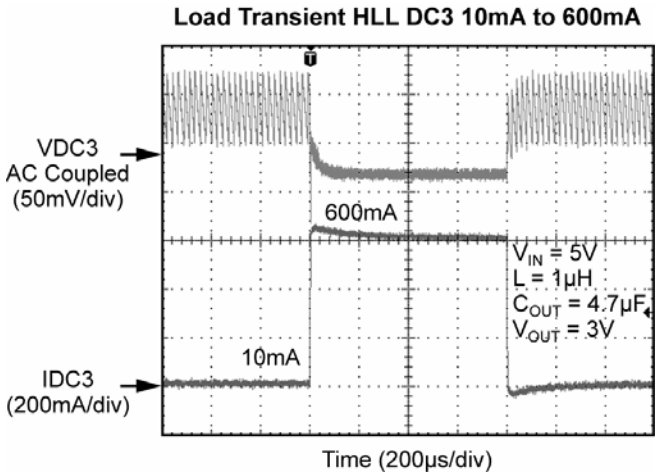
Load Transient HLL DC2 10mA to 300mA



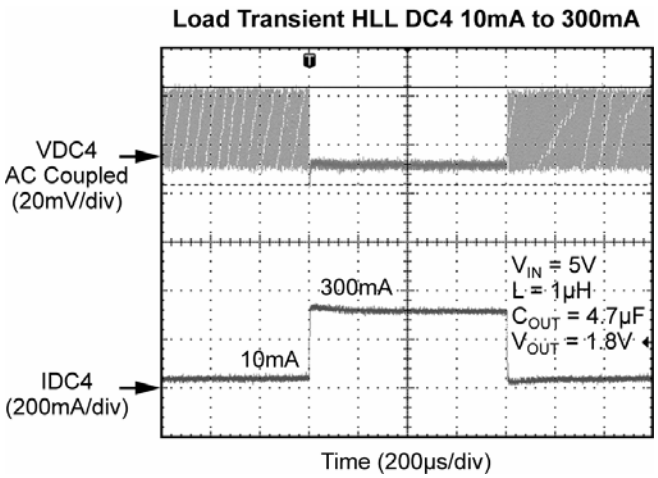
Load Transient HLL DC3 10mA to 300mA



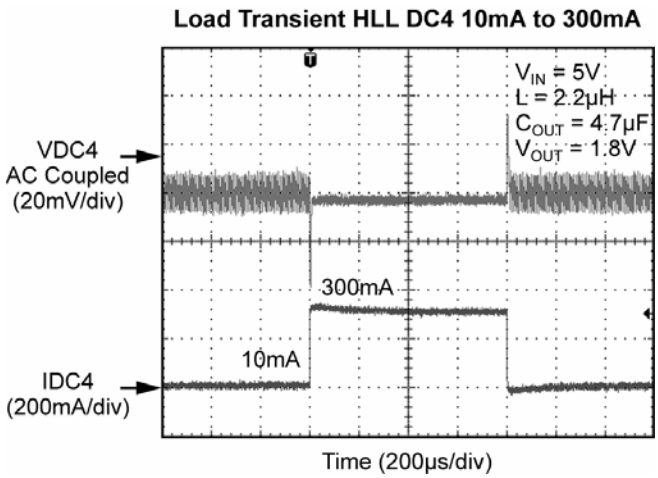
Load Transient HLL DC3 10mA to 600mA



Load Transient HLL DC4 10mA to 300mA

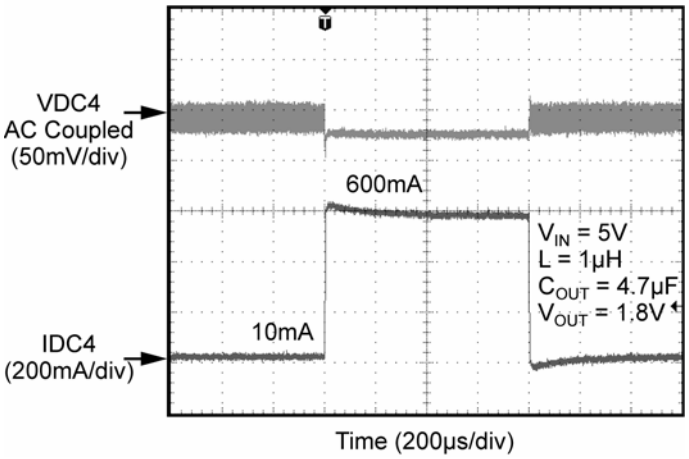


Load Transient HLL DC4 10mA to 300mA

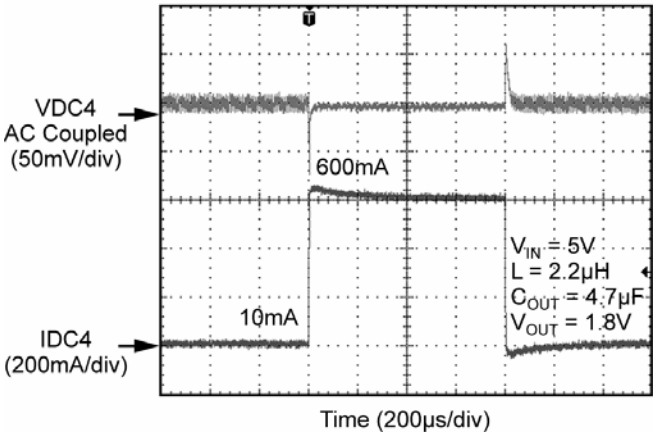


Functional Characteristics (Continued)

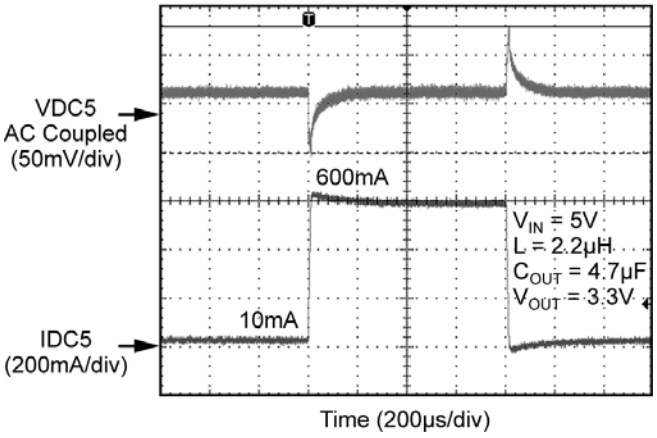
Load Transient HLL DC4 10mA to 600mA



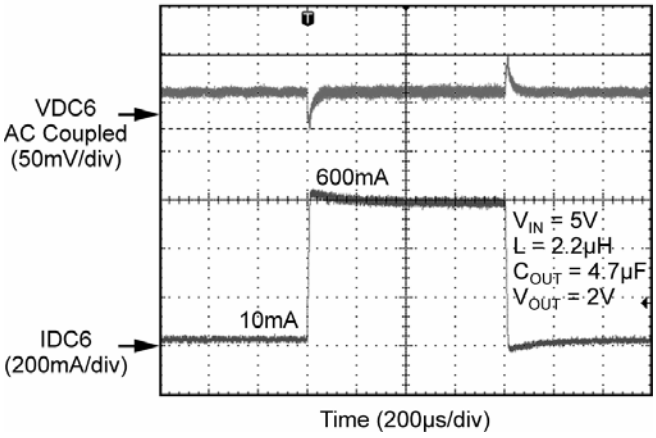
Load Transient HLL DC4 10mA to 600mA



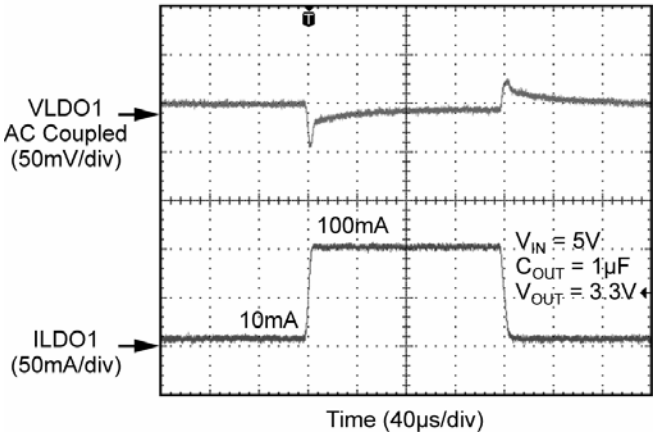
Load Transient PWM DC5 10mA to 600mA



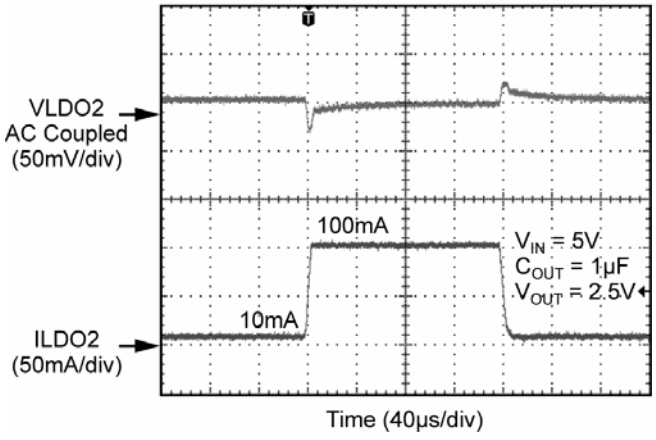
Load Transient PWM DC6 10mA to 600mA



LDO1 Load Transient 10mA to 100mA

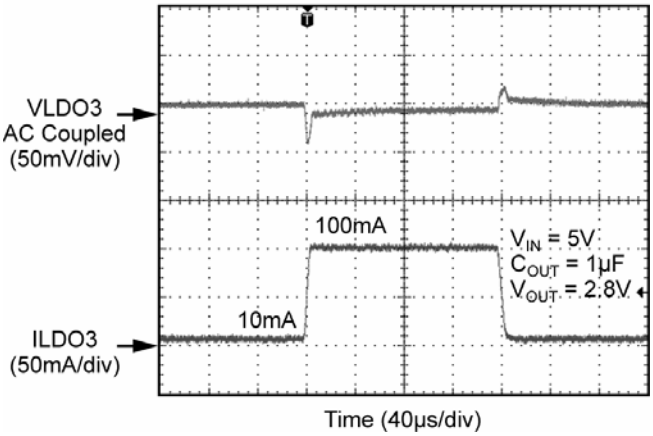


LDO2 Load Transient 10mA to 100mA

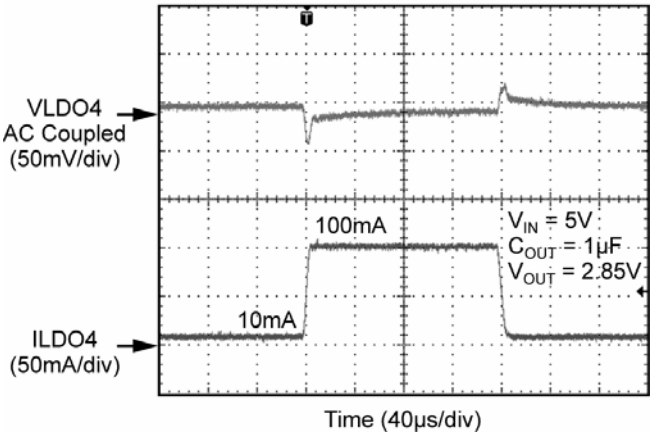


Functional Characteristics (Continued)

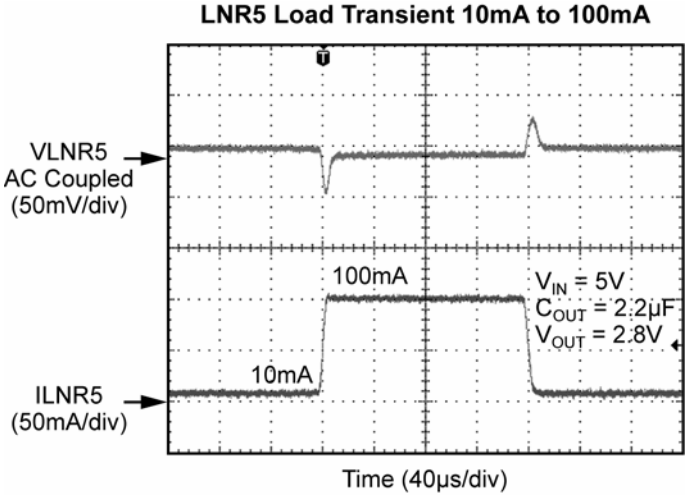
LDO3 Load Transient 10mA to 100mA



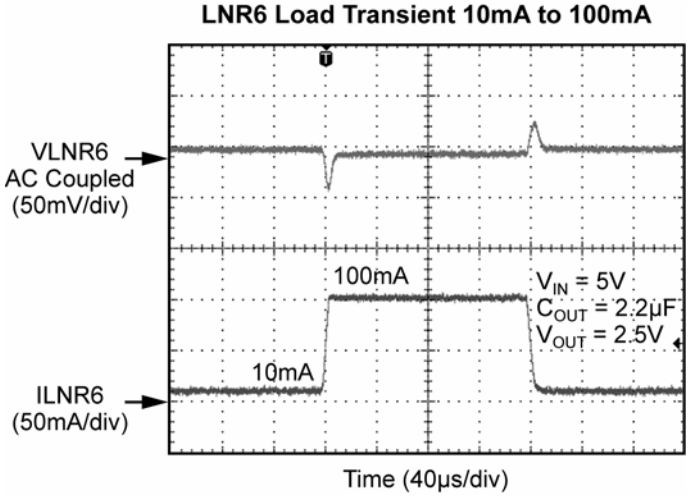
LDO4 Load Transient 10mA to 100mA



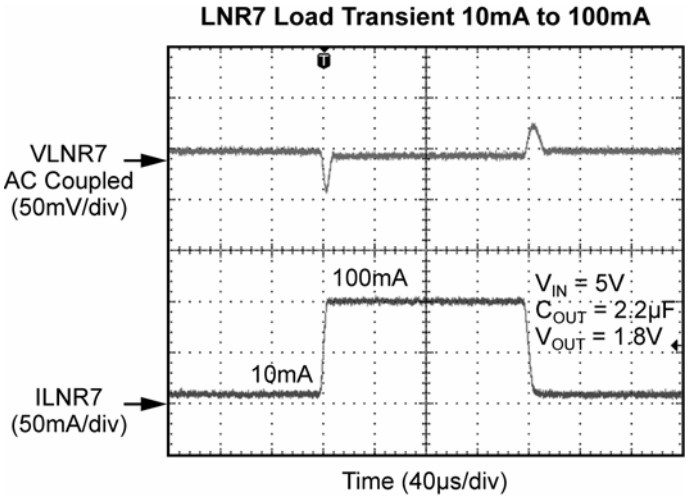
LNR5 Load Transient 10mA to 100mA



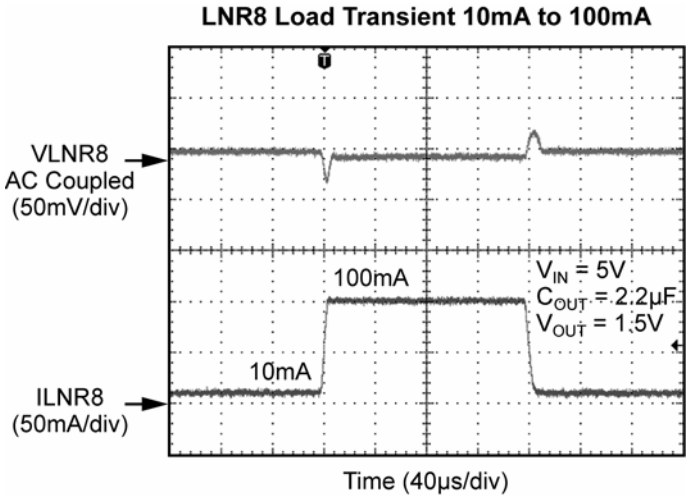
LNR6 Load Transient 10mA to 100mA



LNR7 Load Transient 10mA to 100mA

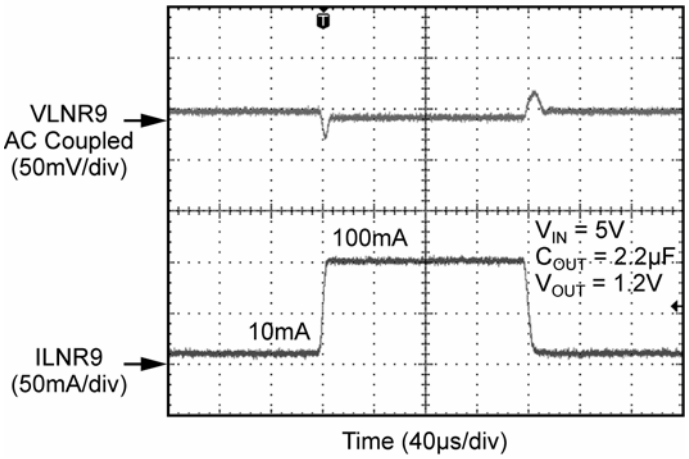


LNR8 Load Transient 10mA to 100mA

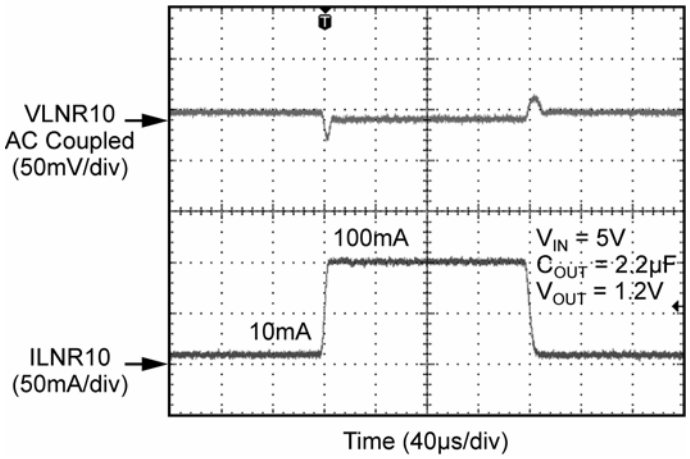


Functional Characteristics (Continued)

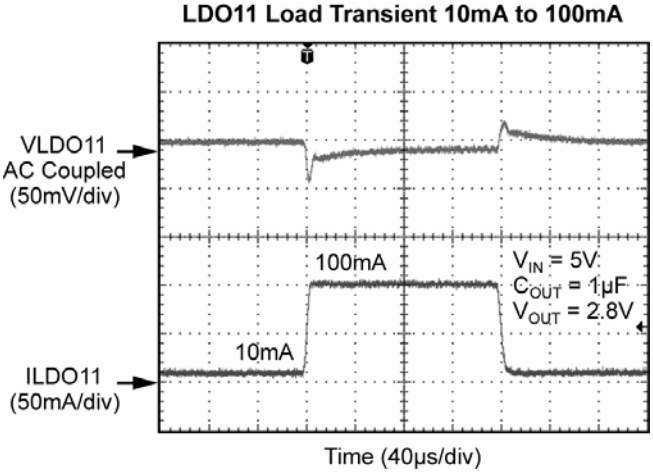
LNR9 Load Transient 10mA to 100mA



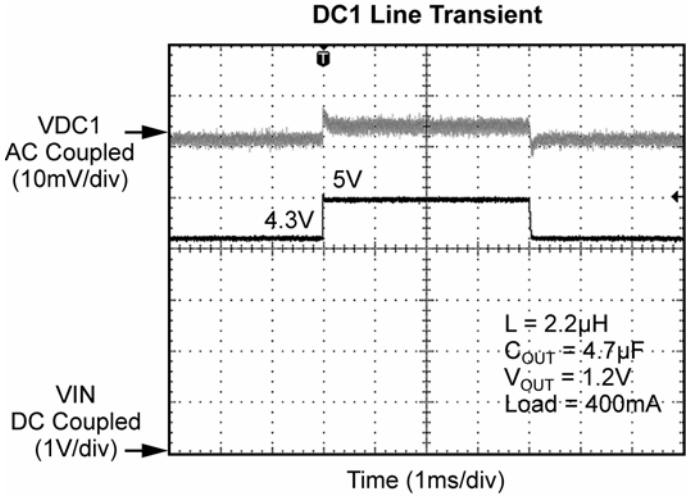
LNR10 Load Transient 10mA to 100mA



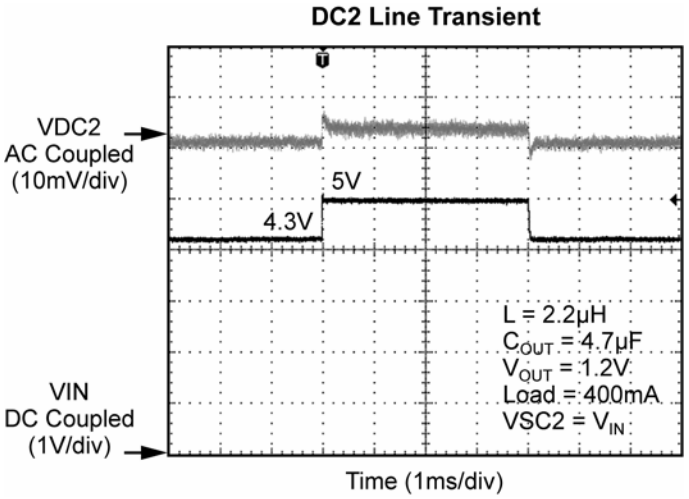
LDO11 Load Transient 10mA to 100mA



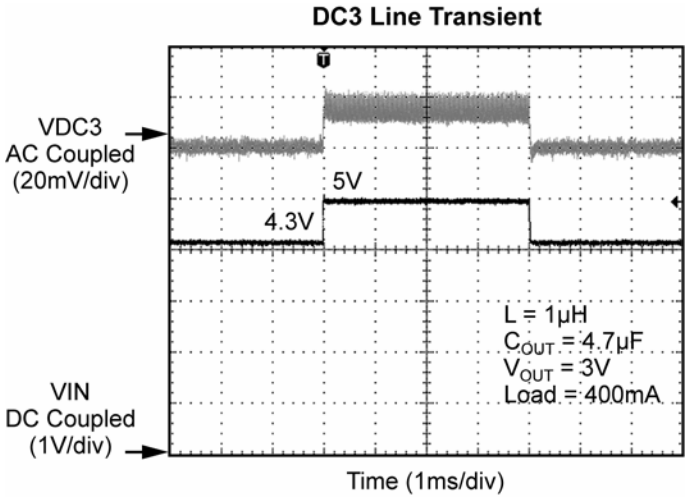
DC1 Line Transient



DC2 Line Transient

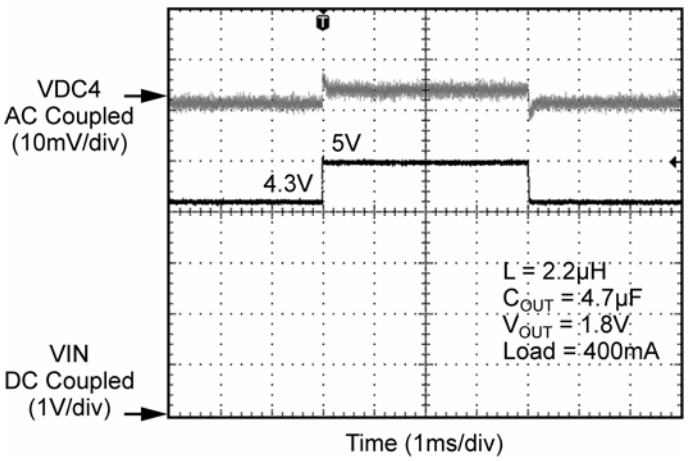


DC3 Line Transient

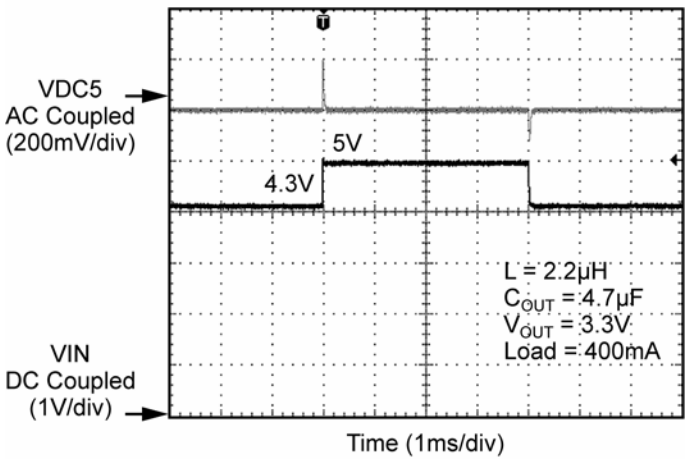


Functional Characteristics (Continued)

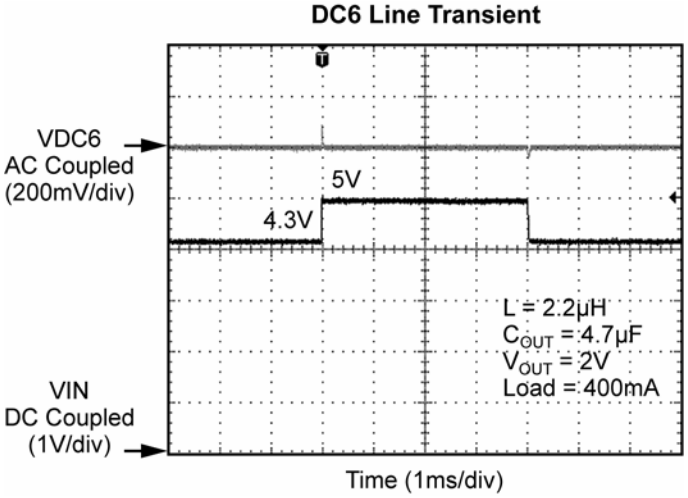
DC4 Line Transient



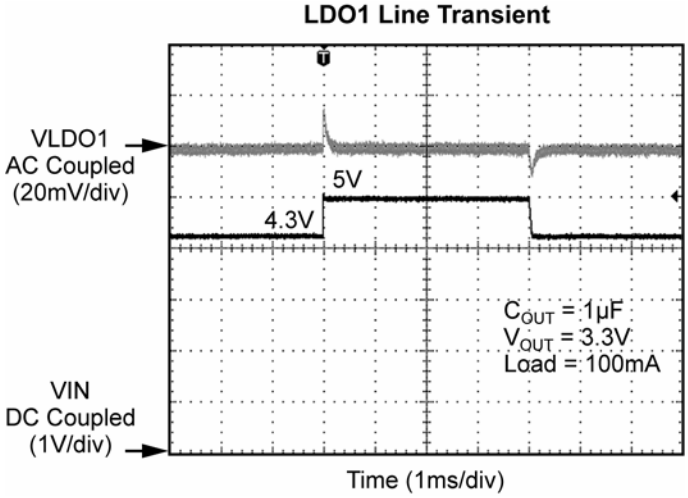
DC5 Line Transient



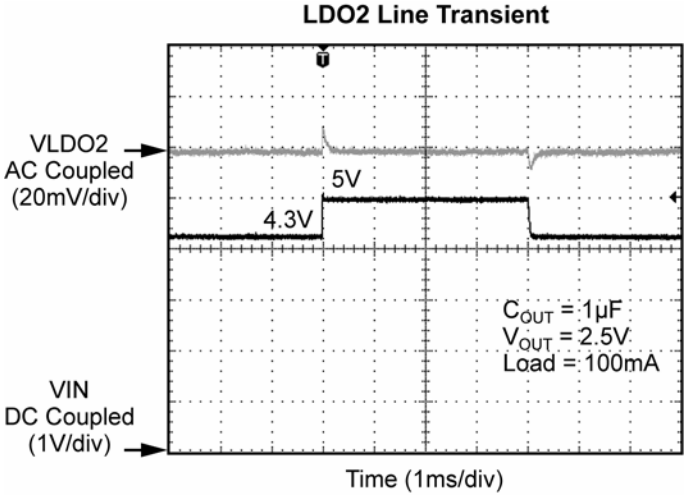
DC6 Line Transient



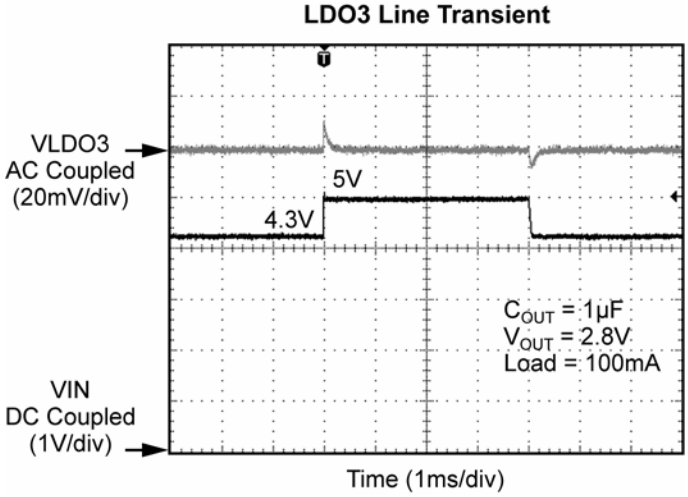
LDO1 Line Transient



LDO2 Line Transient

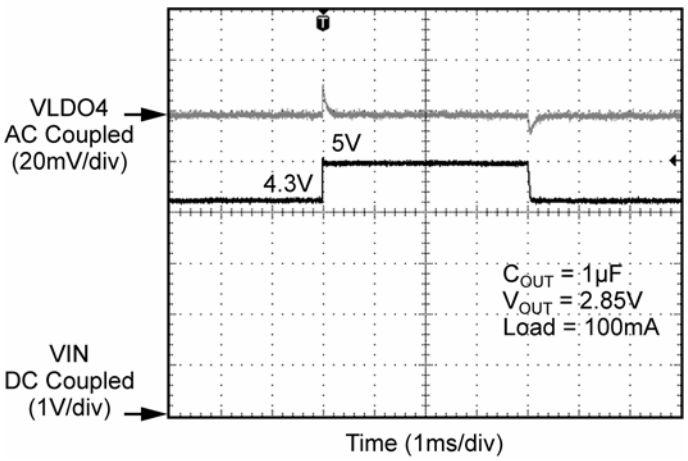


LDO3 Line Transient

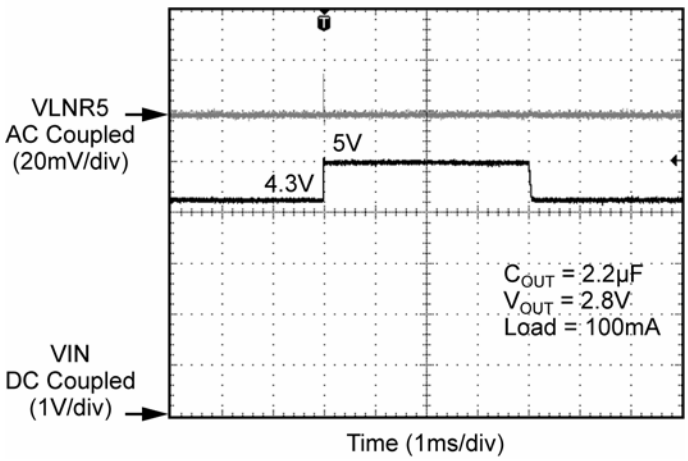


Functional Characteristics (Continued)

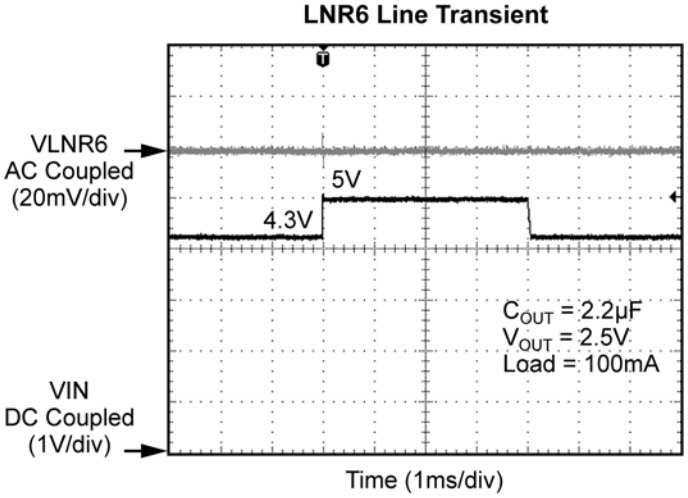
LDO4 Line Transient



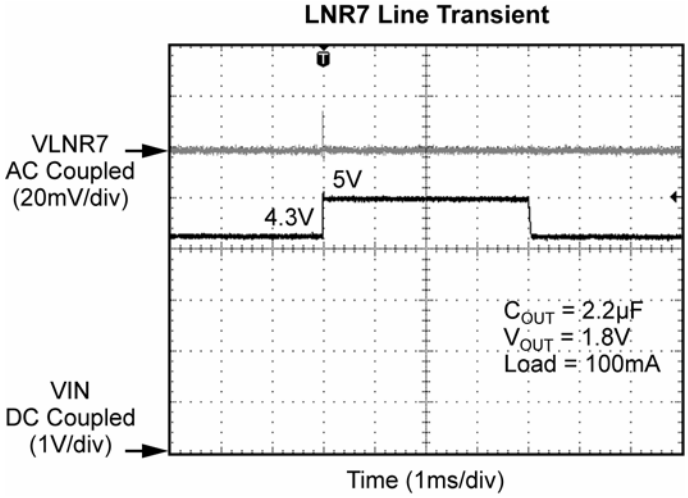
LNR5 Line Transient



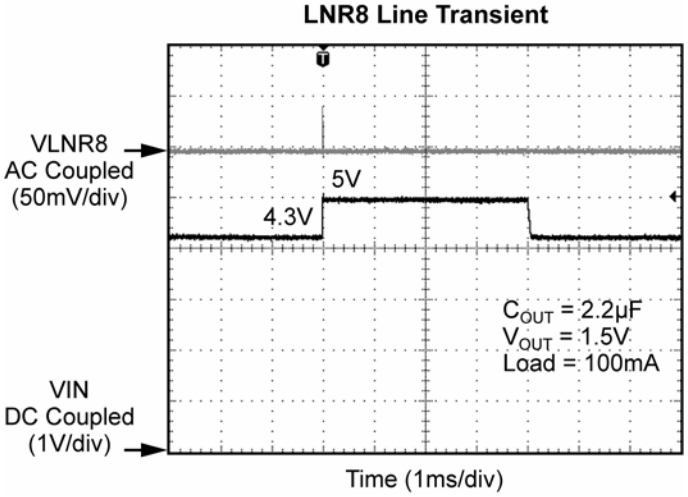
LNR6 Line Transient



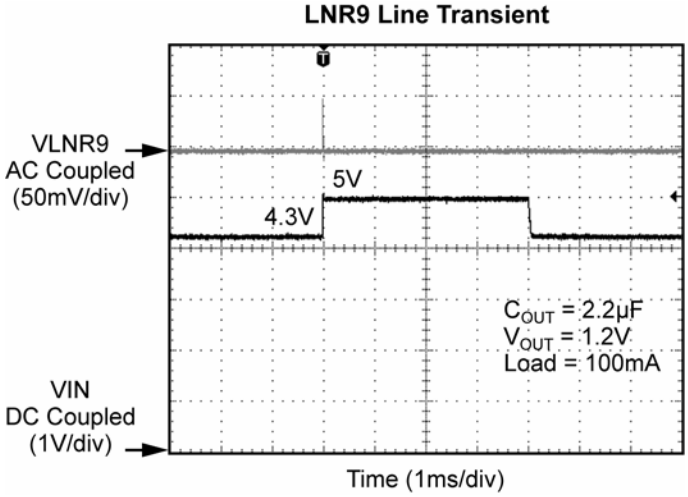
LNR7 Line Transient



LNR8 Line Transient

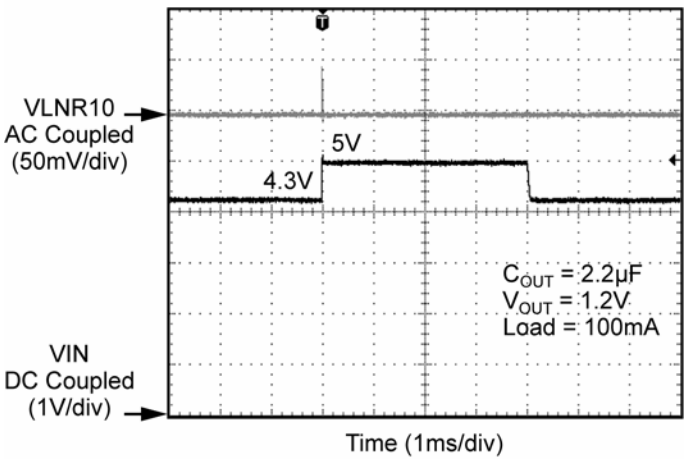


LNR9 Line Transient

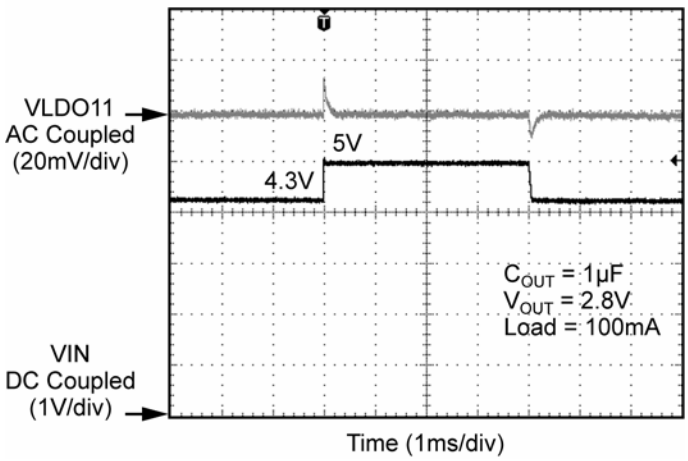


Functional Characteristics (Continued)

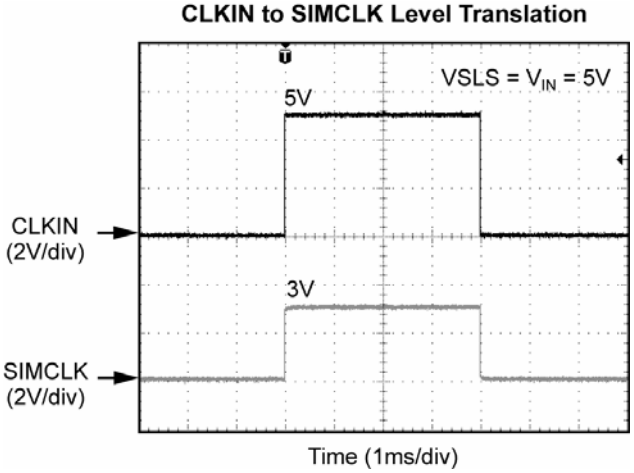
LNR10 Line Transient



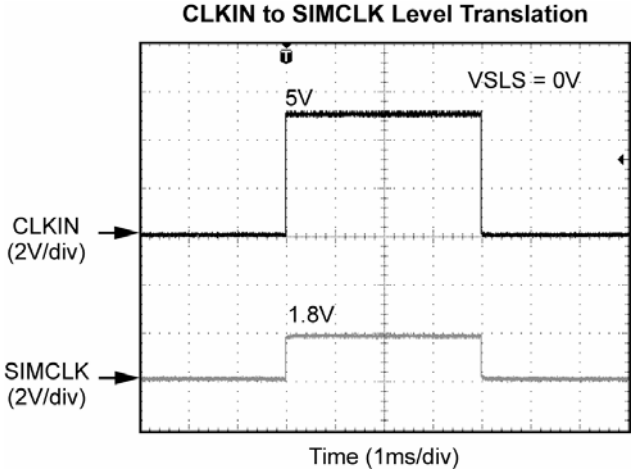
LDO11 Line Transient



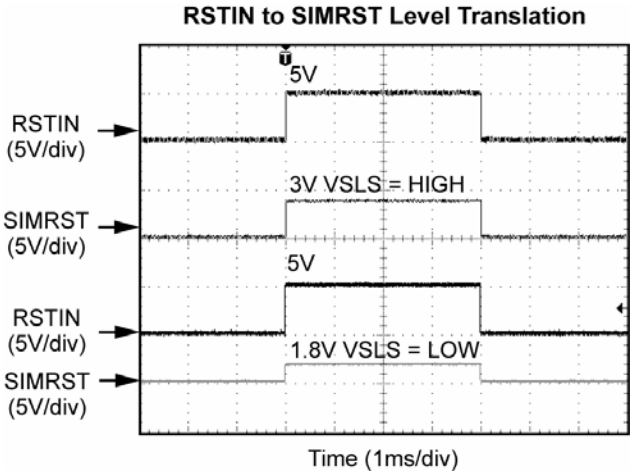
CLKIN to SIMCLK Level Translation



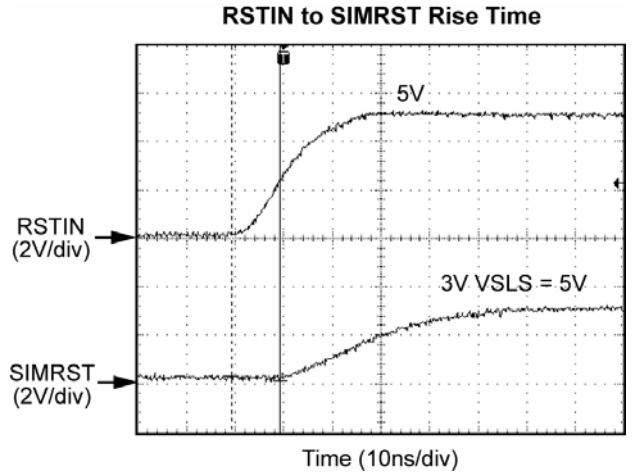
CLKIN to SIMCLK Level Translation



RSTIN to SIMRST Level Translation

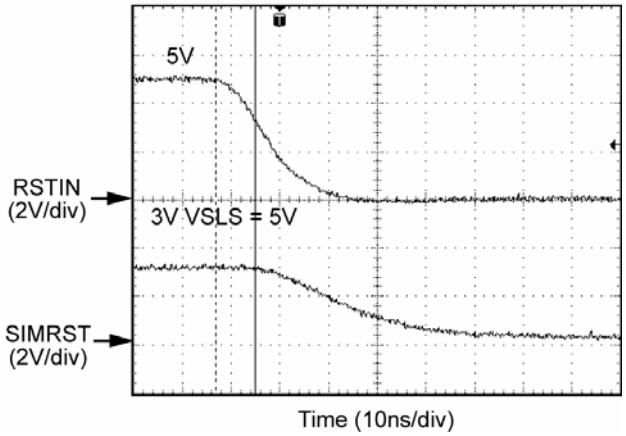


RSTIN to SIMRST Rise Time

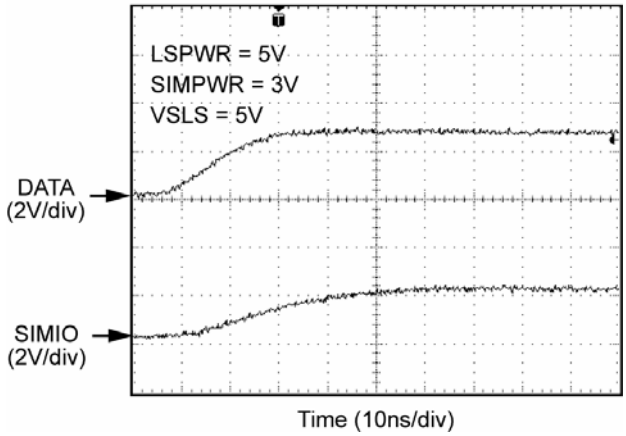


Functional Characteristics (Continued)

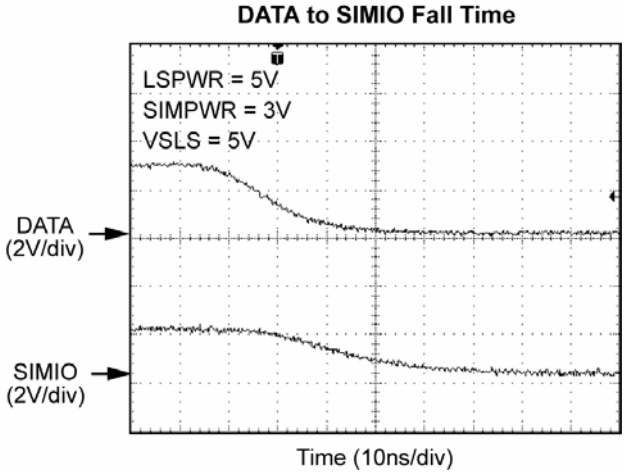
RSTIN to SIMRST Fall Time



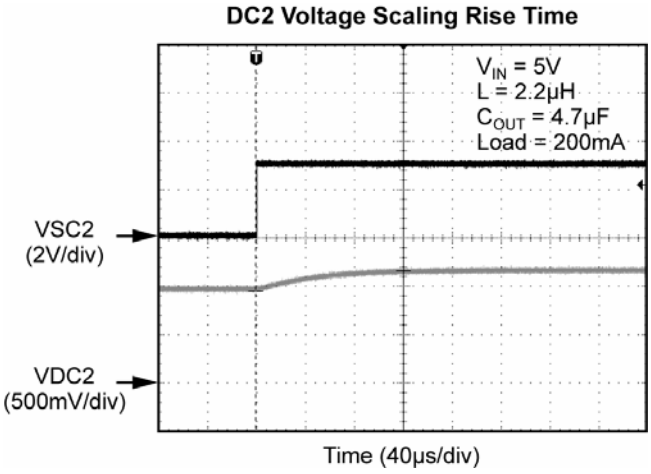
DATA to SIMIO Rise Time



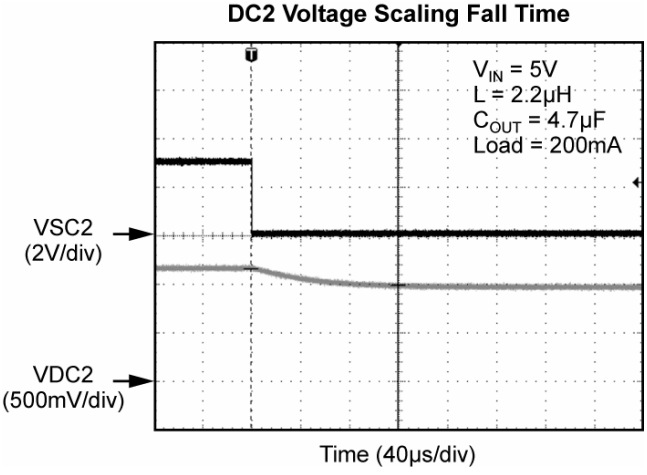
DATA to SIMIO Fall Time



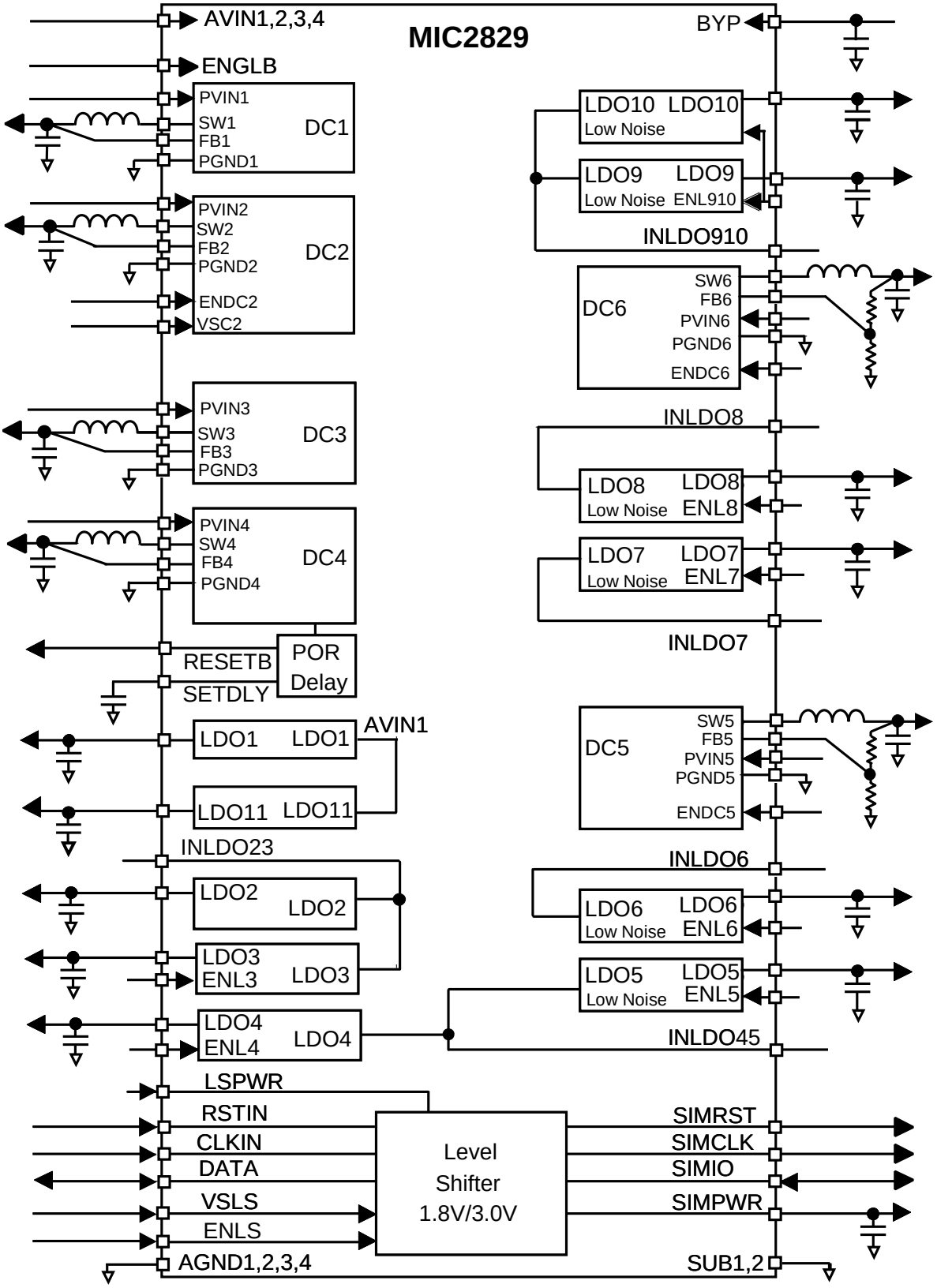
DC2 Voltage Scaling Rise Time



DC2 Voltage Scaling Fall Time



Functional Diagram



MIC2829 Simplified Block Diagram

Functional Description

AVIN1 and AVIN2

The input supply pins (AVIN1 and AVIN2) provide bias to the internal LDO circuitry and the input voltage to LDO1 and LDO11. The AVIN operating range is 2.7V to 5.5V so a minimum 1µF input capacitor with a 6.3V voltage rating placed as close to the AVIN and ground (AGND1 and AGND2) is required. Capacitance decreases as the DC bias across the capacitor increases and should be considered when selecting a suitable capacitor. AVIN1 and AVIN2 are internally connected. All AVINs should be tied together and connected to the PVINs of the device. Refer to the layout recommendations for details.

AVIN3 and AVIN4

The input supply pins (AVIN3 and AVIN4) provide bias to the internal circuitry for the switch mode regulators (DC1 through DC6) and power to SIMPWR. The AVIN operating range is 2.7V to 5.5V, so a minimum 1µF input capacitor with a minimum voltage rating of 6.3V placed close to AVIN and ground (AGND3 and AGND4) is required. AVIN3 and AVIN4 are internally connected. All AVINs should be tied together and connected to the PVINs of the device. Refer to the layout recommendations for details.

PVIN1 to PVIN6

The power input supply pins (PVIN1 to PVIN6) provide power to the switch mode regulators (DC1 to DC6). Due to high switching currents, a minimum 1µF input capacitor with a minimum voltage rating of 6.3V placed close to PVIN and the power ground is required. The PVIN tracks should be as wide as possible and the 1µF capacitor should be placed from PVIN1 to PGND1 due to the proximity of their pin location. The same should be done with each PVIN and PGND combination. All AVINs should be tied together and connected to the PVINs of the device. Refer to the layout recommendations for details.

AGND1 and AGND2

The ground pins (AGND1 and AGND2) are the ground path for the biasing, the control circuitry and the power ground for all LDOs. AGND1 and AGND2 are internally connected. The current loop for the ground should be kept as short as possible. Connect AGND1 and AGND2 together. Refer to the layout recommendations for more details.

AGND3 and AGND4

The analog ground pins (AGND3 and AGND4) are the ground path for the biasing and the control circuitry for all buck regulators. This is a low current ground path and should not be mixed with high current paths such as PGND. To reduce the effects of parasitic interference in the layout, AGND3 should be connected to the PGND plane near the PGND3 pin. Similarly, AGND4 should be connected to the PGND plane near the PGND4 pin. This allows the AGND3 and AGND4 ground voltage to be as close to the PGND ground voltage as possible. Should the AGND3 and AGND4 connect further from the PGND3 and PGND4 pins, then the effects of parasitic inductance and resistance would reduce the performance by altering the accuracy of ground. Refer to the layout recommendations for more details.

PGND1 to PGND6

The power ground pins (PGND1 to PGND6) are the ground path for the high current ground path for DC1 through DC6. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND3, AGND4) loop. All power grounds (PGND1 to PGND6) should be connected on the same plane. Refer to the layout recommendations for more details.

INLDO

The INLDO pins (INLDO23, INLDO45, INLDO6, INLDO7, INLDO8, and INLDO910) are the power input for the respective LDOs. Due to line inductance, a minimum of 1µF input capacitor with a minimum voltage rating of 6.3V should be placed as close as possible to the INLDO pin and ground (AGND1, AGND2). Refer to the layout recommendations for more details.

LDO

The LDO pins (LDO1 to LDO11) are the output of the LDO and LNR regulators. For LDO1, LDO2, LDO3, LDO4 and LDO11, a minimum of 1µF output capacitor with a minimum voltage rating of 6.3V placed as close to the LDO pin and ground (AGND1 and AGND2) as possible is required. For the LNRs (LDO5 to LDO10), a 2.2µF output capacitor with a minimum voltage rating of 6.3V placed as close as possible to the LDO pin and ground (AGND1 and AGND2) is recommended. Refer to the layout recommendations for more details.

BYP

The reference bypass pin (BYP) acts as a filter for the reference voltage of LNR5 to LNR10. A 0.1µF bypass capacitor connected to ground (AGND1 and AGND2) is recommended.

SUB

The SUB pin (SUB1, SUB2) is connected internally to the guard ring ground protection. The guard ring prevents interaction between regulators inside the die package. Connect SUB1 and SUB2 pins to ground (AGND1, AGND2) externally.

ENGLB

The global enable pin (ENGLB) must be pulled high in order for the MIC2829 to function. When ENGLB is pulled high, a startup sequence begins. The regulators DC1, DC3, DC4/LDO2, LDO1/LDO11 turn on in sequence. See Turn-ON Sequence Flow Chart in Figure 1.

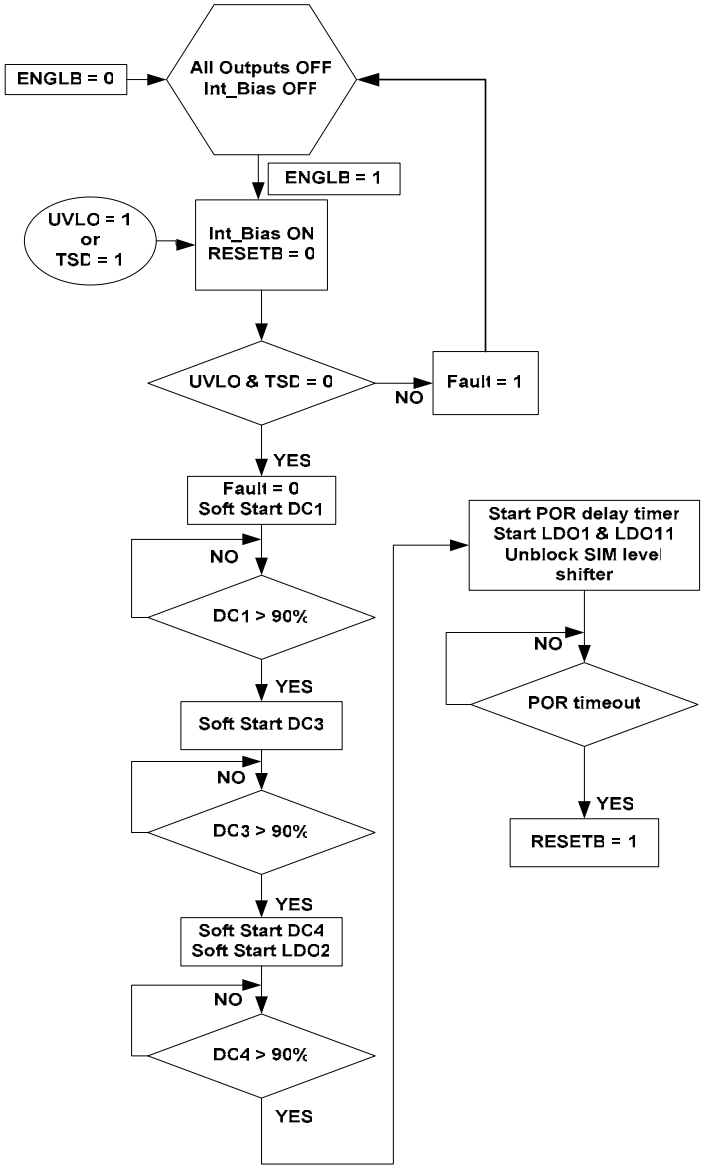


Figure 1. Turn-ON Sequence Flow Chart

ENDC

ENGLB needs to be high in order for any other enables to function. A logic high signal on the enable pin (ENDC2, ENDC5, ENDC6) activates the output voltage of its respective buck regulator shown in Table 1. A logic low signal on the enable pin deactivates the output of the buck regulator. Do not leave floating, as it would leave the regulator in an unknown state.

ENDC	HIGH (>1.1V)	LOW (<0.2V)
ENDC2	DC2 ON	DC2 OFF
ENDC5	DC5 ON	DC5 OFF
ENDC6	DC6 ON	DC6 OFF

Table 1. Buck Regulator Enable

ENL

ENGLB needs to be high in order for any other enables to function. A logic high signal on the enable pin (ENL3 to ENL8, ENL910) activates the output voltage of LDO3, LDO4 and LNR5 to LNR10 as shown in Table 2. A logic low signal on the enable pin deactivates the output of the respective LDO. Do not leave floating, as it would leave the regulator in an unknown state.

ENL	HIGH (>1.1V)	LOW (<0.2V)
ENL3	LDO3 ON	LDO3 OFF
ENL4	LDO4 ON	LDO4 OFF
ENL5	LNR5 ON	LNR5 OFF
ENL6	LNR6 ON	LNR6 OFF
ENL7	LNR7 ON	LNR7 OFF
ENL8	LNR8 ON	LNR8 OFF
ENL910	LNR9, LNR10 ON	LNR9, LNR10 OFF

Table 2. LDO Regulator Enable

SETDLY

If the output voltage of DC4 is greater than 90% of nominal, the Power On Reset (POR) delay circuit begins to source a current to the set-delay pin (SETDLY). The SETDLY pin is used to adjust the delay time of the RESETB flag. A capacitor may be placed from SETDLY to ground (AGND1, AGND2) to adjust the delay time at a rate of 1 second/µF.

RESETB

The RESETB is an open drain output and can, for instance, be tied to the output of DC4 through a 100k resistor. When DC4 output voltage is greater than 96%, then the RESETB voltage will be pulled high after a delay set by the capacitor on the SETDLY pin. A capacitor at the SETDLY pin will delay the RESETB flag at a rate of 1 second / µF. When the output of DC4 is below 90%, RESETB is pulled low.

FB1 to FB4

The feedback pin (FB1 to FB4) is connected to the output of the HyperLight Load™ circuit to provide feedback to the control circuitry. The FB connection should be connected close to the output capacitor. Refer to the layout recommendations for more details.

FB5 and FB6

The feedback pin (FB5, FB6) allows DC5 and DC6 output voltage to be set by applying an external resistor network. The internal reference voltage is 1V and the recommended value of R_{BOTTOM} is 20kΩ or below. A feed-forward capacitor (C_{FF}) of 120pF should be placed parallel to R_{TOP} to improve stability and transient response. This does not impact the output voltage setting. The output voltage is calculated from the equation below.

$$V_{OUT} = 1V\left(\frac{R_{TOP}}{20k\Omega} + 1\right)$$

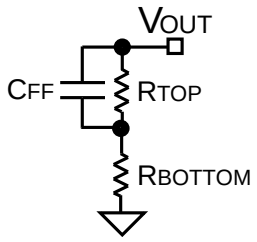


Figure 2. Feedback Resistor Network

SW

The switch pin (SW1 to SW6) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the output of the buck regulator. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes whenever possible.

VSC2

The voltage scaling pin (VSC2) is used to switch the output of DC2 between two different voltage levels. A high on the VSC2 pin will set the output voltage of DC2 to the higher voltage. A low on the VSC2 pin will set the output voltage to the lower voltage. Do not leave floating.

LSPWR

The level shifter input supply pin (LSPWR) provides power to the level shifter. A minimum 1µF input capacitor with a minimum voltage rating of 6.3V placed close to LSPWR and ground (AGND1, AGND2) is required. Refer to the layout recommendations for details.

SIMPWR

SIM power (SIMPWR) provides power to the SIM Card. A minimum 1µF input capacitor with a minimum voltage rating of 6.3V to ground (AGND1, AGND2) is required. Refer to the layout recommendations for details.

VSLS

VSLS selects the level shifted voltage for the SIM Card. A high logic voltage on VSLS selects the level shifter to 3V. A low logic voltage on VSLS selects the level shifter to 1.8V. Do not leave floating.

RSTIN, SIMRST

RSTIN is the digital reset input for the SIM Card and translates to SIMRST through the digital level shifter. It is one directional. If VSLS is low, then the input at RSTIN will be level shifted to 1.8V at the SIMRST output. If VSLS is high, then the input at RSTIN will be level shifted to 3V at the SIMRST output.

CLKIN, SIMCLK

CLKIN is the digital input clock for SIM card. The CLKIN translates to SIMCLK and is one directional. If VSLS is low, then the input at CLKIN will be level shifted to 1.8V at the SIMCLK output. If VSLS is high, then the input at CLKIN will be level shifted to 3V at the SIMCLK output.

DATA, SIMIO

DATA is the digital data for the SIM Card. The DATA translate to SIMIO through the digital level shifter and is bi-directional using internal pull ups. If VSLS is low, then the level shifted output is 1.8V at the SIMIO output. If VSLS is high, then the level shifted output is 3V at the SIMIO output. Since DATA and SIMIO are bi-directional, the input at SIMIO is level shifted to equal the LSPWR voltage at the DATA output.

G1 – G9

The G1 through G9 pins are not internally connected. They serve as thermal relief and should be connected to ground (AGND1, AGND2) to maximize the heat dissipation. See layout recommendations for details.

Application Information

The MIC2829 is a Power Management Integrated Circuit (PMIC) designed for 3G/4G (HEDGE/LTE or WiMAX) modules. It incorporates six buck converters, eleven LDOs and a SIM card level translator in a 5.5mm x 5.5mm package designed to support 3G/4G (HEDGE/LTE or WiMAX) wireless modems. A typical power source for the MIC2829 can be from a USB host or a single cell lithium ion battery.

The MIC2829 has six integrated step-down regulators. Four of the six integrated step-down converters incorporate HyperLight Load™ (HLL) technology. The DC1, DC2, and DC4 operate at 4MHz switching frequency range and can support 1A, 300mA and 600mA respectively. DC3 operates at 2.5MHz and can support up to 600mA.

DC5 and DC6 operate at a 2MHz switching frequency, can support 100% duty cycle operation and can maintain 800mA on each output. They both have adjustable output voltages using external resistors.

The MIC2829 has eleven low dropout regulators (LDOs). Five general purpose LDOs (LDO1 to LDO4, LDO11) have low dropout, output accuracy of ±3% and drawing 40µA of ground current. The other six are high performance LNRs (LNR5-LNR10) with a PSRR of over 70dB at 1kHz and 20µVrms Output Noise. The LNRs require just 20µA to operate.

The MIC2829 also has three level shifters and a 50mA power supply for digital SIM Card signal translations.

Input Capacitor

The MIC2829 has many input pins that are externally connected. A 1µF ceramic capacitor or greater should be placed close to the power input pin and ground. The following chart indicates the minimum capacitance needed for each input pin and their ideal grounding points.

Pin Name	Capacitance	Ideal Ground
AVIN1	1 µF	AGND1
AVIN2	1 µF	AGND2
AVIN3	1 µF	AGND3
AVIN4	1 µF	AGND4
INLDO23	1 µF	AGND1 or AGND2
INLDO45	1 µF	AGND1 or AGND2
INLDO6	1 µF	AGND1 or AGND2
INLDO7	1 µF	AGND1 or AGND2
INLDO8	1 µF	AGND1 or AGND2
INLDO910	1 µF	AGND1 or AGND2
LSPWR	1 µF	AGND1 or AGND2
PVIN1	1 µF	PGND1
PVIN2	1 µF	PGND2
PVIN3	1 µF	PGND3
PVIN4	1 µF	PGND4
PVIN5	1 µF	PGND5
PVIN6	1 µF	PGND6

Table 3. Recommended Input Capacitance

A case size 0402, 1µF ceramic capacitor (Samsung CL05A105KP5NNN) is recommended based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

Output Capacitor

The buck regulators (DC1 to DC6) are designed for use with a 4.7µF or greater ceramic output capacitor. A case size 0402, 4.7µF ceramic capacitor (Samsung, CL05A475MQ5NRN) is recommended based upon performance, size and cost. A case size 0402, 1µF ceramic capacitor (Samsung, CL05A105KP5NNN) is recommended for each LDO (LDO1 to LDO4, LDO11, and SIMPWR) output. Each LNR (LNR5 to LNR10) is designed for low noise operation; therefore, a case size 0402, 2.2µF ceramic capacitor (Samsung, CL05A225MP5NSN) is recommended. Table 4 below indicates the recommended capacitance needed for each output and their ideal grounding points.

Output	Capacitance	Ideal Ground
LDO1	1 µF	AGND1 or AGND2
LDO2	1 µF	AGND1 or AGND2
LDO3	1 µF	AGND1 or AGND2
LDO4	1 µF	AGND1 or AGND2
LDO5	2.2 µF	AGND1 or AGND2
LDO6	2.2 µF	AGND1 or AGND2
LDO7	2.2 µF	AGND1 or AGND2
LDO8	2.2 µF	AGND1 or AGND2
LDO9	2.2 µF	AGND1 or AGND2
LDO10	2.2 µF	AGND1 or AGND2
LDO11	1 µF	AGND1 or AGND2
SIMPWR	1 µF	AGND1 or AGND2
DC1	4.7 µF	PGND1
DC2	4.7 µF	PGND2
DC3	4.7 µF	PGND3
DC4	4.7 µF	PGND4
DC5	4.7 µF	PGND5
DC6	4.7 µF	PGND6

Table 4. Recommended Output Capacitance

Although all grounds eventually connect externally, it is important to place the capacitors close to their ideal ground for the load to minimize parasitic inductance and resistance. This is especially important for a PMIC with multiple regulators. Increasing the output capacitance will lower output ripple and improve load transient response, but could increase solution size or cost. Both the X7R or X5R temperature rated capacitors are recommended. The Y5V and Z5U temperature rated capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies.

Inductor Selection

When selecting an inductor, it is important to consider the following factors (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC2829 was designed for use with an inductance range from 1µH to 2.2µH. Typically, a 2.2µH inductor is recommended for a balance of transient response, efficiency and output ripple. For faster transient response, a 1µH inductor will yield the best result. For lower output ripple, a 2.2µH inductor is recommended. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as follows:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right]$$

As shown by the calculation above, the peak inductor current is inversely proportional to the switching frequency (f) and the inductance (L); the lower the switching frequency or the inductance the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application Circuit and Bill of Materials for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$Efficiency\ \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time which is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET R_{DSON} multiplied by the Switch Current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required for driving the gates on and off at the constant switching frequency and other internal switching transitions make up the switching losses.

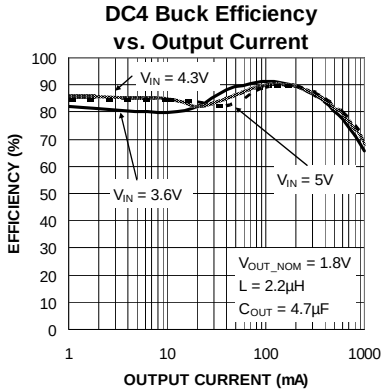


Figure 3. HLL Efficiency vs. Output Current

Figure 3 shows an efficiency curve. From an output current of 1mA to 100mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By lowering the switching frequency, the HyperLight Load™ buck regulator (DC1 to DC4) is able to maintain high efficiency at low output currents.

Over 100mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the Gate-to-Source overdrive on the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing conduction losses in the device. All but the inductor losses are inherent to the device. For higher current levels, inductor selection

becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$P_{L\_LOSS} \approx I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$Efficiency\ Loss \approx \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{L\_LOSS}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Partitioning for Optimal System Efficiency

Many of the LDOs can be post-regulated from the DC regulator output to increase system efficiency. For example, DC4 output can be used to power low output voltage LNRs in order to reduce power loss during voltage conversion.

Thermal Considerations

Whenever there is power dissipation, there will be thermal considerations. In order to account for the temperature rise in a PMIC with multiple regulators, the power dissipation in each regulator must be accounted for. The current rating of each regulator is shown below:

Output	Maximum Load (mA)
DC1	1000
DC2	300
DC3	600
DC4	600
DC5	800
DC6	800
LDO1	200
LDO2	200
LDO3	200
LDO4	200
LDO5	200
LDO6	200
LDO7	200
LDO8	200
LDO9	200
LDO10	200
LDO11	200
SIMPWR	50

Table 5. Output Current Rating

If each regulator on the MIC2829 is turned on at its maximum load capability, the power dissipation into the device will cause excessive temperature rise. In order to avoid excessive temperature rise and unexpected thermal shutdown the total power dissipation should be considered.

LDO Power Dissipation

The power dissipation of a LDO can be calculated with the input voltage, the output voltage and the output current, as shown in the following equation.

$$P_{D\_LDO} \approx (V_{IN} - V_{OUT})\ I_{OUT} + V_{IN}\ I_{GND}$$

Since the ground current (I_{GND}) is relatively low, it can be ignored for this calculation. For example, if the input voltage is 3.3V, the output voltage is 2.8V and the output current of the LDO is 200mA, the power dissipation of the LDO can be calculated as follow:

$$P_{D\_LDO} \approx (3.3V - 2.8V) \times 200mA$$

$$P_{D\_LDO} \approx 0.1W$$

Buck Regulator Power Dissipation

Neglecting some minor losses, the power dissipation in a MIC2829 buck regulator (DC1 to DC6) is approximately the switcher's input power minus the switcher's output power and minus the power loss in the inductor.

$$P_{D\_SWITCHER} \approx P_{IN}\ x\ I_{IN} - P_{OUT}\ x\ I_{OUT} - P_{L\_LOSS}$$

Total Power Dissipation

The total power dissipation in the MIC2829 package is equal to the sum of the power loss of each regulator.

$$P_{D\_TOTAL} \approx SUM\ (P_{D\_LDOS} + P_{D\_SWITCHERS})$$

The maximum power dissipation of the package can be calculated by the following equation.

$$P_{D(\max)} \approx \left(\frac{T_{J(\max)} - T_A}{\theta_{JA}}\right)$$

$T_{J(MAX)}$ is the maximum junction temperature (125°C), T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the package (38.7°C/W).

The following table shows the maximum power dissipation versus the ambient temperature.

$P_{D(MAX)}$ (W)	T_A (°C)
4.26	-40
3.75	-20
3.23	0
2.71	20
2.20	40
1.68	60
1.16	80
0.65	100
0.13	120

Table 6. Maximum Power Dissipation

It is good practice to not exceed the maximum power dissipation of the device in order to avoid excessive temperature rise or unexpected thermal shutdown.

HyperLight Load™ Mode

The HyperLight Load™ (HLL) buck regulators on the MIC2829 use a proprietary control loop (patented by Micrel). It has two modes of operation (HLL mode and PWM mode).

The transition from HLL mode to PWM mode is determined by the inductor ripple current. If the inductor ripple current reaches below zero it is considered to be in discontinuous mode (DCM). The HLL control loop will control the switching in DCM using pulse frequency modulation (PFM). As the load pulls the output voltage below the monitored threshold, the HLL control loop turns on the topside PMOS transistor for a predetermined time until the output voltage rises above the monitored threshold. Once the upper threshold is reached, the topside PMOS is switched off and the voltage will then be slowly pulled down by the load. As the load increases, the switching frequency increases. By varying the switching frequency, the regulator only switches when needed which improves efficiency by reducing switching losses.

As the load increases and the inductor ripple current rises above zero, the HLL regulator switches into continuous conduction mode (CCM). The equation to calculate the load when the HLL regulator goes into continuous conduction mode may be approximated by the following formula:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f} \right)$$

As shown in the equation, the load at which HLL regulators transitions from HyperLight Load™ mode to PWM mode is a function of the input voltage (V_{IN}), the output voltage (V_{OUT}), the duty cycle (D), the inductance (L) and the switching frequency (f). Note that the duty cycle is approximately V_{OUT} divided by V_{IN} for buck converters. The following graph shows the HLL regulator switching frequency versus the output current. Since the inductance range of MIC2829 is from 1µH to 2.2µH, the device may then be tailored to enter HyperLight Load™ mode or PWM mode at a specific load current by selecting the appropriate inductance. For example, in Figure 4, when the inductance is 2.2µH the HLL regulator will transition into PWM mode at a load of approximately 30mA. Under the same condition, if 1µH inductance is used, the MIC2829 will transition into PWM mode at approximately 100mA.

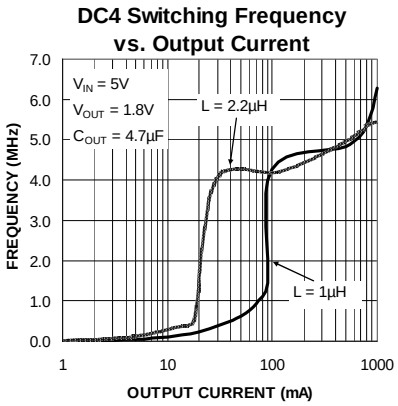
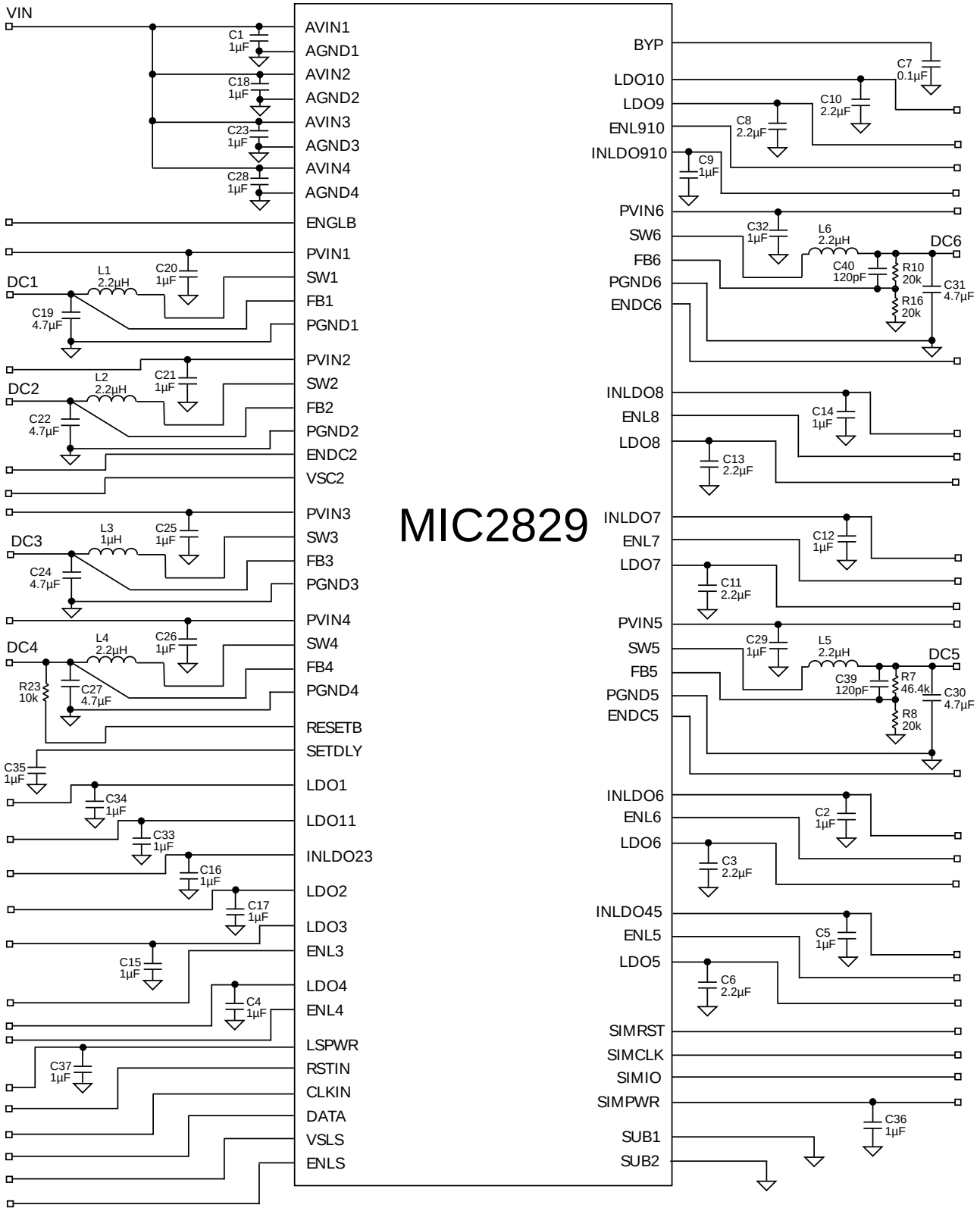


Figure 4. Switching Frequency with Various Inductance

In CCM, the HLL regulator works in pulse width modulation (PWM) by controlling the PMOS transistor off-time. To regulate the output voltage, the PMOS transistor off-time is controlled. As the output voltage decreases, the PMOS transistor off-time is decreased. As the output voltage increases, the off-time is increased. This method of controlling the off-time achieves the same goal as controlling the on-time as in other PWM regulators by increasing or decreasing the duty cycle of the PMOS transistor. In CCM, the synchronous switching between the PMOS and the NMOS is modulated at 4MHz for DC1, DC2 and DC4. Due to the higher output voltage of DC3 (3V), the switching frequency in CCM is at 2.5MHz. The HLL regulators may reach the minimum-off-time limit at lower input voltage and higher load currents. In order to regulate at such high duty cycles, the HLL regulator transitions into the on-time control scheme. During the on-time control scheme, the off-time is set constant at around (65ns), and the on-time is increased to deliver more energy. By doing so, the duty cycle is increased, and the output voltage maintains regulation even at lower input voltages and extreme load situations. As a result of increasing the on-time and fixing the off-time, the switching frequency is lowered. In CCM, the switching frequency is relatively constant, but at higher output voltage and output current levels, the control may transition into on-time control to regulate the output and thus, lower the switching frequency.

Typical Application Circuit



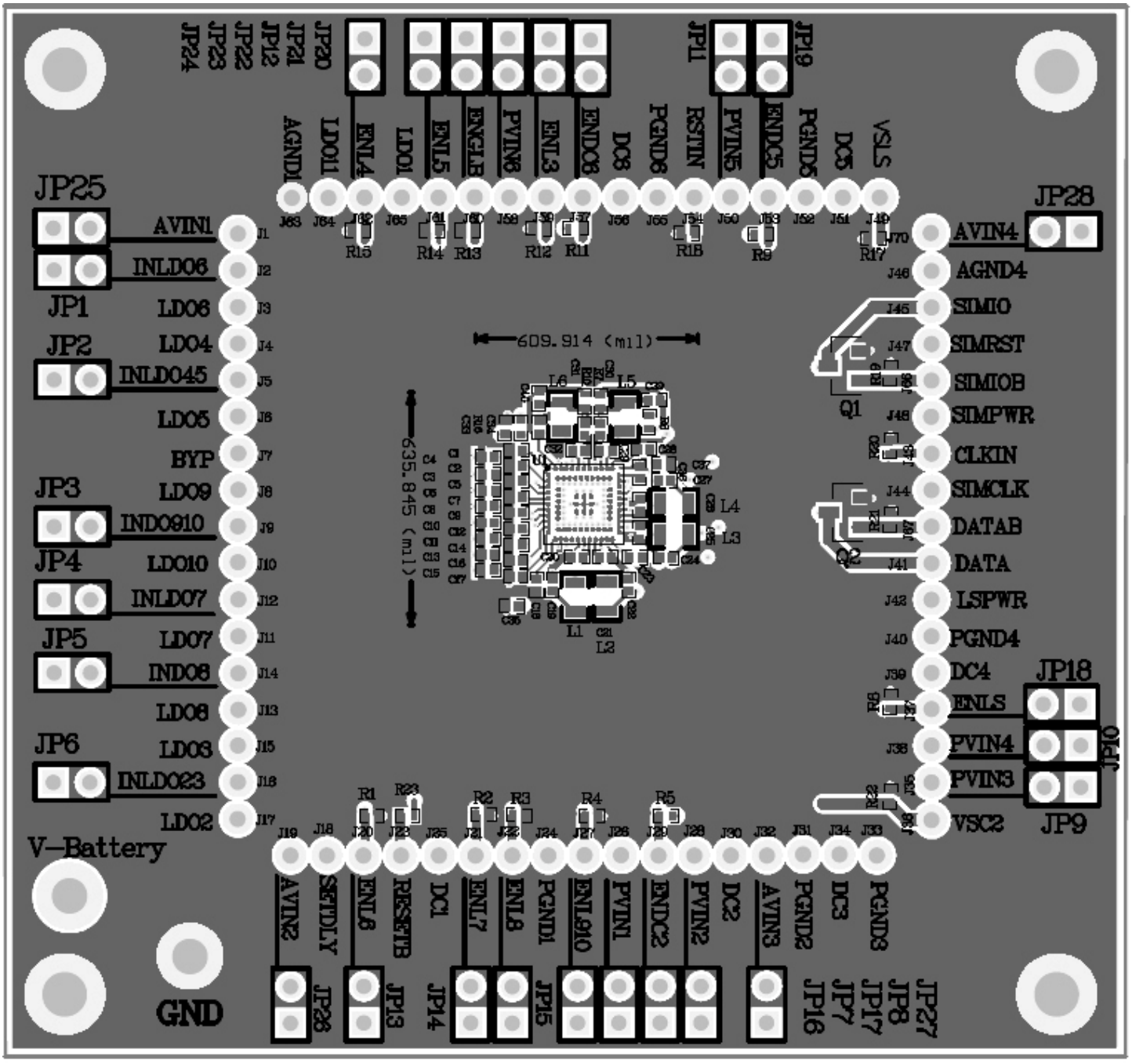
Bill of Material

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C4, C9, C14 – C18, C20, C21, C23, C25, C26, C28, C29, C32 – C37	CL05A105KP5NNN	Samsung(1)	1.0µF Ceramic Capacitor, 10V, X5R, Size 0402	22
C3, C5, C6, C8, C10 – C13	CL05A225MP5NSN	Samsung	2.2µF Ceramic Capacitor, 10V, X5R, Size 0402	8
C19, C22, C24, C27, C30, C31	CL05A475MQ5NRN	Samsung	4.7µF Ceramic Capacitor, 6.3V, X5R, Size 0402	6
C7	CL05B104K05NNNC	Samsung	100nF Ceramic Capacitor, 16V, X7R, Size 0402	1
C39, C40	CL05C121JB5NNNC	Samsung	120pF, Ceramic Capacitor, 50V, C0G, Size 0402	2
L1, L2, L4, L5, L6	CIG21L2R2MNE	Samsung	2.2µH 950mA, 160mΩ, L2.0mm x W1.25mm x H1.0mm	5
L3	CIG21L1R0MNE	Samsung	1.0µH 1.15A 110mΩ, L2.0mm x W1.25mm x H1.0mm	1
R7, R10	CRCW040246K4FKED	Vishay(2)	46.4 kΩ, 1%, 0402	1
R8, R16	CRCW040220KFKED	Vishay	20 kΩ, 1%, 0402	3
R23	CRCW040210KFKED	Vishay	10kΩ, 1%, 0402	1
U1	**MIC2829-xxYAL or MIC2829-xxYAB**	**Micrel, Inc.(3)**	**3G/4G HEDGE/LTE PMIC**	**1**

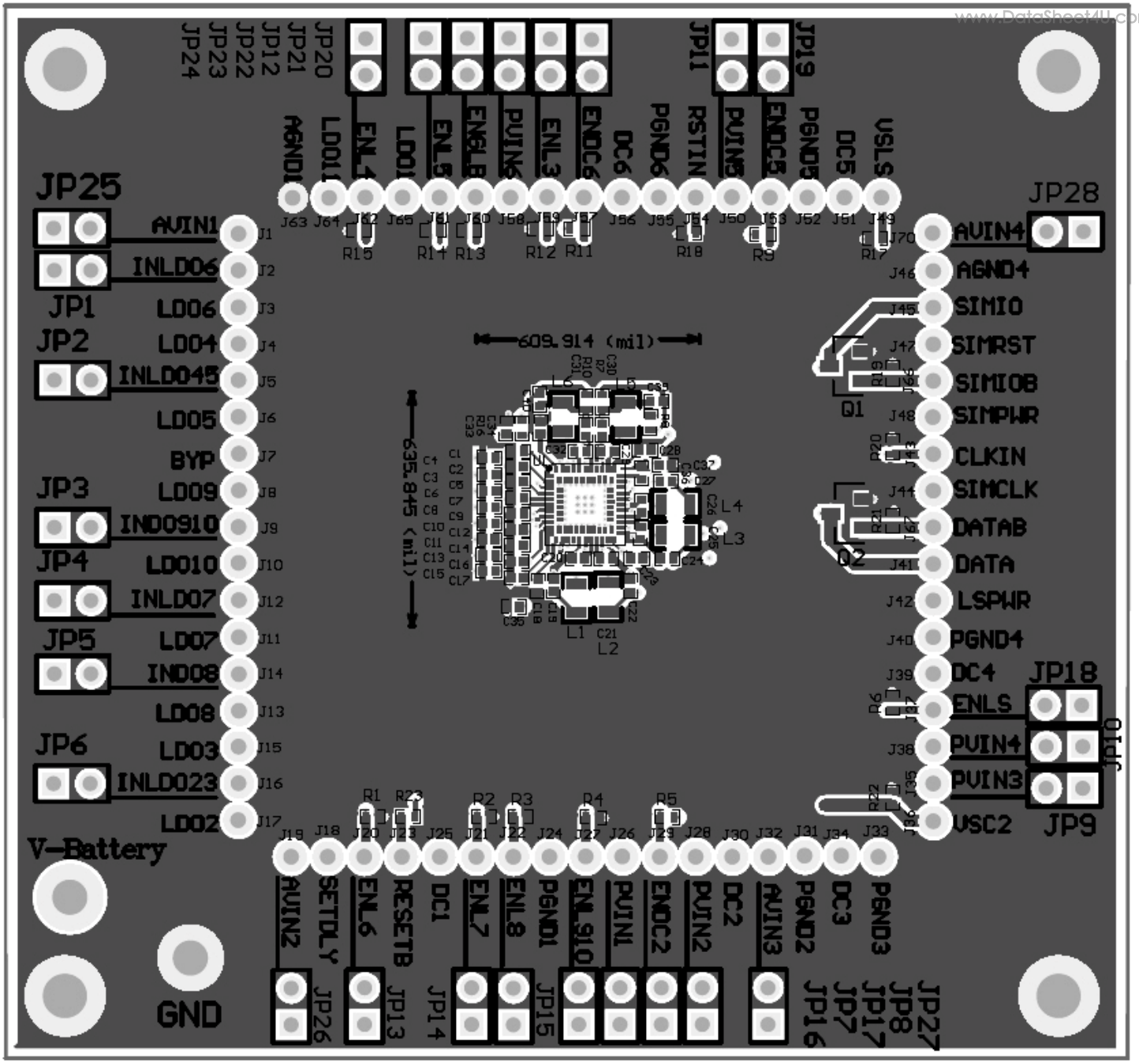
Notes:

1. Samsung: www.sem.samsung.com.
2. Vishay: www.vishay.com.
3. **Micrel, Inc: www.micrel.com.**

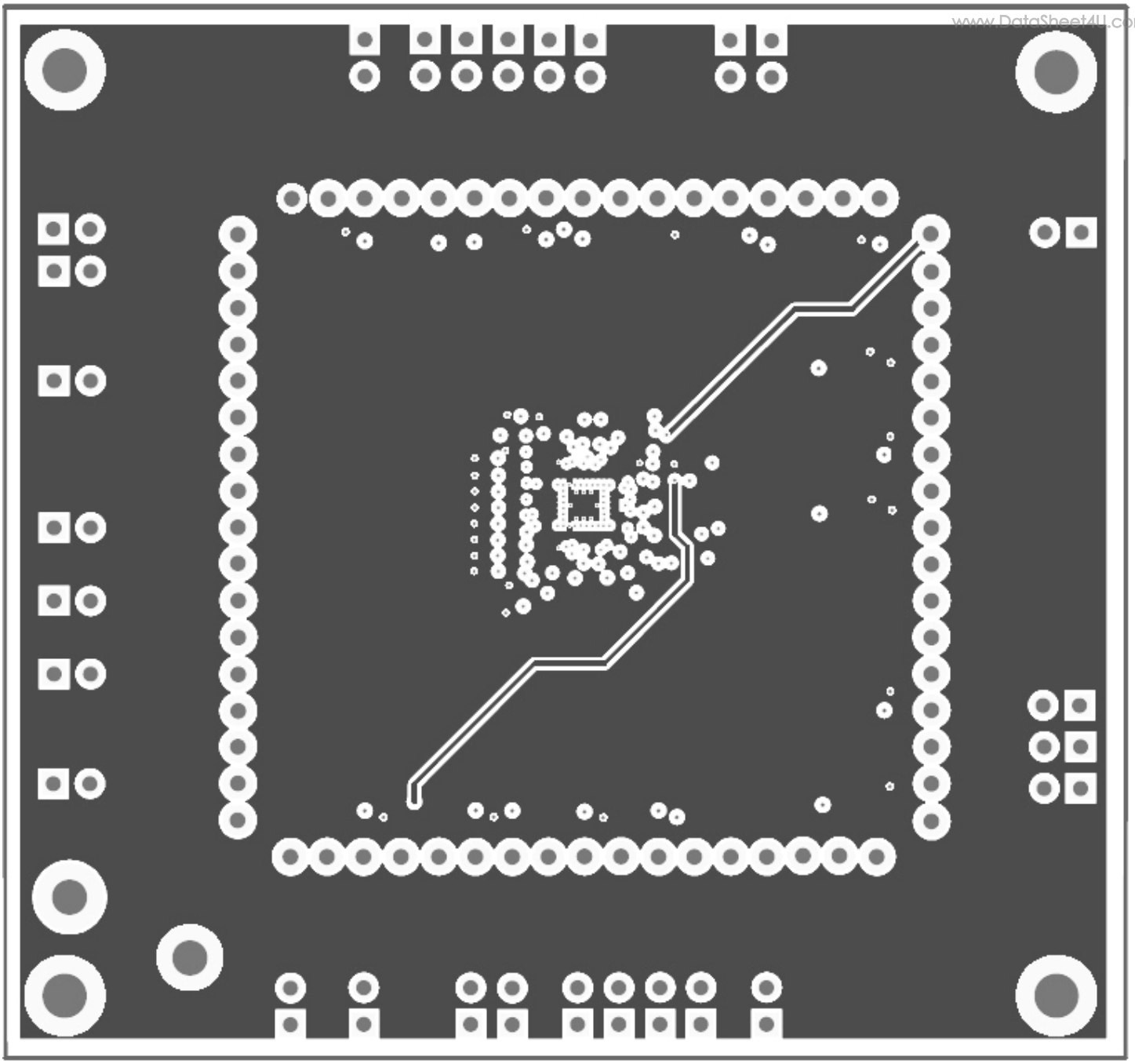
PCB Layout Recommendations



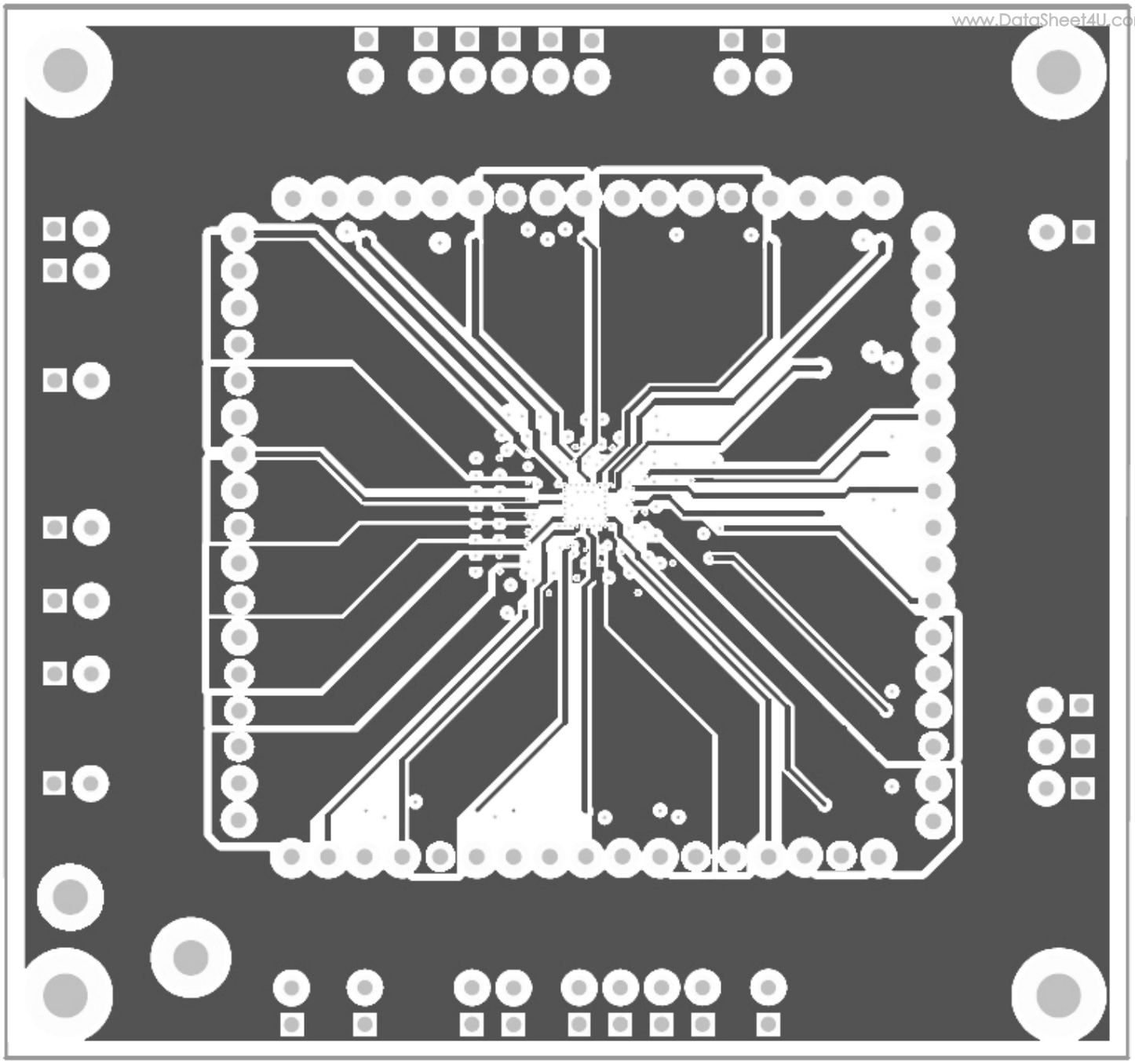
FBGA Top (Layer 1)



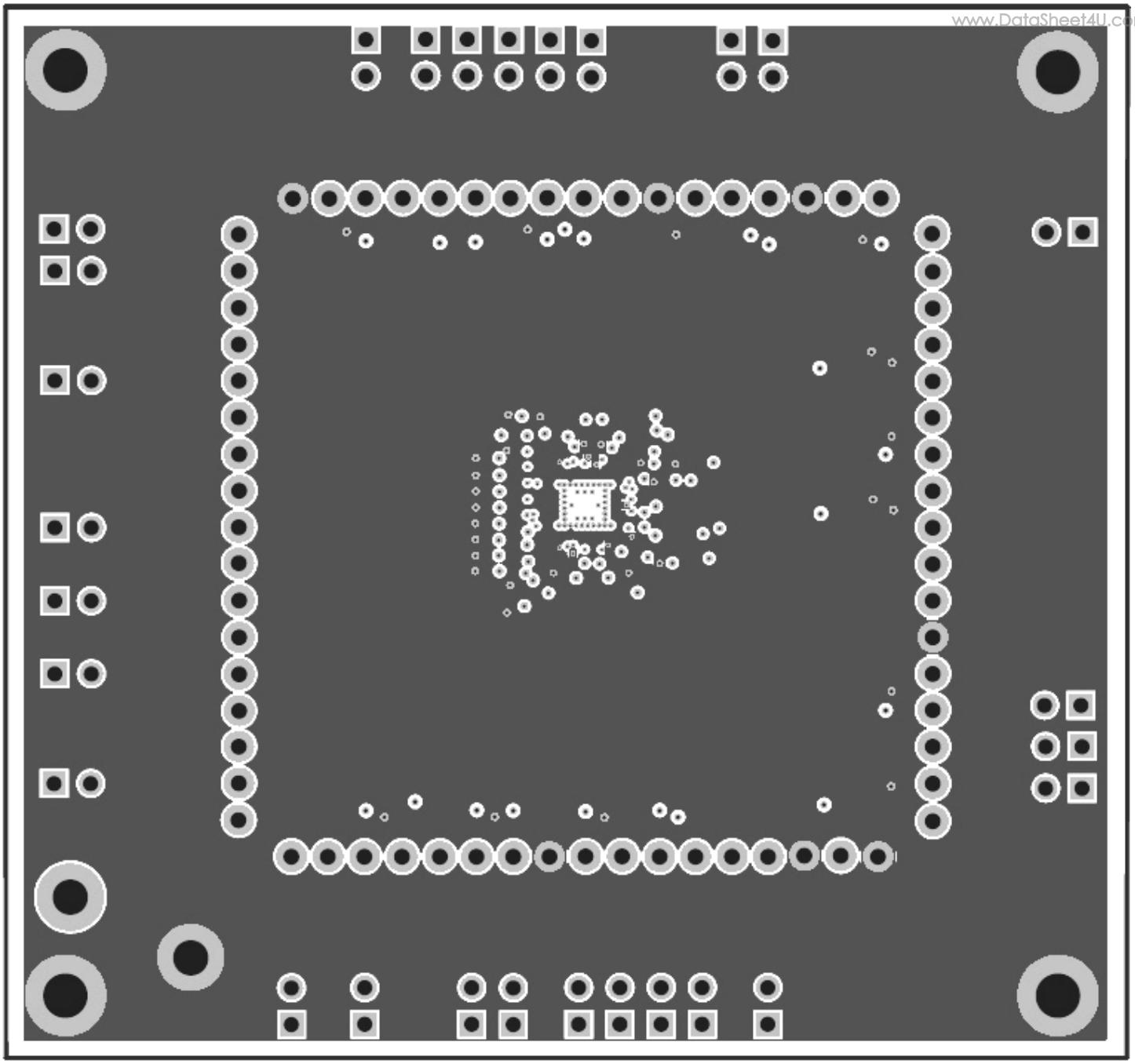
LGA Top (Layer 1)



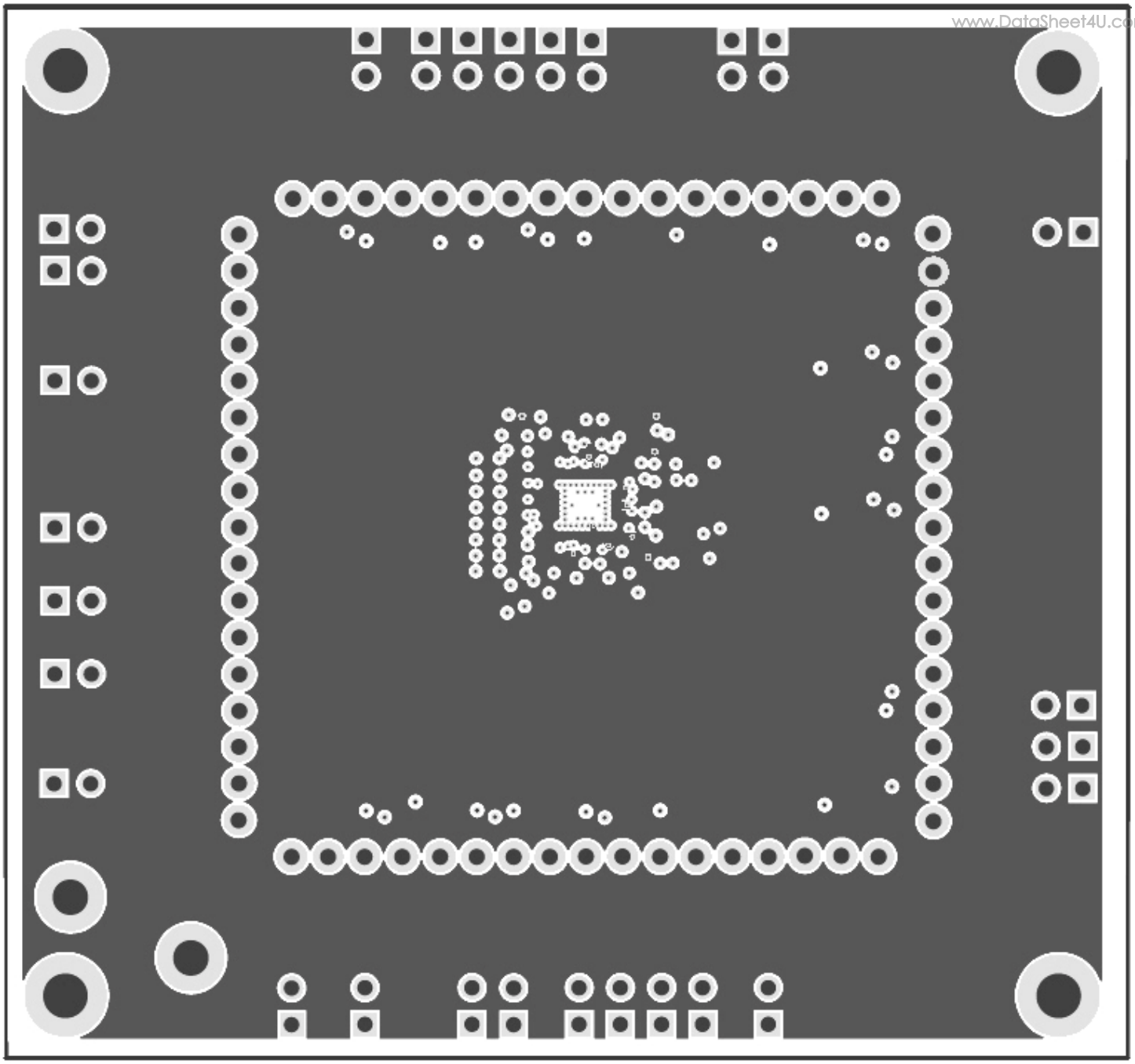
FBGA/LGA LDO GND (Layer 2)



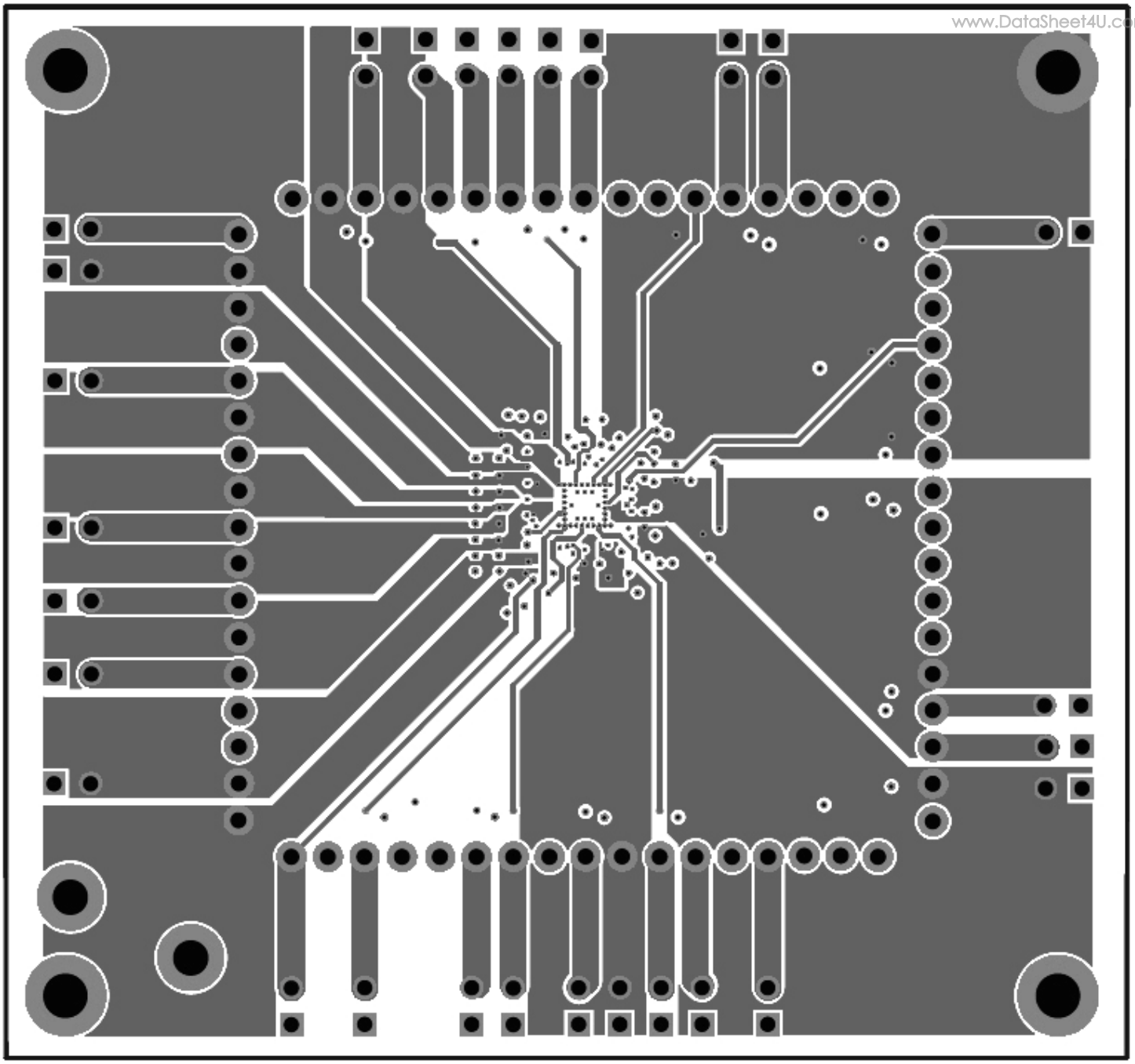
FBGA/LGA Power and Signal (Layer 3)



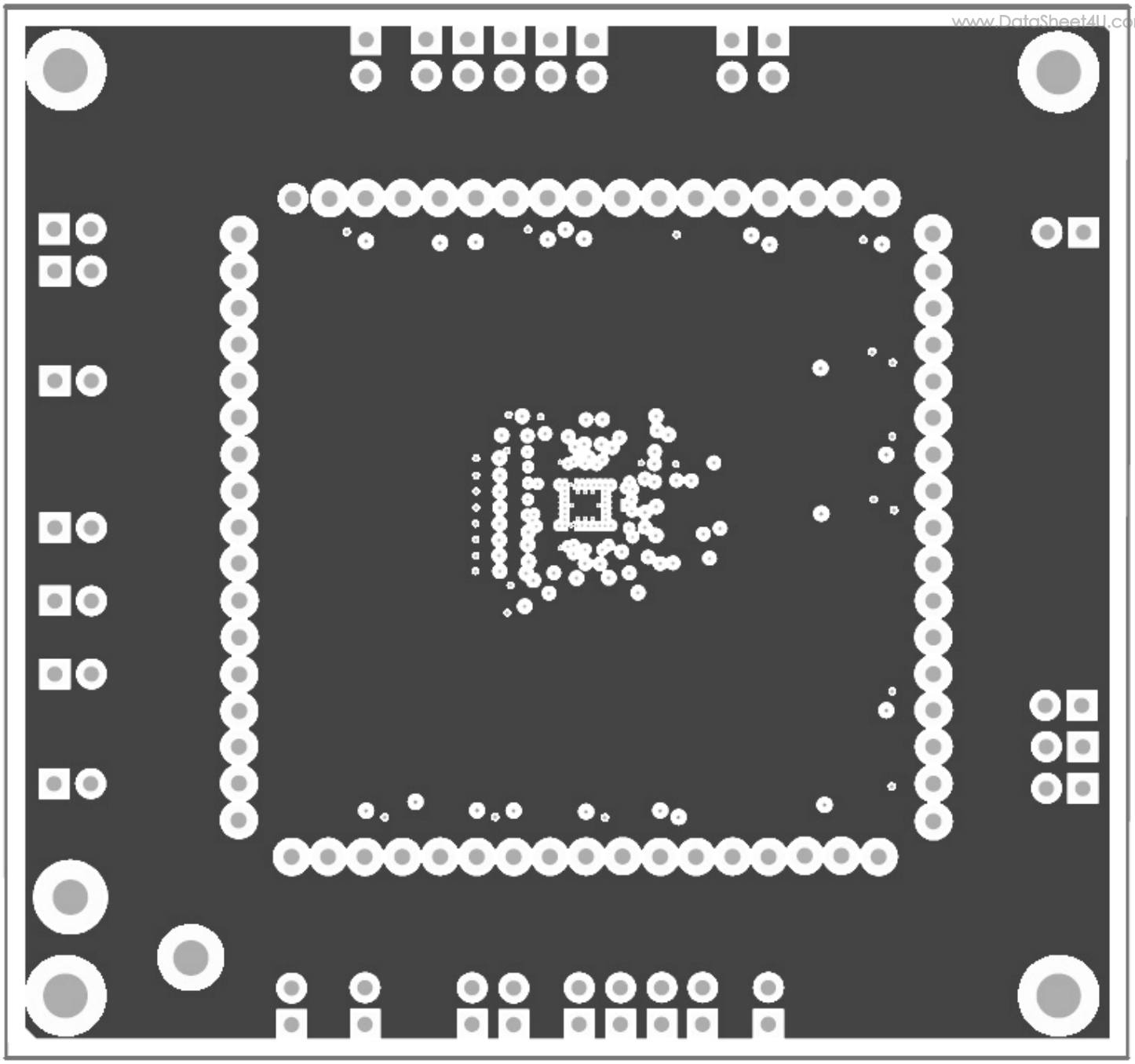
FBGA/LGA DC Regulator PGND (Layer 4)



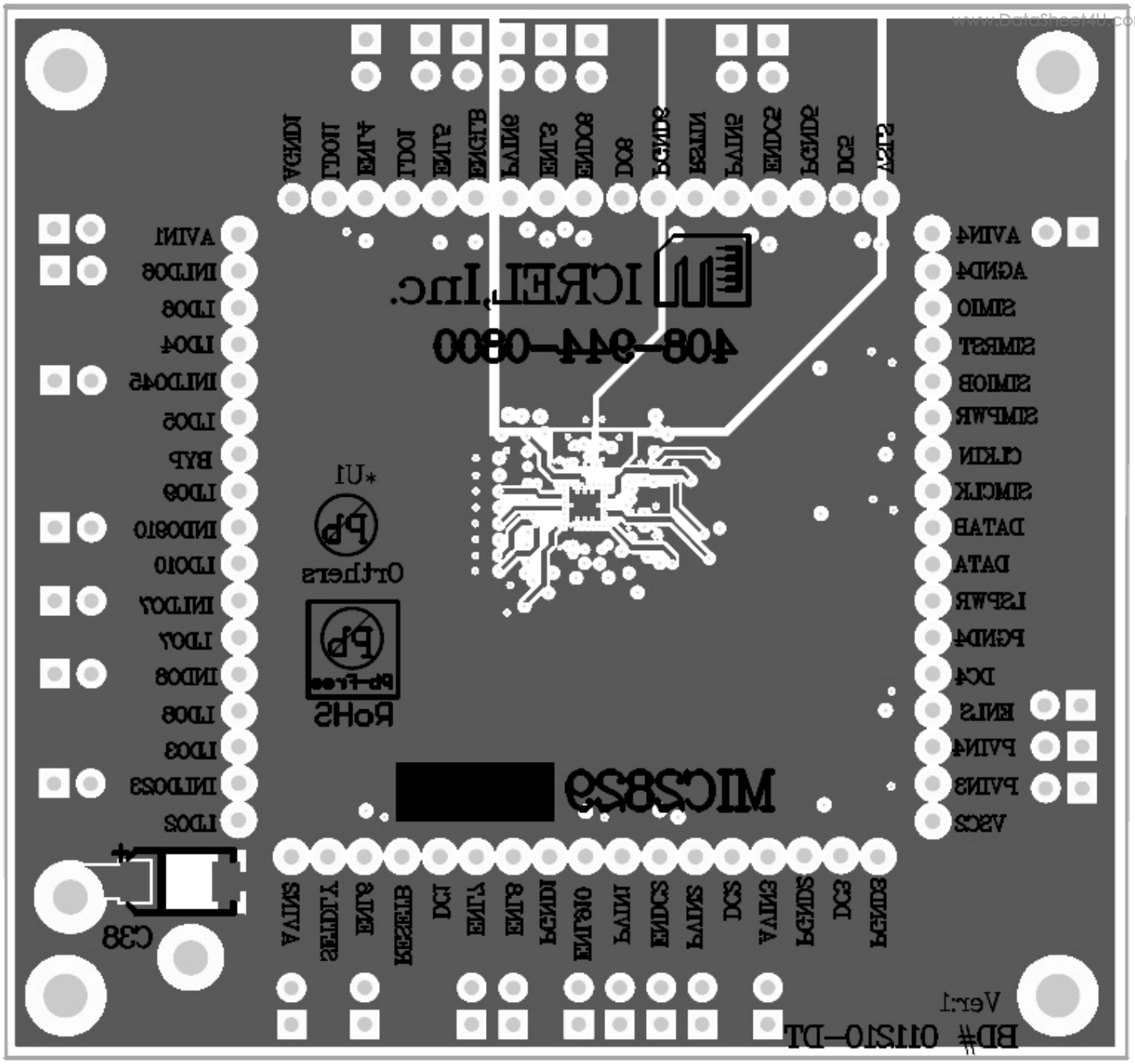
FBGA/LGA DC Regulator AGND (Layer 5)



FBGA/LGA Signal (Layer 6)

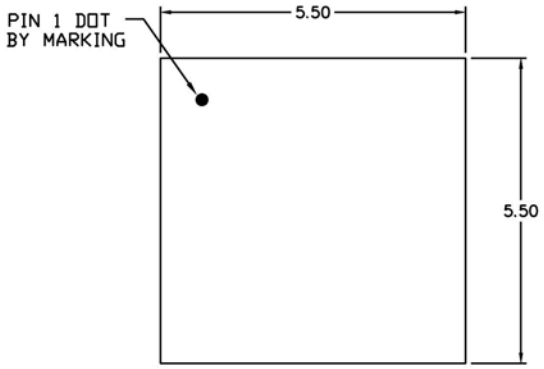


FBGA/LGA LDO GND (Layer 7)

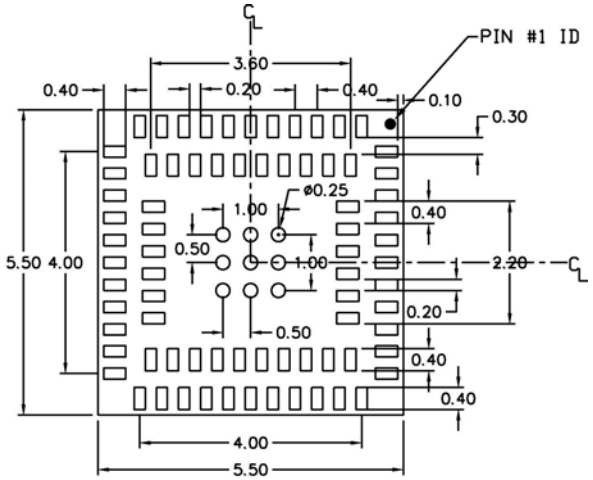


FBGA/LGA Bottom (Layer 8)

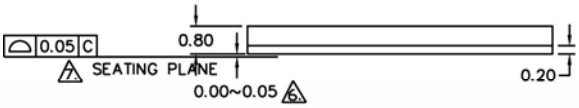
Package Information (LGA)



TOP VIEW



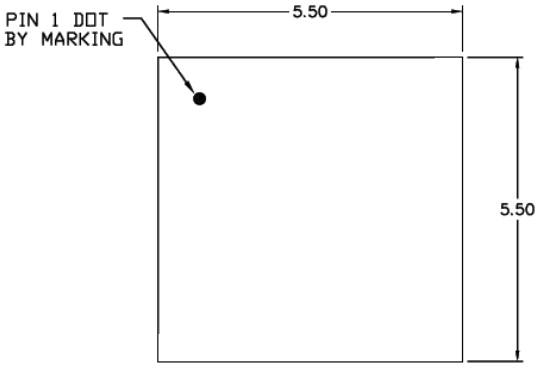
BOTTOM VIEW



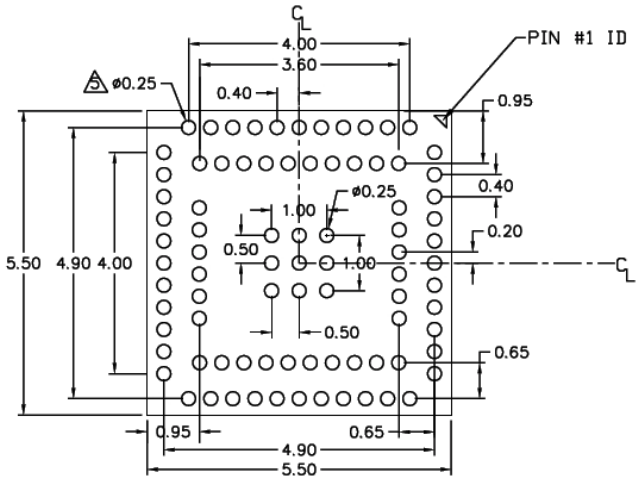
SIDE VIEW

76-pin 5.5mm x 5.5mm LGA Package (AL)

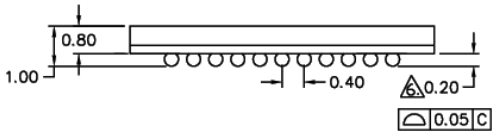
Package Information (FBGA)



TOP VIEW



BOTTOM VIEW



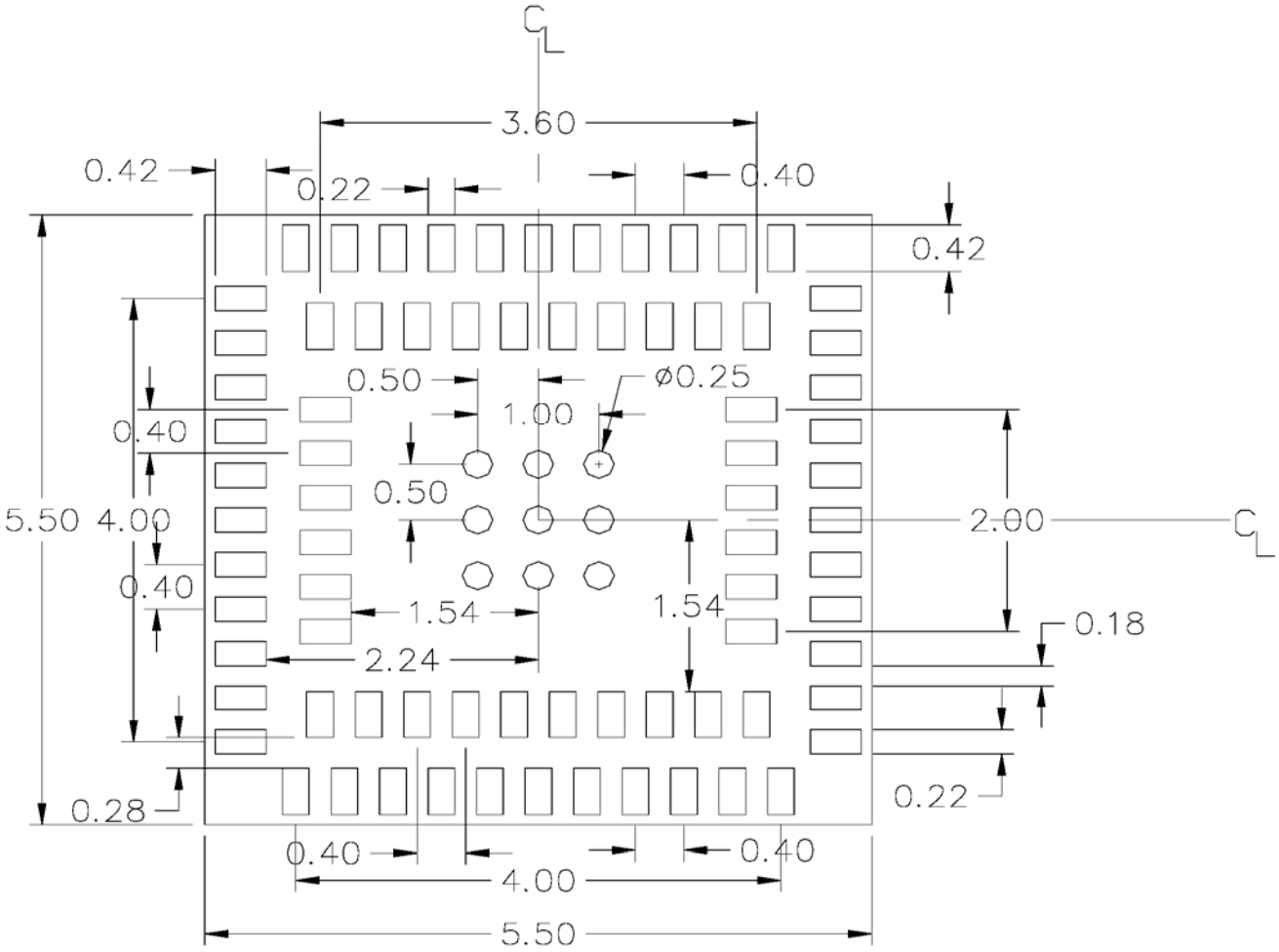
SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO SOLDER BUMPS AND IS MEASURED BETWEEN 0.10 AND 0.15 mm FROM TIP.
6. APPLIED ONLY FOR TERMINALS.

85-pin 5.5mm x 5.5mm FBGA Package (AB)

Recommended Land Pattern (LGA)

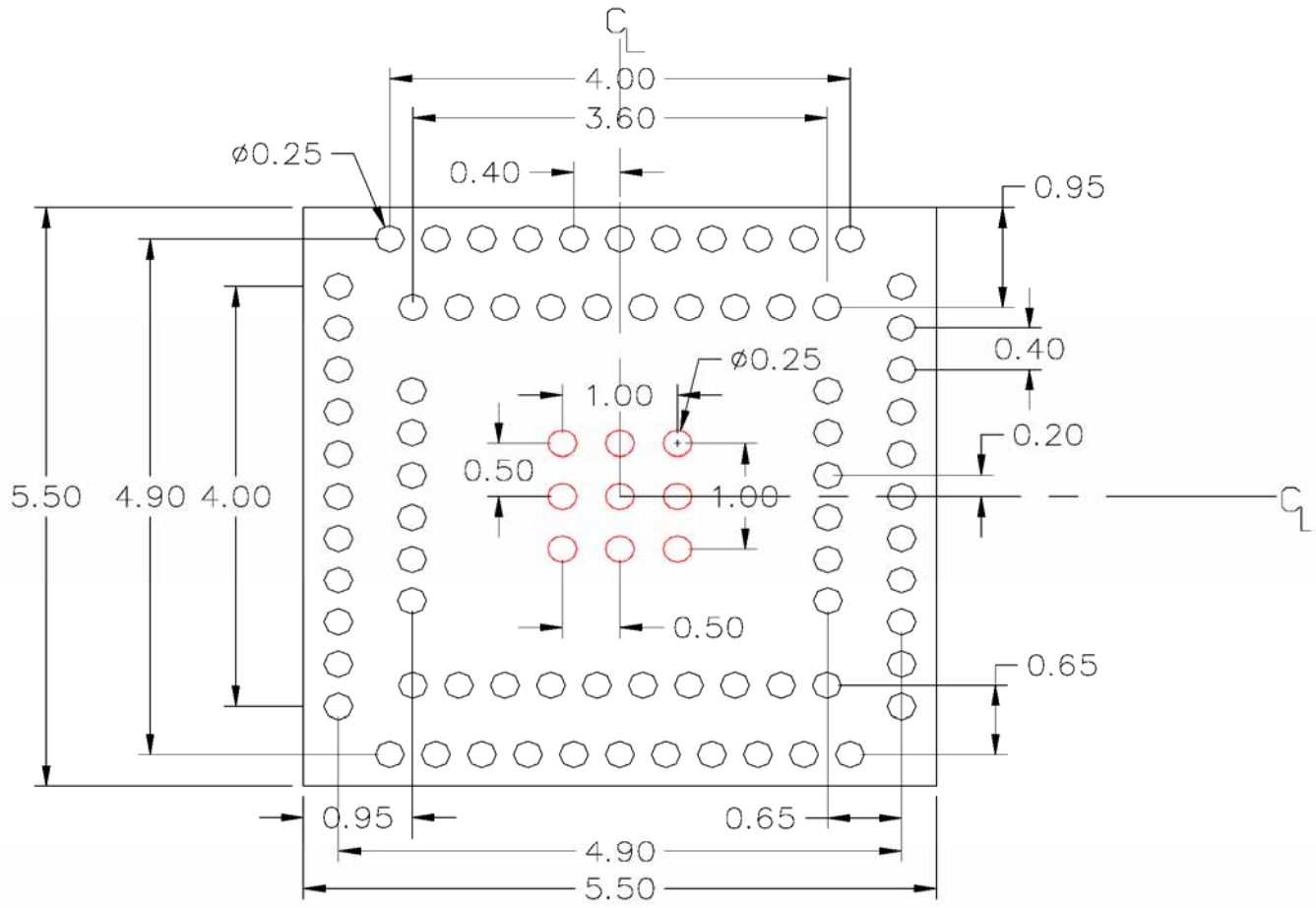
LP # LGA5555Q-76LD-LP-1
All units are in mm
Tolerance ± 0.02 if not noted



76-pin 5.5mm x 5.5mm LGA Land Pattern

Recommended Land Pattern (FBGA)

LP # FBGA5555-85LD-LP-1
All units are in mm
Tolerance ± 0.02 if not noted



Red circle indicates Thermal PAD. It should be connected to GND plane for maximum thermal performance.

85-pin 5.5mm x 5.5mm FBGA Land Pattern

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com