MIC21LV32

36V Dual Phase, Advanced COT Buck Controller Stackable for Multiphase Operation

Features

- Input Voltage Range: 4.5V to 36V
- Input Down to 2V when V_{DD} = 5V from External Supply
- Adjustable Output Voltage from 0.6V to 28V
- Adaptive Constant On-Time Control:
  - High DeltaV operation
  - Any Capacitor™ stable
- 0.6V Internal Reference with ±1% Accuracy
- Novel Ripple Injection Method to Allow Greater than 50% Duty Cycle Operation
- **Operates in CCM, Stackable for Multiphase Operation up to Eight Phases**
- Accurate Current Balancing Between Phases
- Accurate 180° Phasing of Outputs
- 100 kHz to 1 MHz Switching Frequency per Phase
- Secondary LDO to Improve System Efficiency
- Supports Start-up to Pre-bias Output
- Remote Sense Amplifier for Tight Output Regulation
- **Droop Feature to Support Adaptive Voltage Positioning (AVP) for Improved Load Transient Response**
- Precision Enable Function for Low Standby Current
- External Programmable Soft Start to Reduce Inrush Current
- Lossless R_{DSON} Current Sensing with NTC Temperature Compensation or Resistor Sensing Method
- Programmable Current Limit and Hiccup Mode Short-Circuit Protection
- Thermal Shutdown with Hysteresis
- –40°C to +125°C Junction Temperature Range
- Compact Size 5 mm x 5 mm 32-Pin VQFN Package

Applications

- Distributed Power Systems
- Communications/Networking Infrastructure
- Printers, Scanners, Graphic and Video Cards
- FPGA, CPU, Memory, GPU Core Supplies

General Description

The MIC21LV32 is a constant on-time, dual phase synchronous buck controller featuring a unique adaptive on-time control architecture with stackable feature up to eight phases. The MIC21LV32 operates over an input supply range from 4.5V to 36V and can be used to supply up to 50A of output current. The output voltage is adjustable down to 0.6V with an ensured accuracy of ±1% at the FBS pin. The device operates with programmable switching frequency from 100 kHz to 1 MHz per phase.

The Hyper Speed Control® architecture supports ultra-fast transient response under medium to heavy loads. The soft start is also programmable externally with a capacitor, thus enabling safe start-ups into heavy loads. The MIC21LV32 has a remote sense amplifier for accurate output voltage control.

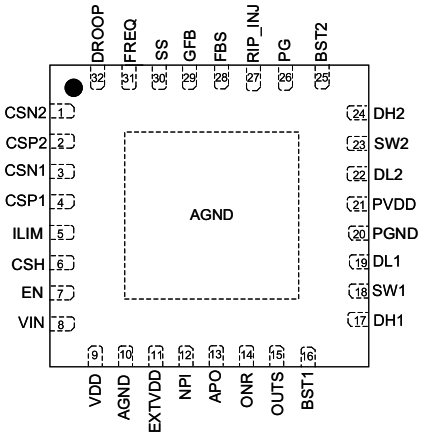
The MIC21LV32 offers a full suite of protection features to ensure protection of the IC during Fault conditions. These include undervoltage lockout to ensure proper operation, programmable soft start to reduce inrush current, Hiccup mode short-circuit protection and thermal shutdown.

The MIC21LV32 is available in a 32-pin 5 mm x 5 mm VQFN package with a –40°C to +125°C operating junction temperature range.

Package Type

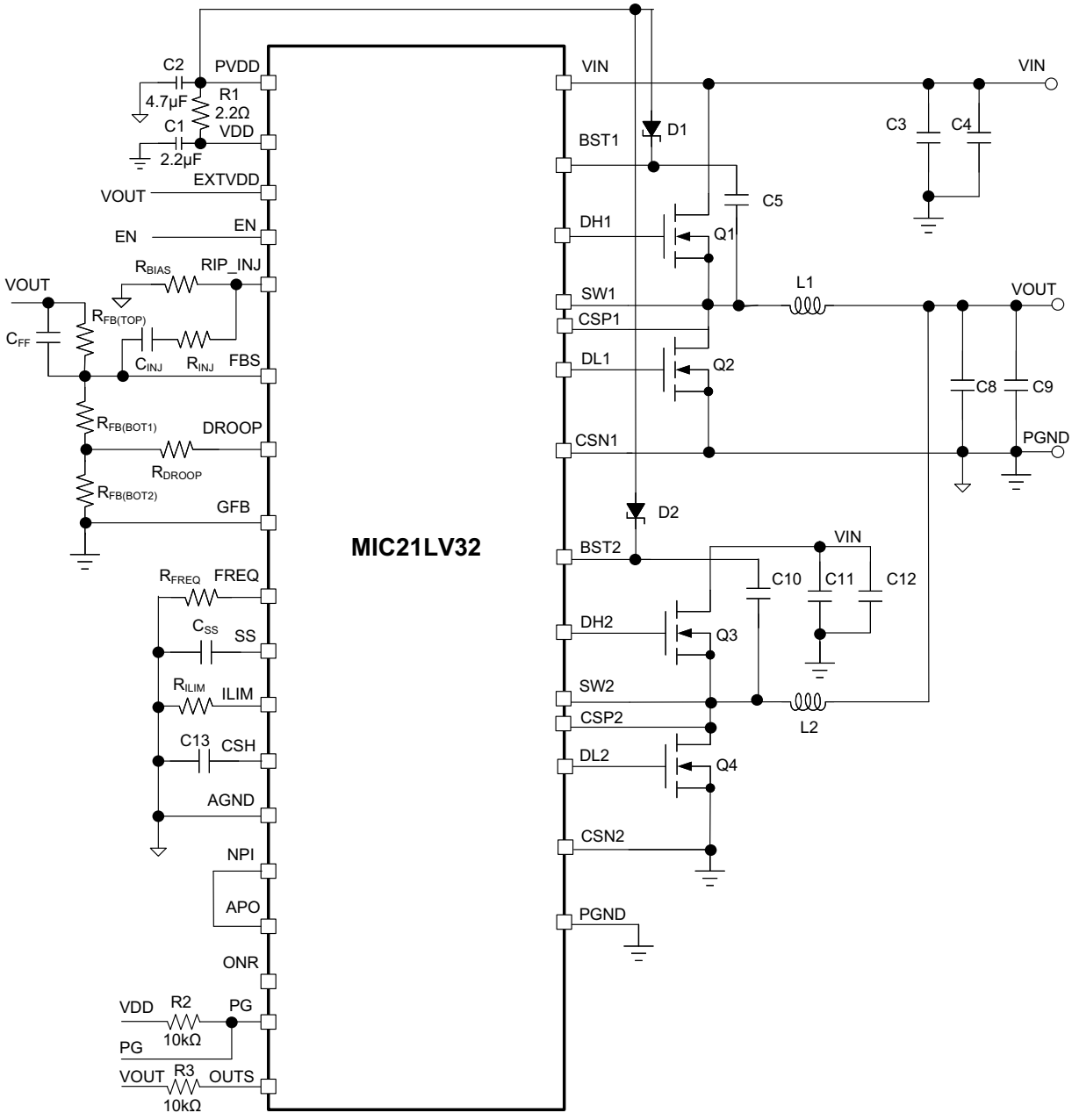
MIC21LV32

32-Pin 5 mm X 5 mm VQFN* (ML)

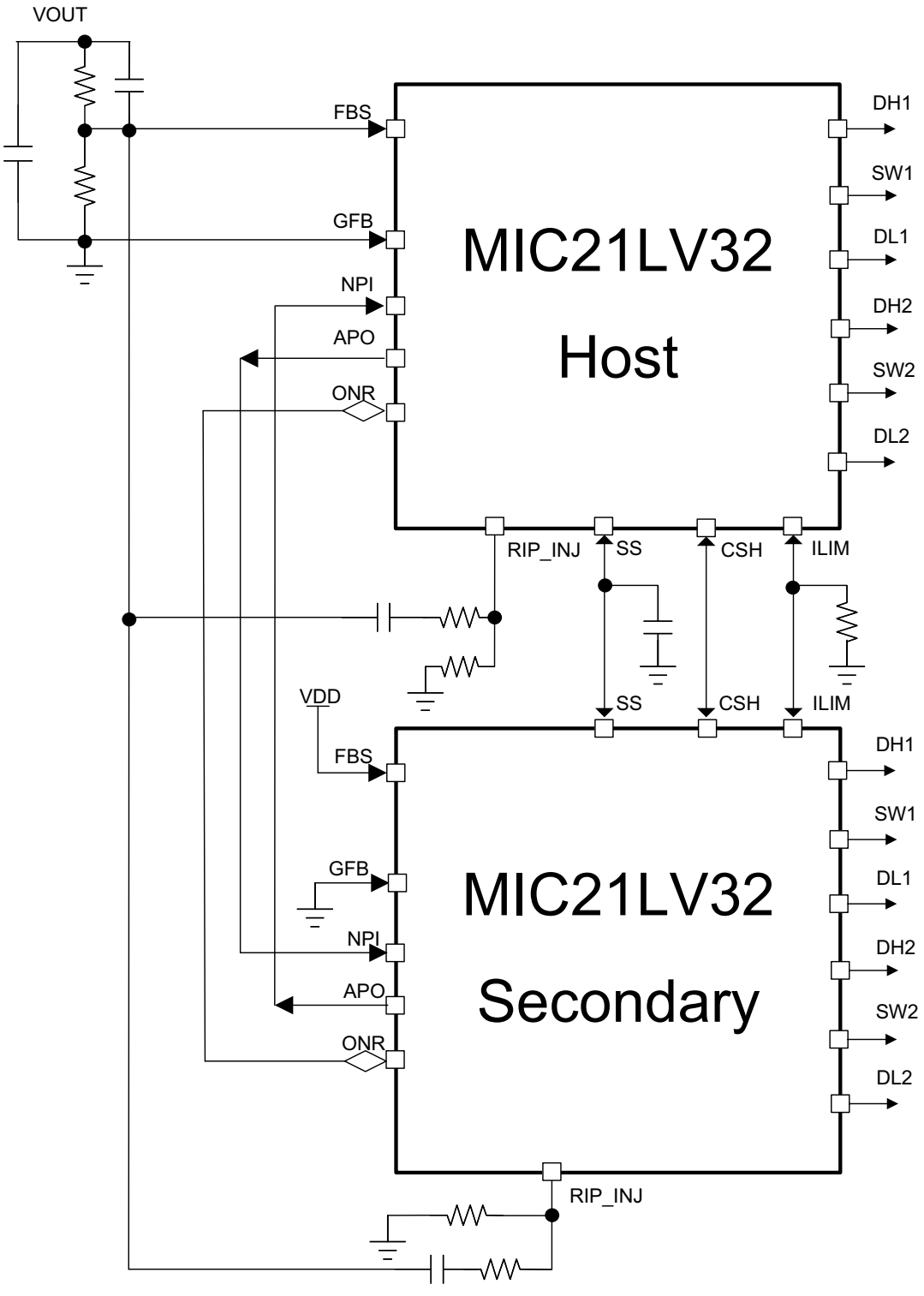


*Includes Exposed Thermal Pad (EP); see Table 3-1.

Typical Application Circuits

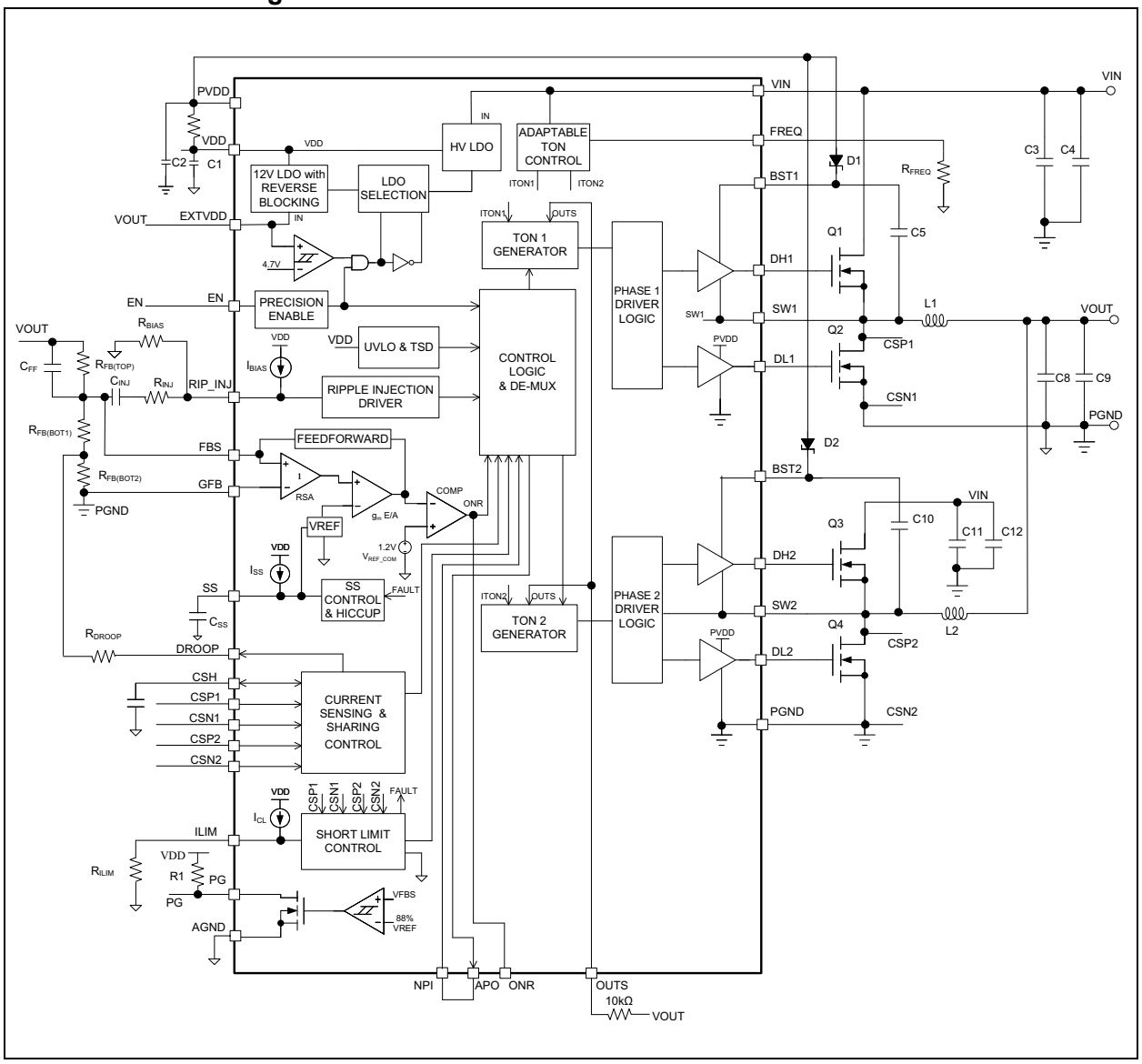


Application circuit based on R_{DSON} current sensing without temperature compensated ILIM and Droop. Temperature compensation can be done using NTC resistors (refer to **Section 4.0 "Functional Description"**).



MIC21LV32 Connected in 4-Phase Configuration

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} to PGND ..... -0.3V to +40V
V_{DD}, OUTS to AGND ..... -0.3V to +6V
PV_{DD} to PGND ..... -0.3V to +6V
EN to AGND ..... -0.3V to (V_{IN} + 0.3V)
SW1, SW2, CSP1, CSP2 to PGND ..... -0.3V to (V_{IN} + 0.3V)
BST1 to SW1, BST2 to SW2 ..... -0.3V to 6V
DH1 to SW1, DH2 to SW2 ..... -0.3V to (V_{BSTX} -V_{SWX} + 0.3V)
I_{LIM}, FREQ, SS, RIP_INJ, FBS, DROOP, PG, CSH, NPI, APO, ONR to AGND ..... -0.3V to (V_{DD} + 0.3V)
EXTVDD to AGND ..... -0.3V to +14V
CSN1, CSN2, GFB, PGND to AGND ..... -0.3V to +0.3V
Maximum Junction Temperature (T_J) ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (T_{LEAD}) ..... +300°C
ESD Rating(1)(HBM) 2000V
ESD Rating (1)(MM) 200V

Operating Ratings‡

Supply Voltage (V_{IN}) ..... 4.5V to 36V
PV_{DD}, V_{DD} Pin Voltage ..... 4.5V to 5.5V
OUTS Pin Voltage ..... 0.6V to 5.5V
EXTVDD Pin Voltage ..... 0V to 13V
SW1, SW2, CSP1, CSP2 Pin Voltage ..... 0V to V_{IN}
ILIM, FREQ, SS, RIP_INJ, FBS, DROOP, PG, CSH, NPI, APO, ONR to AGND ..... 0V to V_{DD}
DL1, DL2 to AGND ..... 0V to V_{DD}
DH1 to SW1, DH2 to SW2 ..... 0V to V_{DD}
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Junction Temperature(2) (T_J) ..... -40°C to +125°C

† **Notice:** Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not ensured to function outside its operating ratings.

Note 1: Specification for packaged product only.

2: $P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA}$, where θ_{JA} depends upon the printed circuit layout.

ELECTRICAL CHARACTERISTICS[1]

Electrical Characteristics: V_{IN} = 12V; V_{OUT} = 1.2V; f_{SW} = 500 kHz/phase; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C, unless noted. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range	V_{IN}	**4.5**	—	**36**	V	
Quiescent Supply Current	I_Q	—	5000	**8000**	µA	V_{FBS} = +1.5V, V_{IN} = 36V
Shutdown Current	I_{SD}	—	25	**50**	µA	V_{IN} = 36V, V_{EN} = 0V
V_{DD} and EXTVDD						
V_{DD} Voltage Range	V_{DD}	**4.8**	5.1	**5.4**	V	V_{IN} = 6V to 36V, I_{VDD} = 20 mA **(Note 5)**
V_{DD} Undervoltage Lockout Upper Threshold	V_{DDUV_R}	3.7	4.2	4.5	V	V_{DD} rising
V_{DD} UVLO Hysteresis	V_{DDUV_HYS}	—	600	—	mV	Hysteresis
V_{DD} Regulation	ΔV_{DD}	—	1	**2.5**	%	V_{IN} = 24V, I_{VDD} from 1 mA to 40 mA **(Note 5)**
V_{DD} Regulator Dropout Voltage	V_{DROP_VDD}	—	0.8	1.05	V	V_{IN} = 5.5V, I_{VDD} = 25 mA
EXTVDD Switchover Voltage	V_{SO_EVDD}	**4.5**	4.7	**4.9**	V	V_{IN} = 24V, EXTVDD rising, I_{VDD} = 40 mA
EXTVDD Switchover Voltage Hysteresis	V_{SO_HYS}	—	250	—	mV	Hysteresis
EXTVDD Dropout Voltage	V_{DROP_EVDD}	—	250	—	mV	V_{EXTVDD} = 5V, I_{VDD} = 40 mA
EXTVDD Leakage Current	I_{LK_EVDD}	—	0.1	—	µA	V_{EXTVDD} = 14V, V_{EN} = 0V
Soft Start						
Soft Start Source Current	I_{SS}	0.9	1.2	1.7	µA	
DC-DC Regulator						
Output Voltage Adjustable Range	V_{OUT}	0.6	—	28	V	**Note 2**
Reference and Remote Sensing Amplifier						
Feedback Regulation Voltage	$V_{FBS-GFB}$	**0.594**	0.6	**0.606**	V	-40°C ≤ T_J ≤ +125°C, measured with EA in servo loop
FBS Bias Current	I_{FBS}	—	2	—	nA	V_{FBS} = +0.6V **(Note 2)**
GFB Bias Current	I_{GFB}	—	12	—	µA	
Remote Sense Amplifier Gain	G_{RSA}	—	1.00	—	V/V	
Enable						
Enable Upper Threshold Voltage	V_{EN_TH}	**1.1**	1.2	**1.35**	V	Enable rising
Enable Hysteresis	V_{EN_HYS}	—	65	—	mV	
Enable Bias Current	I_{EN}	—	100	**200**	nA	V_{EN} = 12V

Note 1: Specification for packaged product only.

2: Ensured by design and characterization. Not production tested.

3: Measured in Test mode.

4: The maximum duty cycle is limited by the fixed mandatory off-time of typically 360 ns.

5: Limited by maximum junction temperature T_J = 125°C.

ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Characteristics: V_{IN} = 12V; V_{OUT} = 1.2V; f_{SW} = 500 kHz/phase; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C, unless noted. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
On Timer						
Nominal Switching Frequency per Phase	f_{SWNOM_PH}	**450**	500	**550**	kHz	V_{IN} = 12V, V_{OUTS} = 5V, R_{FREQ} = 40.2 kΩ
Minimum Switching Frequency per Phase	f_{SWMIN_PH}	—	100	—	kHz	V_{IN} = 12V, V_{OUTS} = 5V, R_{FREQ} = 200 kΩ
Maximum Switching Frequency per Phase	f_{SWMAX_PH}	—	800	—	kHz	V_{IN} = 12V, V_{OUTS} = 5V, R_{FREQ} = 25.5 kΩ
Minimum On-Time	T_{ONMIN}	—	60	—	ns	Measured in application (**Note 2**)
Minimum Off-Time	T_{OFFMIN}	—	360	—	ns	V_{FBS} = 0V
Maximum Duty Cycle	D_{MAX}	—	85	—	%	f_{SW} = 400 kHz per phase (**Note 4**)
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{FBS} = +1V (**Note 2**)
Current Limit						
ILIM Source Current	I_{CL}	**8.64**	9.6	**10.56**	µA	
ILIM Source Current Temperature Coefficient	TC_{ICL}	—	0	—	ppm/°C	**Note 2**
Nominal Current Limit Threshold Voltage per Phase	V_{ILIM_TH}	142	156	174	mV	R_{ILIM} = 60.4 kΩ, R_{ILIM} = 105 kΩ, R_{ILIM} = 21 kΩ
		—	47	—	mV	
		—	250	—	mV	
Negative Current Limit Threshold Voltage	V_{ILIM_NTH}	60	75	90	mV	R_{ILIM} = 60.4 kΩ
Current Sharing Amplifier						
CSH Operating Point	V_{CSH_OP}	**1.154**	1.19	**1.226**	V	V_{CSN1} = V_{CSN2} = V_{CSP1} = V_{CSP2} = 0V
Current Sense Amplifier(s) Gain	G_{CSA}	—	8	—	V/V	As reflected on V_{CSH} pin and DROOP pin
Current Sense Input Voltage Range	V_{CS}	**–120**	—	**+120**	mV	-40ºC ≤ T_J ≤ +125ºC
Phase to Phase Current Balance	ΔI_{PH}	—	5	—	%	Using equal sense resistors on the bottom, equal inductances, V_{OUT} = 5V, f_{SW} = 500 kHz, V_{IN} = 12V, $V_{CSP1} - V_{CSN1}$= –120 mV, $V_{CSP2} - V_{CSN2}$= –120 mV
MIC21LV32 to MIC21LV32 Current Balance	ΔI_{PH_DEV}	—	8	—	%	In stacking applications

Note 1: Specification for packaged product only.

2: Ensured by design and characterization. Not production tested.

3: Measured in Test mode.

4: The maximum duty cycle is limited by the fixed mandatory off-time of typically 360 ns.

5: Limited by maximum junction temperature T_J = 125°C.

ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Characteristics: V_{IN} = 12V; V_{OUT} = 1.2V; f_{SW} = 500 kHz/phase; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C, unless noted. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Adaptive Voltage Positioning (AVP), i.e., DROOP						
V_{DROOP} at No Load	V_{DRP_NLOAD}	—	10	—	mV	Measure DROOP voltage ~ 0V when $V_{CSP1} – V_{CSN1}$ = 0V, $V_{CSP2} – V_{CSN2}$ = 0V
V_{DROOP} at Maximum Positive Range	$V_{DRP(PMAX)}$	—	0.96	—	V	Measure DROOP voltage ~1.2V when $V_{CSP1} – V_{CSN1}$ = -120 mV, $V_{CSP2} – V_{CSN2}$ = -120 mV
Ripple Injection						
Ripple Injection Pulse Width	$t_{PW(RI)}$	—	100	120	ns	
Ripple Injection Prepositioning Current	I_{BIAS}	—	4.8	6	µA	Force V_{RIPINJ} = 0V, V_{SS} = 0V, measure current
Injection Driver On-Resistance	$R_{DSON(INJ)}$	—	50	—	Ω	
Internal MOSFET Drivers						
DHx On-Resistance, High State	R_{ON_DHH}	—	2.5	4.5	Ω	I_{SOURCE} = 0.1A
DHx On-Resistance, Low State	R_{ON_DHL}	—	1.6	3.2	Ω	I_{SINK} = 0.1A
DLx On-Resistance, High State	R_{ON_DLH}	—	2.5	4.5	Ω	I_{SOURCE} = 0.1A
DLx On-Resistance, Low State	R_{ON_DLL}	—	0.8	1.5	Ω	I_{SINK} = 0.1A
SW, VIN and BST Leakage						
BST Leakage	$I_{LEAK(BST)}$	—	—	10	µA	V_{IN} = 36V
VIN Leakage	$I_{LEAK(VIN)}$	—	—	50	µA	V_{IN} = 36V
SW Leakage	$I_{LEAK(SW)}$	—	—	20	µA	V_{IN} = 36V
Power Good (PG)						
PG Threshold from Low-to-High	V_{PG_TH}	**83**	88	**93**	$\%V_{OUT}$	V_{FBS} rising
PG Threshold Hysteresis	V_{PG_HYS}	—	7	—	$\%V_{OUT}$	V_{FBS} falling
PG Delay	t_{D_PG}	—	100	—	µs	V_{FBS} rising
PG Low State Voltage	V_{PG_L}	—	70	**200**	mV	V_{FBS} < 90% x V_{NOM}, I_{PG} = 1 mA
PG Leakage Current	$I_{LEAK(PG)}$	—	—	**100**	nA	V_{PG} = 5.5V
Stackability APO, NPI, ONR						
High-Level Input Voltage for NPI	$V_{IH(NPI)}$	2.0	—	—	V	Current = 0.5 mA
Low-Level Input Voltage for NPI	$V_{IL(NPI)}$	—	—	0.8	V	Current = 0.5 mA
High-Level Output Voltage for APO	$V_{OH(APO)}$	—	4.7	—	V	Current = 0.5 mA
Low-Level Output Voltage for APO	$V_{OL(APO)}$	—	0.25	—	V	Current = 0.5 mA
High-Level Output for ONR	$V_{OH(ONR)}$	—	4.5	—	V	Current = 0.5 mA
Low-Level Output for ONR	$V_{OL(ONR)}$	—	0.25	—	V	Current = 0.5 mA
Leakage Current	I_{LEAK}	—	—	1	µA	V_{DD} = 5V
ONR Short Current	$I_{SHT(ONR)}$	—	5.8	—	mA	

Note 1: Specification for packaged product only.

2: Ensured by design and characterization. Not production tested.

3: Measured in Test mode.

4: The maximum duty cycle is limited by the fixed mandatory off-time of typically 360 ns.

5: Limited by maximum junction temperature T_J = 125°C.

ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Characteristics: V_{IN} = 12V; V_{OUT} = 1.2V; f_{SW} = 500 kHz/phase; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C, unless noted. **Boldface** values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	—	160	—	°C	T_J rising (**Note 2**)
Thermal Shutdown Hysteresis	T_{SD_HYS}	—	20	—	°C	**Note 2**

Note 1: Specification for packaged product only.

2: Ensured by design and characterization. Not production tested.

3: Measured in Test mode.

4: The maximum duty cycle is limited by the fixed mandatory off-time of typically 360 ns.

5: Limited by maximum junction temperature T_J = 125°C.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–40	—	+125	°C	**Note 1**
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Temperature	T_S	–65	—	+150	°C	
Lead Temperature	T_{LEAD}	—	—	+300	°C	Soldering, 10s
Package Thermal Resistance						
Thermal Resistance, 5 mm x 5 mm, 32-Lead VQFN	θ_{JC}	—	2	—	°C/W	Junction to case
Thermal Resistance, 5 mm x 5 mm, 32-Lead VQFN	θ_{JA}	—	34	—	°C/W	Junction to ambient

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1.5V; f_{SW} = 500 kHz/phase; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C.

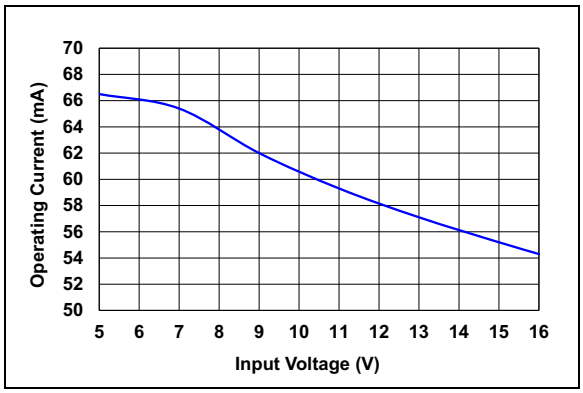


FIGURE 2-1: *V_{IN} Operating Current vs. Input Voltage.*

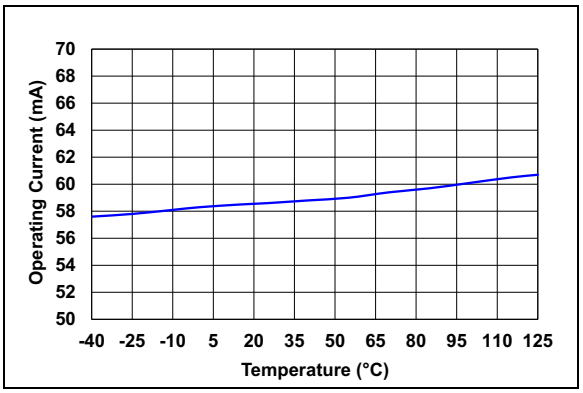


FIGURE 2-4: *V_{IN} Operating Current vs. Temperature.*

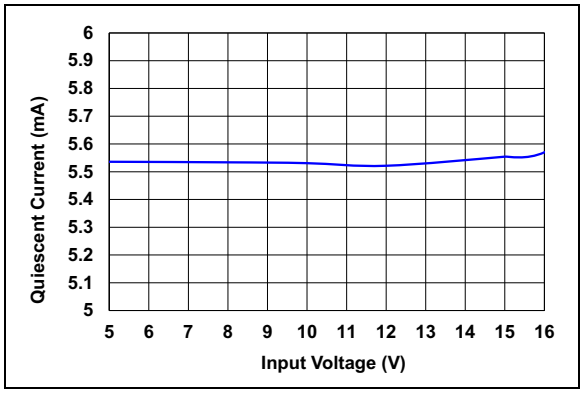


FIGURE 2-2: *V_{IN} Quiescent Current vs. Input Voltage.*

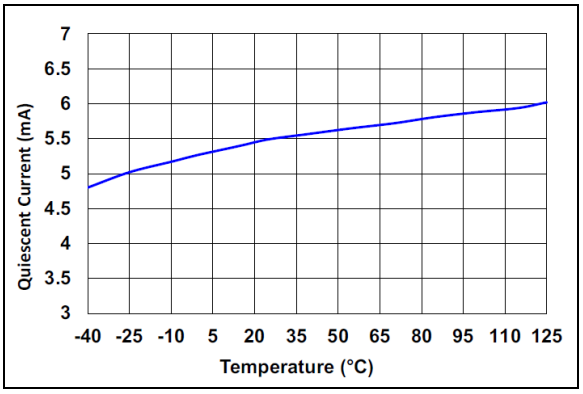


FIGURE 2-5: *V_{IN} Quiescent Current vs. Temperature.*

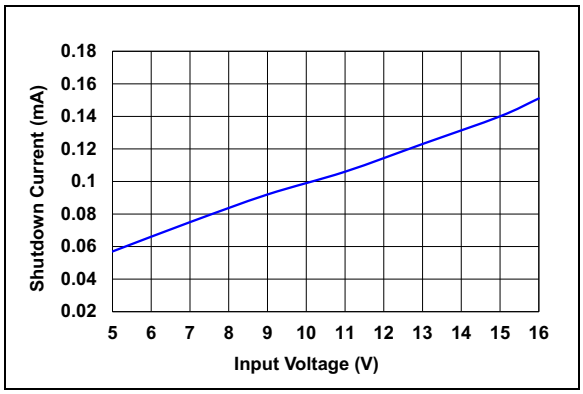


FIGURE 2-3: *V_{IN} Shutdown Current vs. Input Voltage.*

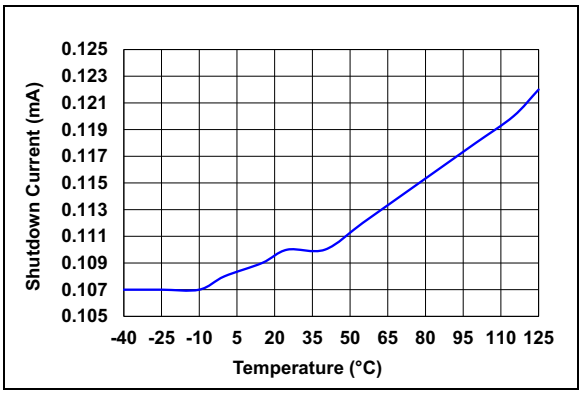


FIGURE 2-6: *V_{IN} Shutdown Current vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1.5V; f_{SW} = 500 kHz/phase; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C.

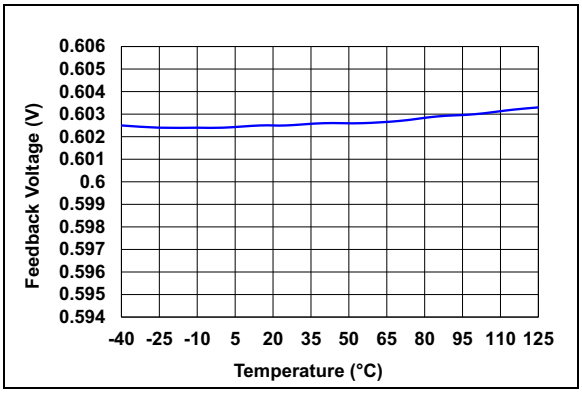


FIGURE 2-7: *Feedback Voltage vs. Temperature.*

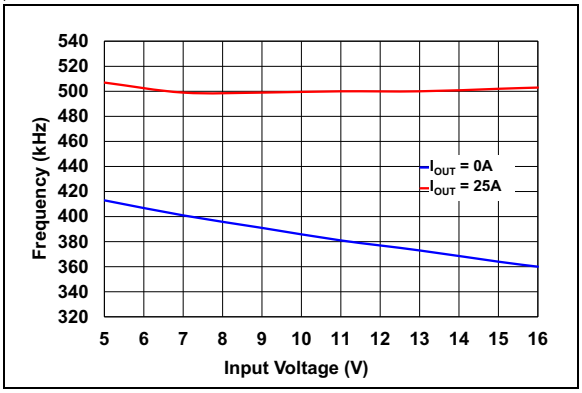


FIGURE 2-10: *Switching Frequency vs. Input Voltage.*

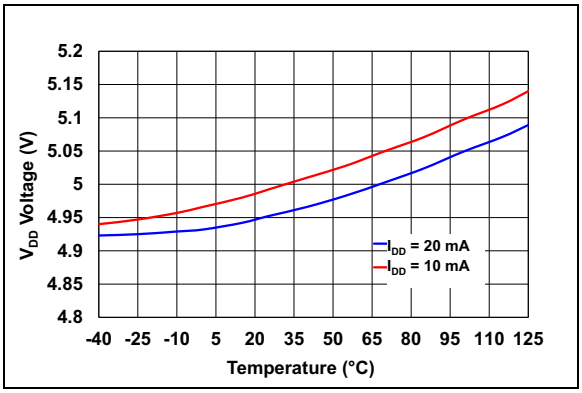


FIGURE 2-8: *V_{DD} Voltage vs. Temperature.*

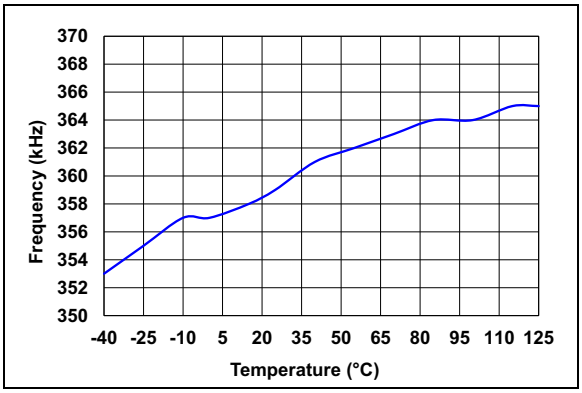


FIGURE 2-11: *Switching Frequency vs. Temperature.*

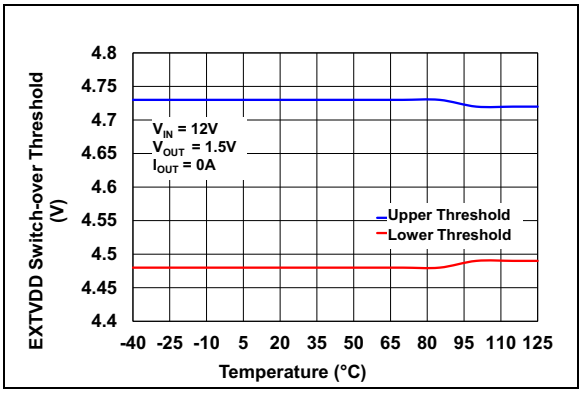


FIGURE 2-9: *EXTVDD Switchover Voltage vs. Temperature.*

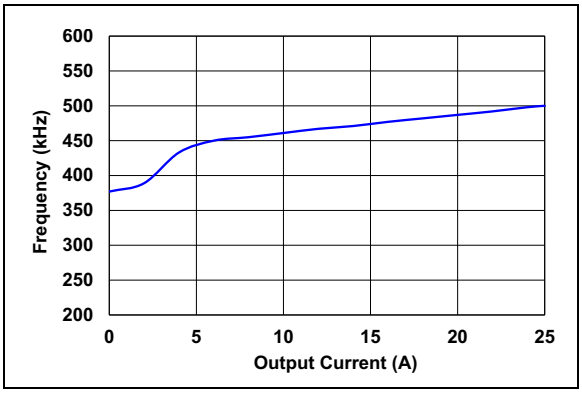


FIGURE 2-12: *Switching Frequency vs. Output Current.*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1.5V; f_{SW} = 500 kHz/phase; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C.

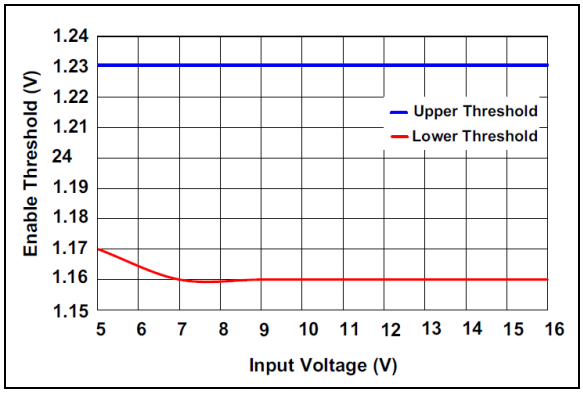


FIGURE 2-13: *Enable Threshold Voltage vs. Input Voltage.*

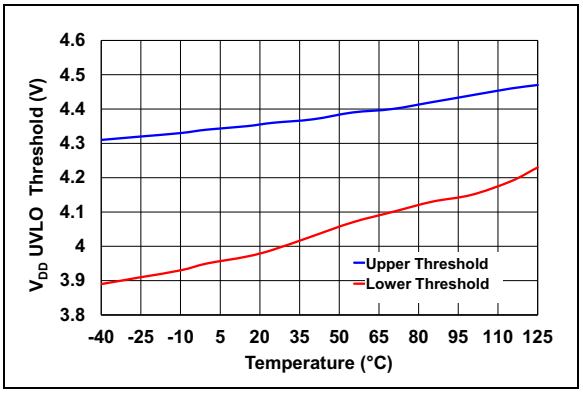


FIGURE 2-16: *V_{DD} UVLO Threshold vs. Temperature.*

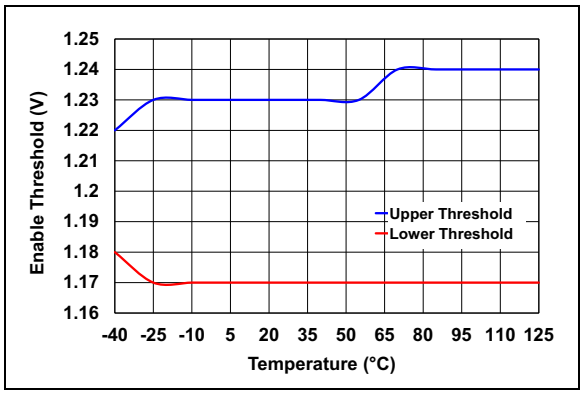


FIGURE 2-14: *Enable Threshold Voltage vs.Temperature.*

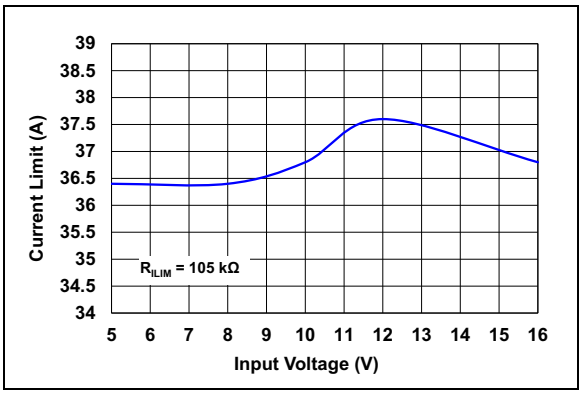


FIGURE 2-17: *Current Limit vs. Input Voltage.*

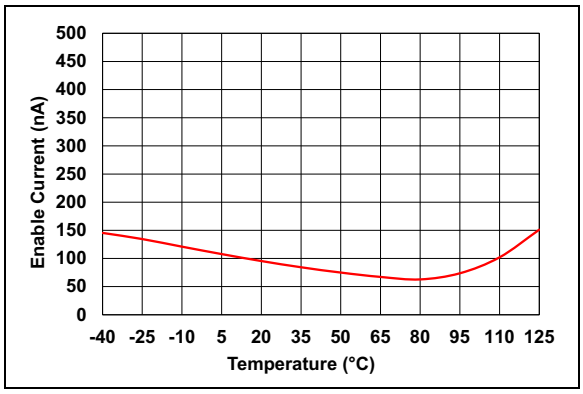


FIGURE 2-15: *Enable Current vs. Temperature.*

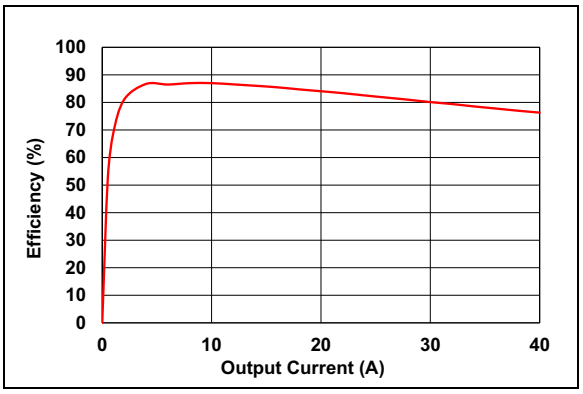


FIGURE 2-18: *Efficiency vs. Output Current.*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1.5V; f_{SW} = 500 kHz/phase; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C; C_{SS} = 20nF.

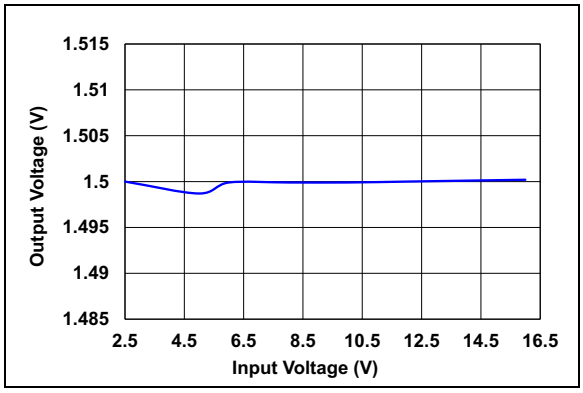


FIGURE 2-19: *Output Voltage vs. Input Voltage.*

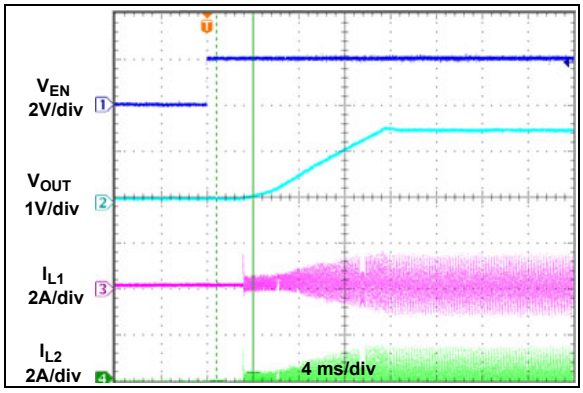


FIGURE 2-22: *Soft Start with Enable (I_{OUT} = 0A).*

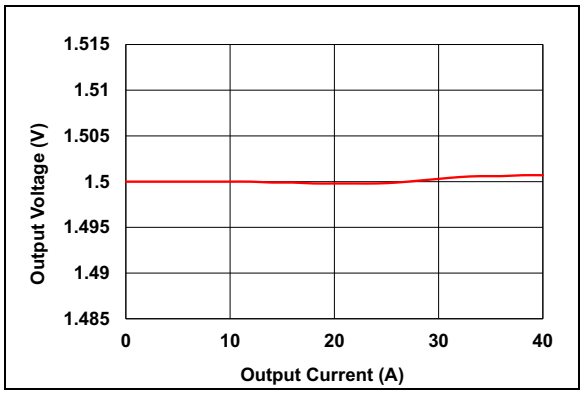


FIGURE 2-20: *Output Voltage vs. Output Current.*

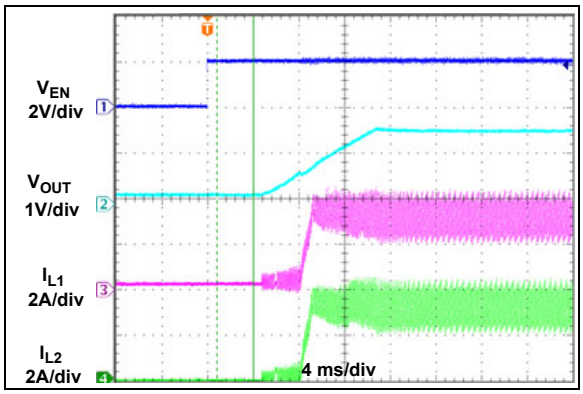


FIGURE 2-23: *Soft Start with Enable (I_{OUT} = 6A).*

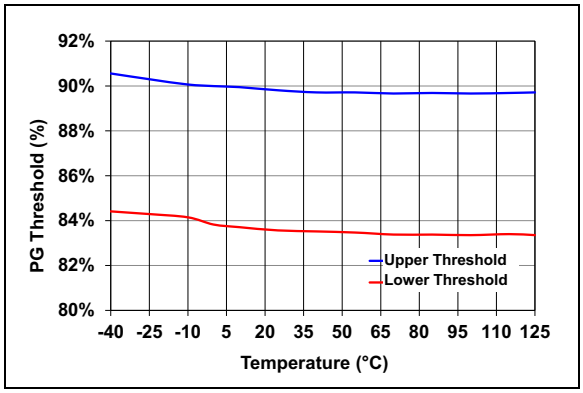


FIGURE 2-21: *PG Threshold vs. Temperature.*

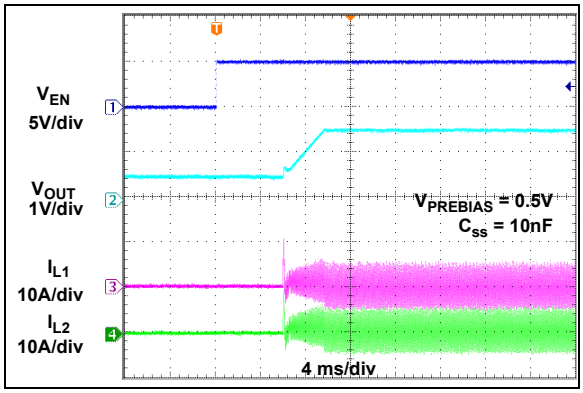


FIGURE 2-24: *Pre-Bias Start-up ($V_{PREBIAS}$ = 0.5V, I_{OUT} = 0A).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1.5V; f_{SW} = 500 kHz/phase; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C; C_{SS} = 20nF.

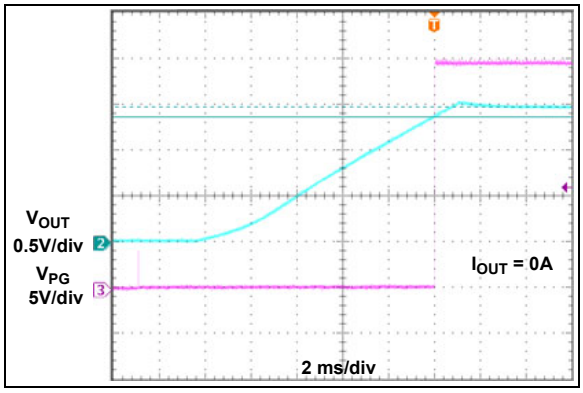


FIGURE 2-25: *Power Good Response.*

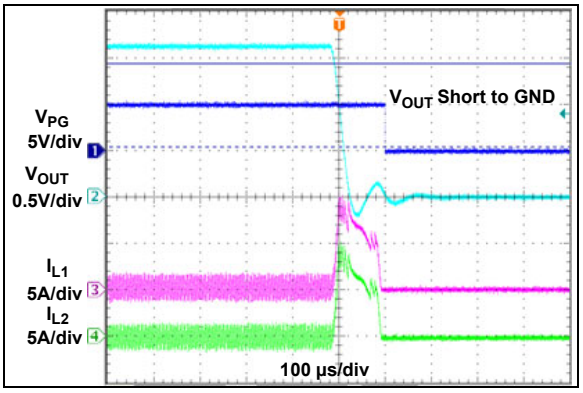


FIGURE 2-28: *Output Short.*

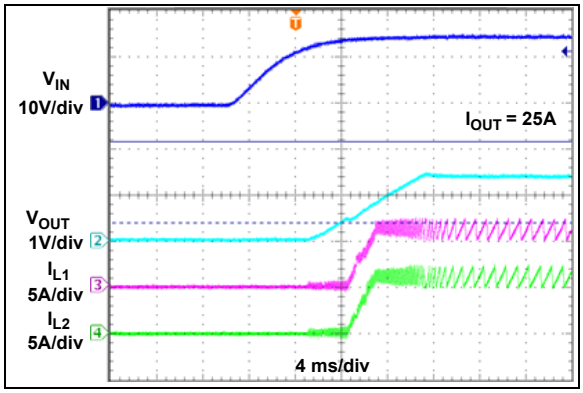


FIGURE 2-26: *V_{IN} Power-up with 25A Load.*

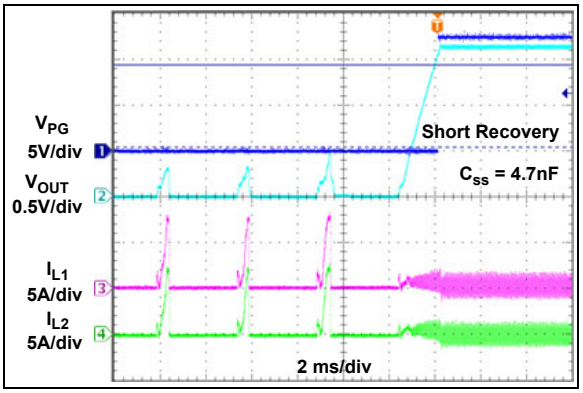


FIGURE 2-29: *Output Short Recovery.*

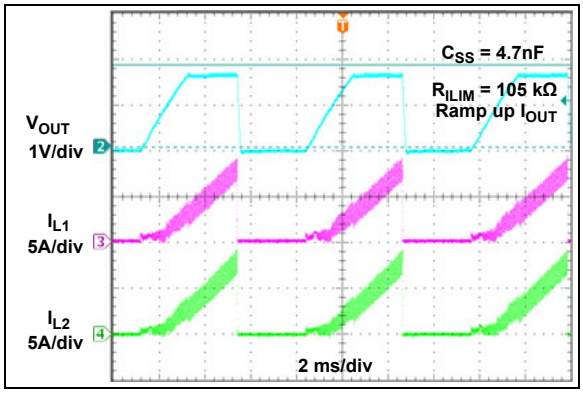


FIGURE 2-27: *Current Limit per Phase.*

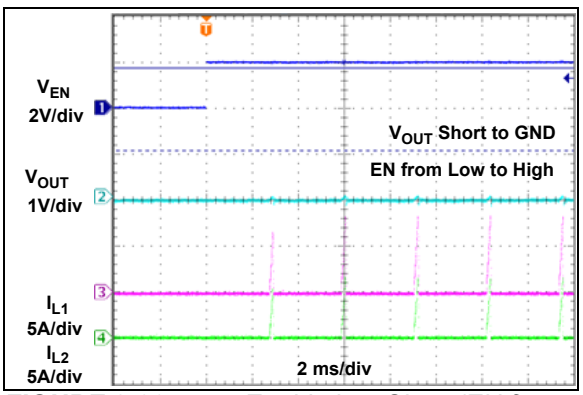


FIGURE 2-30: *Enable into Short (EN from Low-to-High).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1.5V; f_{SW} = 500 kHz/phase; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C; C_{SS} = 20nF.

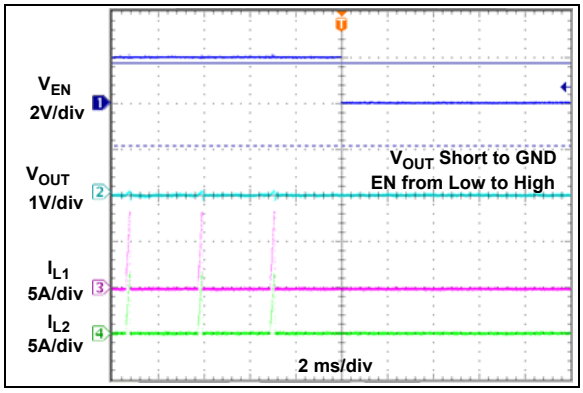


FIGURE 2-31: *Disable into Short (EN from High-to-Low).*

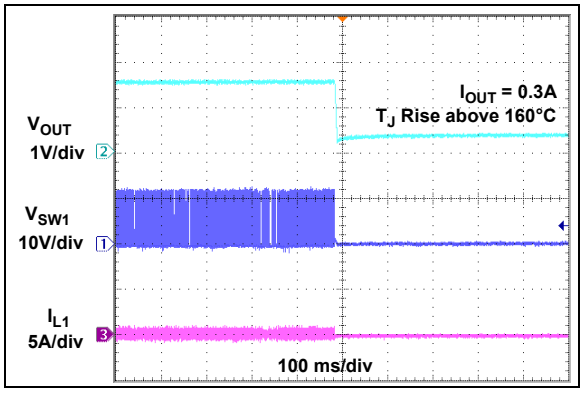


FIGURE 2-34: *Thermal Shutdown.*

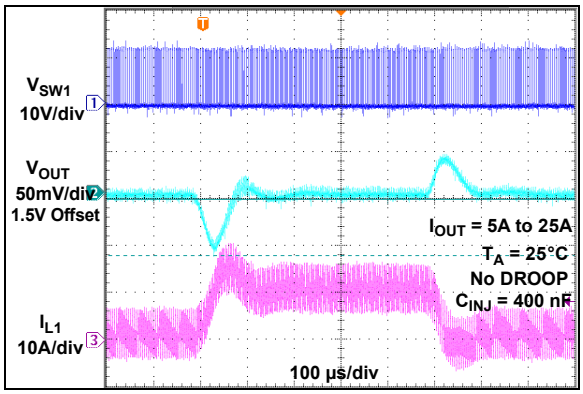


FIGURE 2-32: *Load Transient without Droop.*

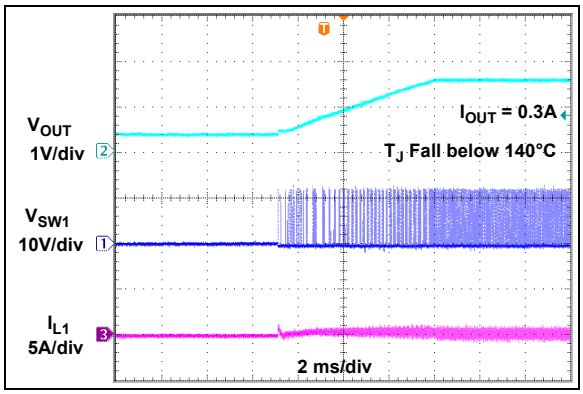


FIGURE 2-35: *Thermal Shutdown Recovery.*

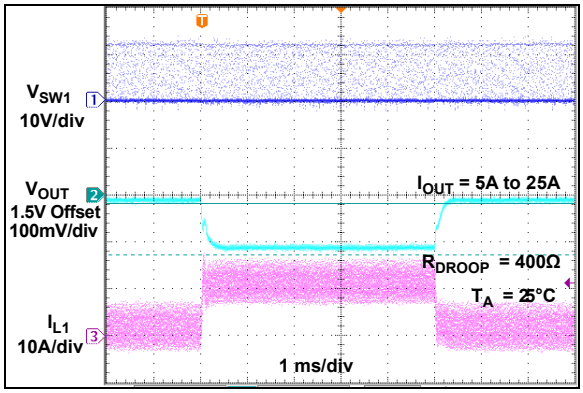


FIGURE 2-33: *Load Transient with Droop.*

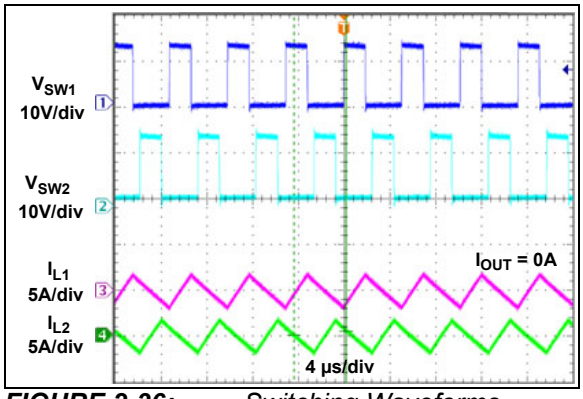


FIGURE 2-36: *Switching Waveforms Phasing (V_{OUT} = 5V, I_{OUT} = 0A).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1.5V; f_{SW} = 500 kHz/phase; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C; C_{SS} = 20nF.

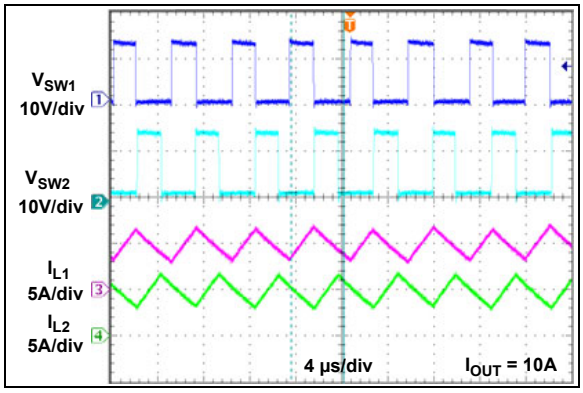


FIGURE 2-37: *Switching Waveforms Phasing (V_{OUT} = 5V, I_{OUT} = 10A).*

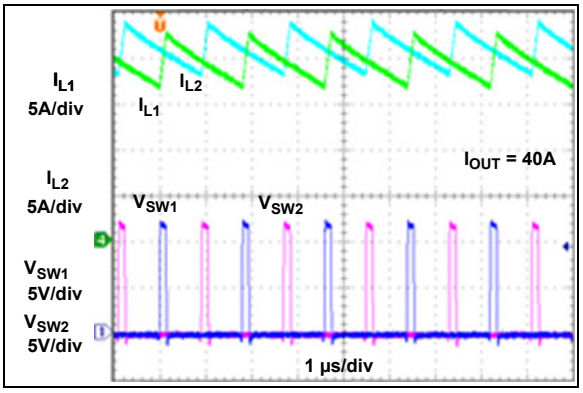


FIGURE 2-39: *Switching Waveforms Phasing and Current Sharing with R_{DSON} Sensing (I_{OUT} = 40A).*

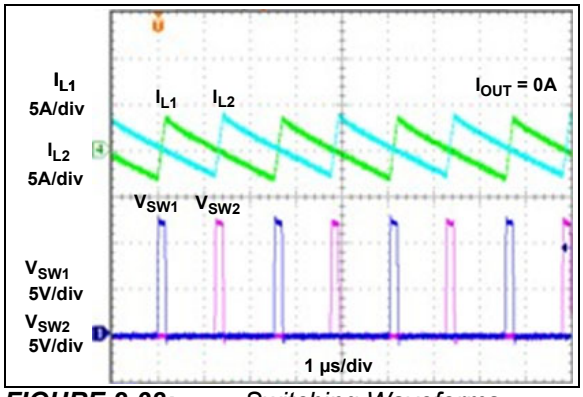


FIGURE 2-38: *Switching Waveforms Phasing and Current Sharing with R_{DSON} Sensing (I_{OUT} = 0A).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	CSN2	Current Sense Return pin for Phase 2. Connect Kelvin connection from the low-side FET source to CSN2 to avoid ground drops due to high current.
2	CSP2	Current Sense Positive pin for Phase 2. Connect Kelvin connection from the low-side FET drain to CSP2 to avoid ground drops due to high current.
3	CSN1	Current Sense Return pin for Phase 1. Connect Kelvin connection from the low-side FET source to CSN1 to avoid ground drops due to high current.
4	CSP1	Current Sense Positive pin for Phase 1. Connect Kelvin connection from the low-side FET drain to CSP1 to avoid ground drops due to high current.
5	ILIM	Current Limit Adjust Input pin. Connect a resistor from ILIM to AGND to set the current limit. Refer to **Section 4.5.2 "Current Limit"** for more details. Both channels share the same current limit threshold. When connected in a stackable application, all ILIM pins tied together, sharing common resistor sized for voltage drop, corresponding to current limit per phase.
6	CSH	Average Current Sense Voltage Output pin. Used for current sharing; see **Section 4.5.1 "Current Balancing Between Phases"** and **Section 4.5.9 "Adaptive Voltage Positioning (AVP), also Known as Droop Function (Recommended for CCM Only)"**. Connect 100 pF capacitor from CSH to AGND. In stackable application, tie all CSH pins together.
7	EN	Active-High Enable Input pin. 36V compatible with 1.2V precise threshold. Pull EN to GND to disable the buck converter output. Connect to VIN for always-on operation. EN can be used for power sequencing and as a UVLO adjustment input. For a precision UVLO, put an appropriately sized resistor divider from VIN to AGND and tie the midpoint to the EN pin.
8	VIN	Input Voltage to Controller pin. Connect to VIN through 1.21Ω resistor. Connect 1 µF capacitor from this pin to PGND.
9	VDD	5V LDO Output pin. Bias supply for the MIC21LV32 control logic circuit. Connect a minimum 2.2 µF low-ESR ceramic capacitor from VDD to AGND.
10	AGND	Analog Ground pin. Reference node for all control logic circuits inside the MIC21LV32. Connect AGND to PGND at one point.
11	EXTVDD	Auxiliary LDO Input pin. Connect to a supply higher than 4.7V (typ) to bypass the internal high-voltage 5V LDO or leave unconnected/connected to ground when the EXTVDD pin is not used. Connect a 2.2 µF low-ESR ceramic capacitor between EXTVDD and AGND. EXTVDD can be connected to an external supply.
12	NPI	Next Phase Input pin. Connect APO of previous MIC21LV32 to NPI for multiphase operation.
13	APO	Active Phase Output pin. Connect APO to the next MIC21LV32 NPI pin for multiphase operation.
14	ONR	On-Time Request pin. It is an input or an output pin. Connect the ONR pins of all MIC21LV32 devices connected for multiphase operation. It is an output for the host and an input for the secondaries. The ONR output on the host has a pull-up capability of ~1 kΩ. When FBS is connected to VDD, it is an input (secondary).
15	OUTS	Output Voltage Sense pin. It is required to connect the OUTS pin to output through a 10 kΩ resistor and decouple to ground with a 100 nF capacitor directly for $V_{OUT} \leq 5V$. For $V_{OUT} > 5V$, it is required to connect the OUTS pin through a resistive divider from V_{OUT} to AGND. The OUTS pin will set the correct frequency adaptive to the output voltage.
16	BST1	Phase 1 Bootstrap Capacitor and Diode Connection pin. The BST1 pin is the supply voltage for the Phase 1 high-side MOSFET driver. Connect the cathode of an external Schottky diode to the BST1 pin and the anode of the Schottky diode to PVDD. Connect a 0.1 µF low-ESR ceramic capacitor between the BST1 pin and the SW1 pin.
17	DH1	Phase 1 High-Side Gate Driver Output pin. Connect DH1 to the Phase 1 high-side MOSFET gate.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol	Description
18	SW1	Phase 1 Switch Node Output pin. Connect one terminal of the Phase 1 inductor to the SW1 node.
19	DL1	Phase 1 Low-Side Gate Driver Output pin. Connect DL1 to the Phase 1 low-side MOSFET gate.
20	PGND	Power Ground pin. PGND is the return path for the low-side MOSFET current and for the low-side MOSFET driver. Connect all the PGND pins together and connect to the power ground plane.
21	PVDD	PVDD is Supply pin for the Low-Side MOSFET Driver. Connect to VDD through a 2.2Ω series resistor. Connect a minimum 4.7 µF low-ESR ceramic capacitor from PVDD to PGND.
22	DL2	Phase 2 Low-Side Gate Driver Output pin. Connect DL2 to the Phase 2 low-side MOSFET gate.
23	SW2	Phase 2 Switch Node Output pin. Connect one terminal of the Phase 2 inductor to the SW2 node.
24	DH2	Phase 2 High-Side Gate Driver Output. Connect DH2 to the Phase 2 high-side MOSFET gate.
25	BST2	Phase 2 Bootstrap Capacitor and Diode Connection pin. The BST2 pin is the supply voltage input for the Phase 2 high-side MOSFET driver. Connect the cathode of an external Schottky diode to the BST2 pin and the anode of the Schottky diode to PVDD. Connect a 0.1 µF low-ESR ceramic capacitor between the BST2 pin and the SW2 pin.
26	PG	Open-Drain Power Good Output pin. PG is pulled to ground when the output voltage is below 80% of the target voltage. Pull-up to VDD through a 10 kΩ resistor to set logic high level when the output voltage is above 90% of the target voltage.
27	RIP_INJ	Ripple Injection Node pin. Connect series RC network from the RIP_INJ pin to FBS for injecting sufficient ripple for stable operation. Also connect a prepositioning resistor from this pin to GND, which sets the RIP_INJ pin voltage to its steady-state value. There is a 4.8 µA pull-up current when High-Z to preposition the common point of R_{INJ} and C_{INJ}.
28	FBS	Remote Feedback Input pin. Connect to the midpoint of a resistor divider from the output voltage to GFB to set the desired output voltage. Connect the FBS pin to VDD to configure MIC21LV32 as secondary in multiphase configuration.
29	GFB	Ground Feedback Remote Sense pin. Connect Kelvin sense directly across the output capacitor ground through the low-side FB resistor ground connection.
30	SS	Soft Start Adjustment pin. Connect a capacitor from the SS pin to AGND to adjust the soft start time. See more details in **Section 4.5.5 "Soft Start"**. Connect an optional resistor across the SS pin to AGND for overshoot reduction during soft start.
31	FREQ	Frequency Programming Input pin. Connect to ground through a resistor set to the same switching frequency for each phase.
32	DROOP	Analog Output DROOP pin. This pin is for implementing the "Adaptive Voltage Positioning" feature. Connect a resistor from the DROOP pin to the feedback resistor divider. The DROOP voltage is proportional with inductor current for load currents greater than 0A.
—	EP	Exposed Pad pin. Connect it to AGND.

4.0 FUNCTIONAL DESCRIPTION

4.1 Control Architecture

The MIC21LV32 is an adaptive on-time, dual phase, synchronous step-down DC/DC controller. It is designed to operate over a wide 4.5V to 36V input voltage range and provides a regulated output voltage at up to 50A of output current. An adaptive on-time control scheme is employed in order to obtain a constant switching frequency and simplify the control compensation.

The MIC21LV32 has a differential remote sense amplifier with unity gain for sensing output voltage. The amplifier helps regulate the output voltage at target level over the entire load range by avoiding parasitic voltage drops on the PCB. The output of the differential amplifier will be used as output voltage to the controller. The output voltage is sensed across the MIC21LV32 device's feedback remote sense FBS pin and ground feedback remote sense GFB pin via the voltage divider, and compared to a 0.6V Reference Voltage, V_{REF}, at a low-gain transconductance (g_m) amplifier. The output of the g_m amplifier, V_{gm}, is then further compared with another 1.2V reference, V_{REF_COM}, at the error comparator. If the feedback voltage decreases and the output of the g_m amplifier is below 1.2V, then the error comparator will trigger the control logic and generate an on-time period. The on-time period length is predetermined by the T_{ON1} and T_{ON2} generation circuitries for Phase 1 and Phase 2, respectively.

EQUATION 4-1:

$$T_{ON(EST)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT} = Output Voltage

V_{IN} = Power Stage Input Voltage

f_{SW} = Switching Frequency of Each Phase

The internal logic starts maintaining the same switching frequency and phasing for each phase (180° for two phases; for stackable applications, 90° for four phases; 60° for six phases; 45° for eight phases).

Figure 4-1 shows the MIC21LV32 control loop timing during steady-state operation. During steady-state operation, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the external ripple from the RIP_INJ pin, injected to the FBS node at the turn-on instant of each phase. When the output of the g_m error amplifier falls below the reference voltage, an on-time period is triggered. The on-time of Phase 1 is determined by the T_{ON1} generator. The Phase 1 T_{ON1} generator also includes current sharing error between phases. The Phase 1 high-side driver turns on the Phase 1 high-side FET during T_{ON1}. The Phase 1 high-side FET turn-off instant depends on both the T_{ON} estimation and current sharing error. At the end of Phase 1 T_{ON1}, the internal high-side driver turns off the Phase 1 high-side FET and the low-side driver turns on the Phase 1 low-side FET. The Phase 1 off-time period length depends upon the feedback voltage error in the next cycle for Phase 1. When the output of the g_m error amplifier falls below the reference voltage in the second cycle, the Phase 2 on-time period is triggered. The on-time of Phase 2 is determined by the T_{ON2} generator. The Phase 2 T_{ON2} generator also includes current sharing error between phases. The Phase 2 high-side driver turns on the Phase 2 high-side FET during T_{ON2}. The high-side FET turn-off instant depends on both the T_{ON} estimation and current sharing error. At the end of Phase 2 T_{ON2}, the internal high-side driver turns off the Phase 2 high-side FET and the low-side driver turns on the Phase 2 low-side FET. The duration of the Phase 2 off-time period depends upon the feedback voltage error in the next Phase 2 cycle. The above cycles repeat in a daisy-chain ring, and both phases support the load current alternately and maintain output voltage. In steady state, $T_{ON1} = T_{ON2}$, $T_{OFF1} = T_{OFF2}$ and this way, the resulting phase difference is 180 degrees. For a stackable configuration of four phases in a similar way, $T_{ON1} = T_{ON2} = T_{ON3} = T_{ON4}$ and $T_{OFF1} = T_{OFF2} = = T_{OFF3} = T_{OFF4}$ generates a 90 degree phasing.

If the off-time period determined by the feedback voltage is less than the Minimum Off-Time, $T_{OFF(MIN)}$, which is about 360 ns, then the MIC21LV32 control logic will apply the $T_{OFF(MIN)}$ instead to either phase. The minimum $T_{OFF(MIN)}$ period is required to maintain enough energy in the Boost Capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 360 ns $T_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{T_S - T_{OFF(MIN)}}{T_S} = 1 - \frac{360\ ns}{T_S}$$

Where:

T_S = $1/f_{SW}$

It is not recommended to use the MIC21LV32 with an off-time close to $T_{OFF(MIN)}$ during steady-state operation. Equation 4-2 should be used to choose the T_S for a lower switching frequency when the D_{MAX} is reached, if VIN is very close to V_{OUT}, knowing that the buck converter duty cycle equals V_{OUT} divided by V_{IN}.

The actual on-time and the resulting switching frequency will vary with the part–to–part variation in the rise and fall times of the external MOSFETs, the output load current and the variations in the V_{DD} voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 28V to 1.0V.

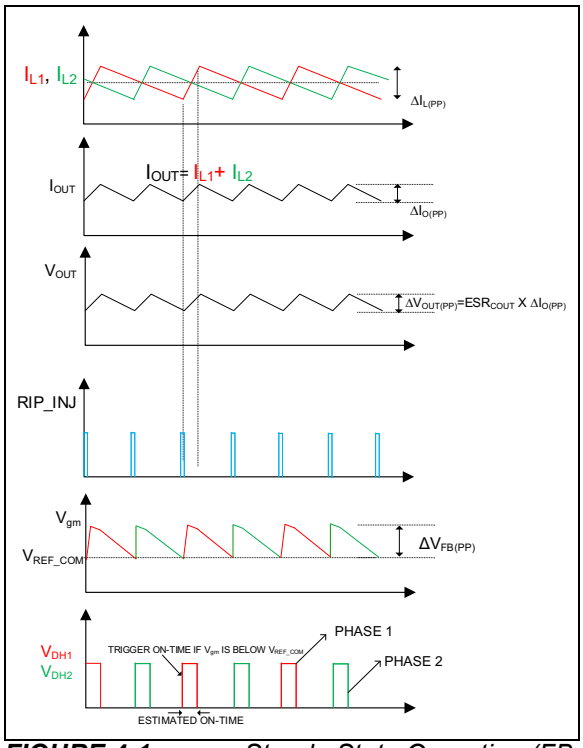


FIGURE 4-1: *Steady-State Operation (FB Ripple Shows Injected and ESR Ripple Only, Reactive Impedances Neglected).*

Figure 4-2 shows the operation of the MIC21LV32 during load transient. The output voltage drops due to the sudden load increase, which causes the V_{FBS} to decrease and the output voltage of the g_m amplifier, V_{gm}, to be less than V_{REF_COM}. This will cause the error comparator to trigger an on-time period. At the end of the on-time period, a Minimum Off-Time, $T_{OFF(MIN)}$, is generated to charge C_{BST}, since the feedback voltage is still below V_{REF}. Then, the next on-time period is triggered and applies D_{MAX} due to the low feedback voltage. Therefore, the switching frequency changes during the load transient to deliver D_{MAX} and zero duty cycle when high-current load disappears for both phases, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC21LV32 converter. The phases will overlap during load transient until the output voltage error is corrected. The transient response is shown in Figure 4-3.

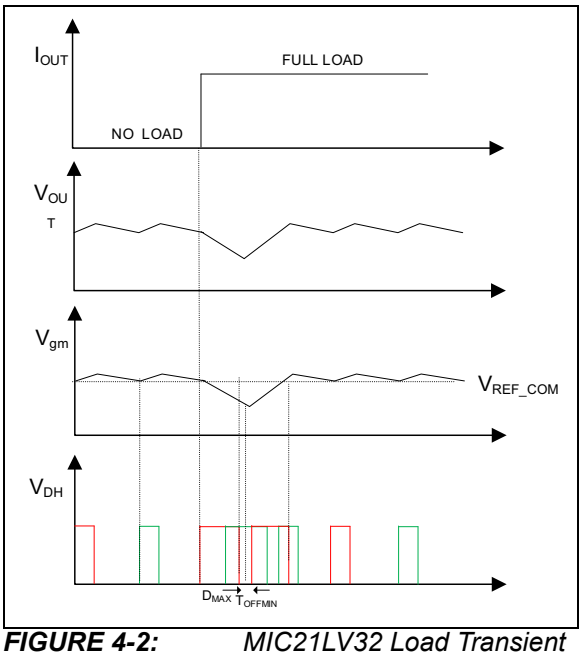


FIGURE 4-2: *MIC21LV32 Load Transient Response Timing.*

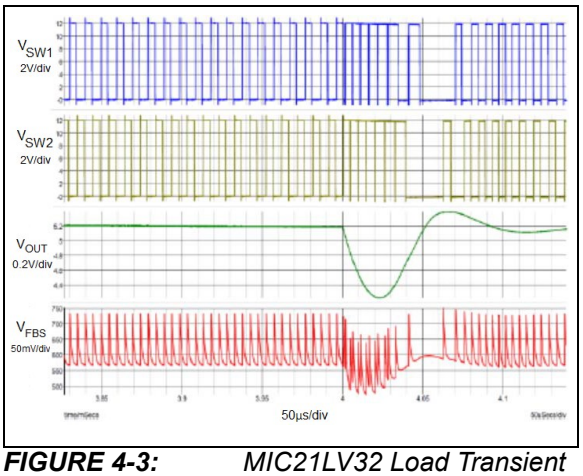


FIGURE 4-3: *MIC21LV32 Load Transient Response.*

Unlike true Current-mode control, the MIC21LV32 uses the output voltage ripple to trigger an on-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. In order to meet the stability requirements, the MIC21LV32 feedback voltage ripple must be in phase with the inductor current ripple, and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV to 100 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation.

4.2 Start-up Into Pre-Bias Load

To get proper pre-bias start-up performance, the voltage at the junction of C_{INJ} and R_{INJ} needs to be at its steady-state value when the device starts switching. This is done by biasing the RIP_INJ pin voltage using a current source (I_{BIAS}) at the RIP_INJ pin and a resistor (R_{BIAS}) at the RIP_INJ pin before the device starts switching. The Injection (INJ) driver will be in High-Impedance mode before the device starts switching. This results in a voltage equal to $I_{BIAS} \times R_{BIAS}$ at the RIP_INJ pin before switching starts. This voltage charges the C_{INJ} cap to the value of $I_{BIAS} \times R_{BIAS}$. As the C_{INJ} takes time to charge to the final voltage, depending on the $C_{INJ} \times (R_{INJ} + R_{FB(BOT)})$, the I_{BIAS} must be enabled before the switching starts. The MIC21LV32 has a POK delay of ≈4 ms (i.e., when EN is high, the device starts switching after ≈4 ms). Therefore, this 4 ms delay is enough to charge C_{INJ} to the final value. Once the device starts switching, the I_{BIAS} will no longer have any effect as the ripple injection driver will be either high or low (the ripple injection driver will not be in High-Impedance mode when the device starts switching).

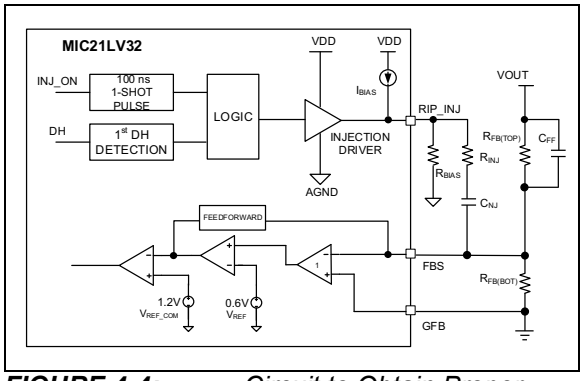


FIGURE 4-4: *Circuit to Obtain Proper Pre-Bias Start-up Performance and Ripple Injection.*

I_{BIAS} is an internal current source. R_{BIAS} is an external resistor from RIP_INJ to AGND. R_{BIAS} can be calculated using the formula below:

EQUATION 4-3:

$$R_{BIAS} = \frac{5V \times 100\ ns \times f_{SW}}{I_{BIAS}}$$

Where:

$5V \times 100\ ns \times f_{SW}$ = Average Voltage on the RIP_INJ Pin

Note that as R_{BIAS} is always present, it draws an additional current from the INJ driver when the RIP_INJ pin is 5V for 100 ns. This adds to the device's I_Q. However, its contribution to the device's I_Q will be low because this current will be present for 100 ns only.

4.3 Stability Analysis

The MIC21LV32 uses ripple-based constant on-time architecture to generate switching pulses. The magnitude of the ripple needs to be in the range of 20 mV to 70 mV. In order to avoid ripple voltage variation with input voltage, ripple voltage is injected from the third node through the RIP_INJ pin. Figure 4-5 shows the ripple injection at the FBS node with respect to the reference voltage.

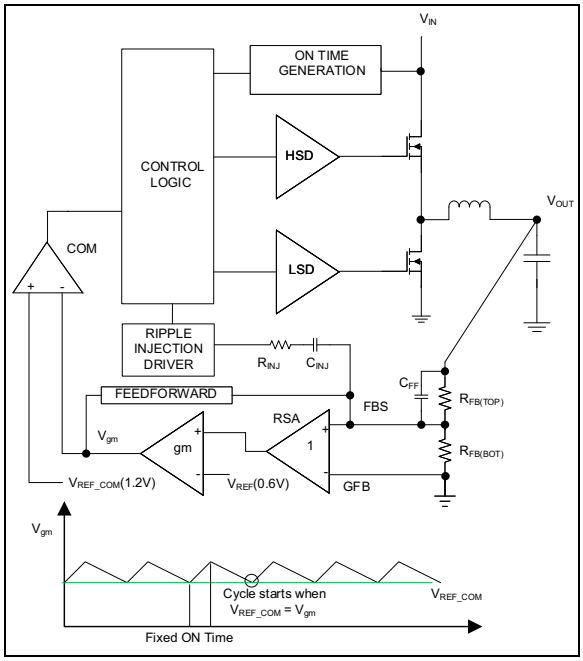


FIGURE 4-5: *MIC21LV32 Ripple Injection at FBS Node.*

The output capacitors generally have three components. The capacitive ripple lags the inductor current ripple. The ESR ripple is in phase with the inductor current. The ESL ripple effect is minimal in low-voltage capacitors.

4.4 Ripple Injection Circuit Components Selection

Follow the steps below for selecting the ripple injection circuit components if low-ESR output capacitors are used. The below procedures provide a good starting point for selecting the ripple injection components. Final values should be confirmed by laboratory measurements.

1. Calculate the product of R_{INJ} and C_{FF} for a given injected Feedback Ripple Voltage, ΔV_{FB}, using the equation below. Choose ΔV_{FB} in the range of 40 mV to 500 mV. A good starting point for ΔV_{FB} is 50 mV.

EQUATION 4-4:

$$R_{INJ} \times C_{FF} = \frac{5V \text{ x } 100 \text{ ns}}{\Delta V_{FB}}$$

Where:

ΔV_{FB} = Injected Feedback Ripple Voltage

2. Choose C_{FF} in the range of 0.47 nF to 10 nF.
3. Calculate R_{INJ} using the equation above.
4. Calculate the Top Feedback Resistor, $R_{FB(TOP)}$, value using the equation below:

EQUATION 4-5:

$$R_{FB(TOP)} \geq \frac{1}{2 \times \pi \times C_{FF} \times 0.8 \times f_{LC}}$$

Where:

f_{LC} = LC Resonant Frequency = 1/(2 x π x sqrt (L x C_{OUT})

5. Calculate Bottom Feedback Resistor, $R_{FB(BOT)}$, value using the equation below:

EQUATION 4-6:

$$R_{FB(BOT)} = \frac{R_{FB(TOP)}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]}$$

Where:

V_{OUT} = Target Output Voltage

V_{REF} = Reference Voltage = 0.6V for MIC21LV32

6. Estimate the crossover frequency using the equation below. If $f_{CO(EST)}$ is above $f_{SW}/5$, lower the C_{FF} value and repeat procedure 6.

EQUATION 4-7:

$$f_{CO(EST)} = \frac{R_{INJ} \times C_{FF}}{\pi \times L \times C_{OUT}} \times \frac{V_{OUT} \times 10^6}{f_{SW}}$$

Where:

L = Inductance

C_{OUT} = Output Capacitance

V_{OUT} = Output Voltage

f_{SW} = Switching Frequency

7a) Select C_{INJ} using the below equation if $f_{CO(EST)}$ calculated above meets Equation 5-11.

EQUATION 4-8:

$$C_{INJ} \geq \frac{1}{0.8 \times R_{INJ} \times f_{CO(EST)}}$$

Add a resistor in parallel with the soft start capacitor connected to the SS pin if $C_{INJ} > C_{FF} \times (R_{FB(TOP)}/R_{FB(BOT)})$. This ensures that there is no overshoot at the end of the soft start. Use Equation 4-9 below to select the parallel resistor value.

EQUATION 4-9:

$$R_{SS} \geq \frac{0.8V}{I_{SS}}$$

Where:

I_{SS} = Soft Start Current Source = 1.2 µA

h) Select C_{INJ} using the below guidelines if $f_{CO(EST)}$ is low (typically below $f_{SW}/15$) when f_{CO} is limited by the minimum ΔV_{FB} required in lower V_{OUT} applications. Assume $f_{CO} = f_{SW}/10$. Calculate the maximum Equivalent Series Resistance (ESR) of the output capacitor using Equation 4-10.

EQUATION 4-10:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT\_TRANS}}{\Delta I_{LOAD\_STEP}}$$

Where:

ΔI_{LOAD_STEP} = Magnitude of the Load Transient

ΔV_{OUT_TRANS} = Acceptable Output Voltage Deviation during Load Transient

Calculate the output capacitance using Equation 4-11.

EQUATION 4-11:

$$C_{OUT} \geq \frac{1}{\pi \times f_{CO} \times ESR_{COUT}}$$

Calculate C_{INJ} using Equation 4-12.

EQUATION 4-12:

$$C_{INJ} = C_{FF} \times \frac{ESR_{COUT}}{2 \times \pi \times f_{CO} \times L} \times \frac{V_{OUT}}{5V \times 100\ ns \times f_{SW}}$$

Using too low a C_{INJ} may result in oscillations at the beginning of the soft start. These oscillations can be reduced either by using a higher C_{INJ} or C_{OUT}, by reducing the feedback ripple.

4.5 Detailed Device Description

The MIC21LV32 always operates in CCM and both phases support the load current equally at high loads.

4.5.1 CURRENT BALANCING BETWEEN PHASES

One important benefit of the two-phase operation is the thermal advantage gained by distributing the heat over multiple devices and a greater PCB area. By doing this, the system designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heatsinks.

In order to achieve the thermal advantage, it is important that each phase carries the same amount of current at any load level. In the MIC21LV32, both phase currents are sensed across the low-side MOSFET,

$R_{DS(ON)}$, during off-time. The low-side MOSFET current is tracked during off-time and held close to peak value in the valley point. The average current information is generated by summing all the phases' sensed currents and dividing by the number of phases (two for two phases). An error current per phase is generated by making the difference between the average current information and each phase current, which is used to modulate T_{ON1} and T_{ON2} in order to cancel the error in the current sharing.

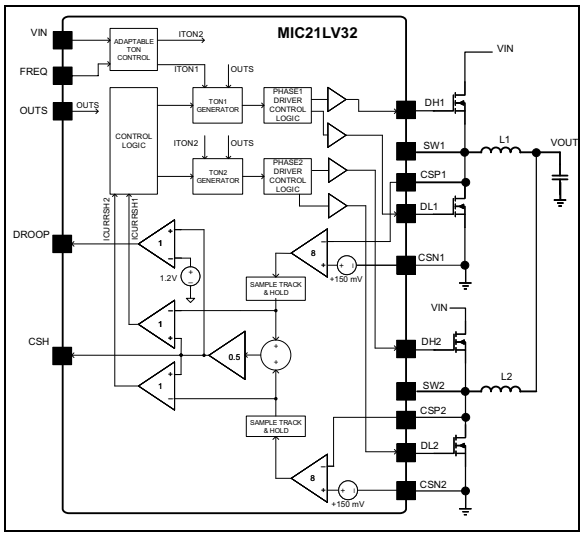


FIGURE 4-6: *MIC21LV32 Current Sharing Circuit.*

4.5.2 CURRENT LIMIT

The MIC21LV32 uses the R_{DSON} of the external low-side power MOSFET to sense overcurrent conditions or a sense resistor inserted with the source of the bottom FET can be used for more accurate results and not requiring temperature compensation. The bottom FET R_{DSON} sensing method will avoid adding cost, use of additional board space and power losses taken by a discrete current sense resistor.

The current limit threshold can be programmed by _connecting a resistance from the ILIM pin to AGND. Both phases use the same current limit threshold.

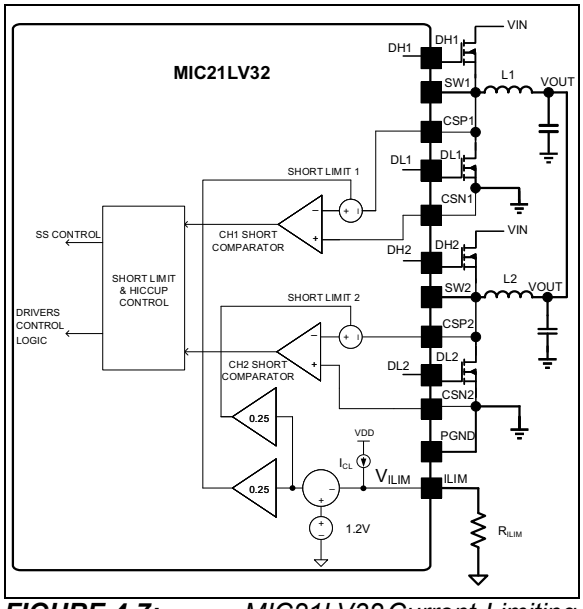


FIGURE 4-7: *MIC21LV32 Current-Limiting Circuit.*

The MIC21LV32 forces a constant 9.6 µA current through the ILIM setting resistor, tied from the ILIM pin to AGND to program V_{ILIM}.

In each switching cycle of both phases of the MIC21LV32 converter, the inductor valley current is sensed by monitoring the V_{DS} voltage across the low-side MOSFET during the off period. There is a 150 ns (typical) blanking period before each current sense signal is considered for protection. The blanking period improves noise immunity. If the valley low-side MOSFET current is greater than the current limit threshold current for seven consecutive cycles in either phase, then the MIC21LV32 turns off the high-side and low-side MOSFETs of both phases and a soft start sequence is triggered after the hiccup timer has expired. This mode of operation is called Hiccup mode and its purpose is to protect the downstream load in case of a hard short. Figure 4-8 illustrates the MIC21LV32 operation during overload conditions. When the load current is increased gradually, the inductor current also increases, as shown in Figure 4-8. When the load current is around the current limit threshold, the high-side and low-side MOSFET current can be higher than the current limit, as highlighted in Figure 4-8 as Case#1. In Case#1, even though the low-side MOSFET instantaneous current exceeds the current limit threshold for some duration, the low-side MOSFET current is lower than the current limit at the end of the 150 ns blanking time. This causes the MIC21LV32 to not enter the current limit protection and initiate the next high-side MOSFET turn-on cycle. After the high-side MOSFET is turned on, the current ramps up to a value that is determined by the operating duty cycle and inductor value. When the high-side MOSFET is turned off and the low-side MOSFET is turned on, as shown as Case#2 in Figure 4-8, the

current through the low-side MOSFET is higher than the current limit after the blanking time of 150 ns for seven consecutive cycles. This causes the MIC21LV32 to enter the current limit protection. As shown in Figure 4-8, the inductor valley current is higher than the current limit threshold as the MIC21LV32 senses the low-side MOSFET current.

When the MIC21LV32 enters current limit protection, both the high-side and low-side MOSFETs are turned off for both phases for a hiccup time-out of 2 ms. The inductor current flows through the body diode of the low-side MOSFET for each phase until it falls down to zero. The MIC21LV32 initiates the soft start after the hiccup time-out, as shown in Figure 4-8.

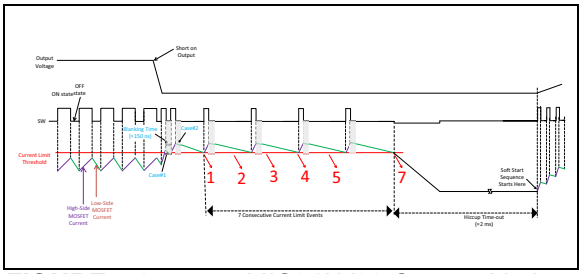


FIGURE 4-8: *MIC21LV32 Current Limit Threshold Relationship to Output Current.*

When multiple MIC21LV32 devices are connected in parallel to support higher load current, all ILIM pins are connected together and one resistor is connected from ILIM to AGND to set the current limit. Only the host device forces the 9.6 µA current from the ILIM pin. The secondaries do not force any current, they just read V_{ILIM}. All phases share the same V_{ILIM} value under stackable phase configuration.

The MIC21LV32 current limit needs to be temperature-insensitive when precise sense resistors or R_{DSON} of the low-side MOSFETs are used.

Since the R_{DSON} resistance increases to about two times, from 25°C to 125°C, an external NTC resistor is required to program the current limit in this case. In case regular precise sense resistors are used, no NTC resistance is needed.

To realize a positive temperature coefficient from the negative temperature coefficient of the NTC resistance, the current limit per phase was internally generated, as shown in Equation 4-13.

EQUATION 4-13:

$$I_{LIM} = \frac{0.3 - 0.25 \times V_{ILIM}}{R_{DSON}}$$

Where:

I_{LIM} = Desired Current Limit per Phase

V_{ILIM} = Programmable Voltage at ILIM Pin

From Equation 4-13, one can derive the V_{ILIM} value through Equation 4-14.

EQUATION 4-14:

$$V_{ILIM} = 1.2V - 4 \times R_{DSON} \times I_{LIM}$$

To program the target V_{ILIM} voltage, Equation 4-15 is used.

EQUATION 4-15:

$$V_{ILIM} = I_{CL} \times R_{ILIM}$$

Where:

I_{CL} = 9.6 µA (typical) Constant-Current Source at ILIM Pin

R_{ILIM} = Current Limit Threshold Voltage Programming Resistance

EXAMPLE 4-1: CALCULATION OF R_{ILIM} FOR BOTTOM MOSFET R_{DSON} CURRENT SENSING

- For I_{LIM} = 10A per phase, R_{DSON} = 10 mΩ at 25°C; using Equation 4-14, V_{ILIM} = 1.2V – 4 * 10 mΩ * 10A = 1.2V – 0.4V = 0.8V at 25°C.
- To get 0.8V on the ILIM pin with a 9.6 µA constant current source, we need a programming equivalent resistance of R_{ILIM} = 0.8V/9.6 µA = 83.3 kΩ at 25°C.
- If the temperature increases to 125°C, then R_{DSON} at 125°C = 20 mΩ at the same 10A limit.
- Therefore, V_{ILIM} = 1.2V – 4 * 20 mΩ * 10A = 1.2V – 0.8V = 0.4V at 125°C. Then, R_{ILIM} = 0.4V/9.6 µA = 41.7 kΩ at 125°C.

As shown in Example 4-1, the sizing of current limit per phase needs to be verified over temperature in order to make sure Equation 4-13 and Equation 4-14 work correctly, because it is necessary to always have:

EQUATION 4-16:

$$1.2V > 4 \times R_{DSON} \times I_{LIM}$$

For linearization and fitting the temperature coefficient of the bottom MOSFET R_{DSON}, a resistance network from the ILIM pin to AGND, used with an NTC resistor, is shown in Figure 4-9.

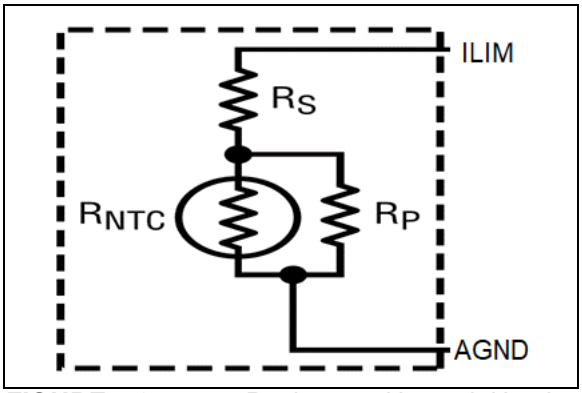


FIGURE 4-9: *Resistance Network Used with R_{NTC} Resistor for Linearization and Fitting the Temperature Coefficient of MOSFET R_{DSON}.*

In case a temperature-independent resistor sensing is used, a simple temperature constant standard resistance is used on the ILIM pin.

4.5.3 NEGATIVE CURRENT LIMIT

The MIC21LV32 supports a cycle-by-cycle negative current limit. The absolute value of the negative current-limiting threshold is 50% of the programmed current limit. If the negative low-side MOSFET current is going to trigger a negative current limit, the low-side MOSFET will be turned off and allow current through the high-side MOSFET body diode. During this time, the output voltage tends to rise, because this protection limits the current to discharge the output capacitor. In order to prevent a huge reverse current over the short limit value, the low-side FET turns on after 500 ns, maintaining negative current at programmed level.

4.5.4 PRECISION ENABLE (EN)

The precision Enable (EN) input is used to control the regulator. The precision feature allows the simple sequencing of multiple power supplies with a resistor divider from another supply. Connecting this pin to ground, or to a voltage lower than 1.2V (typ.), will turn off the regulator. In this state, the current drain from the input supply is 25 µA (typical) at a 12V input voltage.

The EN input has an internal pull-up of about 6 µA. Therefore, this pin can be left floating or pulled to a voltage greater than 1.2V (typical) to turn the regulator on. The hysteresis on this input is about 65 mV (typical) below the 1.2V (typical) threshold. When driving the enable input, the voltage must never exceed the absolute maximum specification for this pin. Although an internal pull-up is provided on the EN pin, it is a good practice to pull the input high when this feature is not used, especially in noisy environments. This can be done easily by connecting a high-value resistor (1 MΩ) between the VIN and EN pins. The MIC21LV32 device also incorporates an internal input Undervoltage Lockout (UVLO) feature. This prevents the regulator from turning on when the input voltage is not high enough to properly bias the internal circuitry. The rising threshold is 4.3V (typ.) while the falling threshold is 3.9V (typ). In some cases, these thresholds may be too low to provide good system performance. The solution is to use the EN input as an external programmable input UVLO to disable the part when the input voltage falls below a target lower threshold. This is often used to prevent excessive battery discharge or early turn-on during start-up. This method is also recommended to prevent abnormal device operation in applications where the input voltage falls below the minimum of 4.5V. Figure 4-10 shows the connections to implement this method of UVLO. Equation 4-17 and Equation 4-18 can be used to determine the correct resistor values.

EQUATION 4-17:

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{OFF}}{V_{ENTH} - V_{ENHYS}} - 1 \right)$$

Where:

R_{TOP} = Top Resistor of the VIN Voltage Resistor Divider

R_{BOT} = Bottom Resistor of the VIN Voltage Resistor Divider

V_{OFF} = Target VIN Voltage Below which the Regulator Turns Off

V_{ENTH} = Device Enable Upper Threshold Voltage

V_{ENHYS} = Enable Threshold Hysteresis

EQUATION 4-18:

$$V_{ON} = V_{OFF} \times \frac{V_{ENTH}}{V_{ENTH} - V_{ENHYS}}$$

Where:

V_{OFF} = Input Voltage where the Regulator Shuts Off

V_{ON} = Input Voltage where the Regulator Turns On

V_{ENHYST} = Enable Threshold Hysteresis

V_{ENTH} = Enable Upper Threshold Voltage

Due to the 6 µA pull-up, the current in the divider must be much higher than this. A value of 20 kΩ for R_{BOT} is a good first choice.

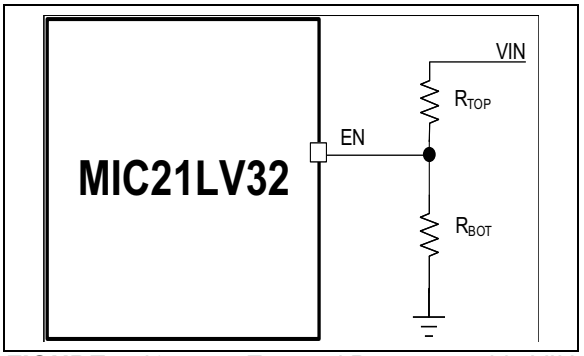


FIGURE 4-10: *External Programmable VIN UVLO Connections.*

4.5.5 SOFT START

Soft start reduces the power supply input surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC21LV32 features adjustable soft start time. The soft start time can be adjusted by changing the value of the capacitor connected from the SS pin to AGND. The MIC21LV32 forces 1.2 µA current from the SS pin. This constant current flows through the soft start capacitor connected from the SS pin to AGND in order to adjust the soft start time.

The soft start capacitor value for the desired V_{OUT} ramp-up time can be calculated from Equation 4-19.

EQUATION 4-19:

$$C_{SS} = \frac{1.2\ \mu A \times t_{SS}}{V_{REF}}$$

Where:

t_{SS} = Output Voltage Soft Start Ramp-up Time

4.5.6 VDD REGULATOR AND EXTVDD LDO

The MIC21LV32 has an integrated high-voltage LDO that provides a 5V regulated output from Input Voltage, V_{IN}, ranging from 5.5V to 36V. When V_{IN} < 5.5V, V_{DD} must be tied to the VIN pins to bypass the internal linear regulator. The internal LDO powers the control circuitry from the VDD pin and gate drive current from the PVDD pin.

The MIC21LV32 also features an auxiliary low-voltage LDO, which is powered by EXTVDD. When the voltage on the EXTVDD is at 4.7V (typical) or higher, this auxiliary LDO is enabled and powers all the internal circuitry. At the same time, the main high-voltage LDO is disabled. This increases the efficiency of the system by reducing the differential voltage across the high-voltage LDO, hence reducing the power losses in the LDO. In general, the output of the buck converter is used as the power supply for the auxiliary LDO by connecting the EXTVDD pin to the output of the buck converter. The maximum voltage that can be applied at EXTVDD is limited to 14V. Figure 4-11 shows the internal 5V LDO and EXTVDD connection in the MIC21LV32.

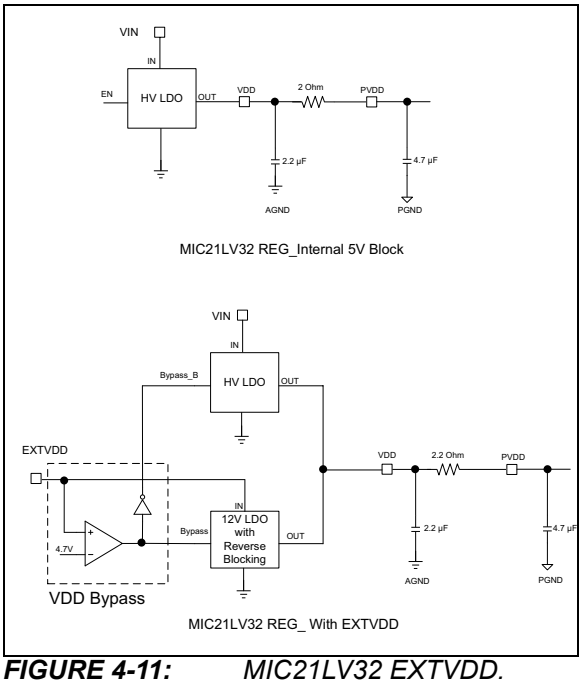


FIGURE 4-11: *MIC21LV32 EXTVDD.*

Given that the EXTVDD is powered from the V_{OUT} of the buck regulator, the V_{OUT} is noisy if there is a fast changing load. When V_{OUT} > 5V + $V_{DROPOUT}$, the noise could be suppressed by a loop of 12V LDO. However, when V_{OUT} = 5V, the 12V LDO works in Dropout mode; there is no loop gain. The LDO acts just like a resistor. It is not recommended to connect EXTVDD to V_{OUT} if V_{OUT} < 5V.

4.5.7 POWER GOOD (PG)

The Power Good (PG) pin is an open-drain output, which indicates logic high when the output is nominally over 88% of its steady-state voltage. A pull-up resistor of more than 10 kΩ should be connected from PG to VDD. During soft start, the PG is held low and is allowed to be pulled high after V_{OUT} is achieved over 88% of the target level.

4.5.8 SEQUENCING

The MIC21LV32 has a precision enable function. The EN pin voltage will either enable/disable switching. When the EN pin voltage is higher than 1.2V (typical), the MIC21LV32 is put into operation. The internal regulator will power up and start switching. Figure 4-12 shows the EN pin sequencing.

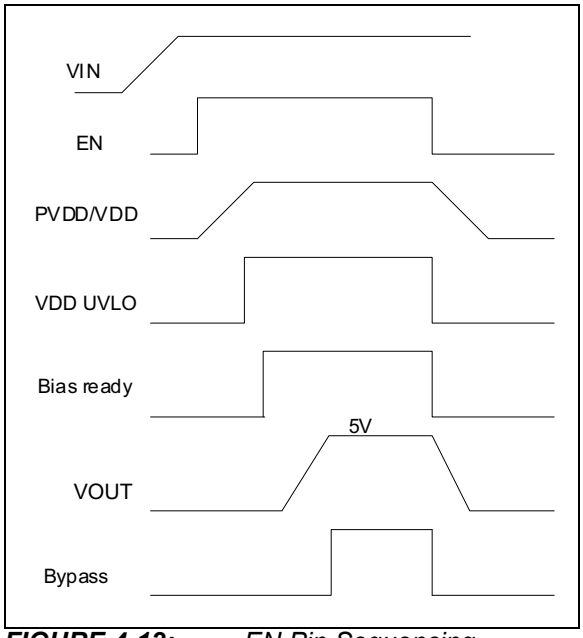


FIGURE 4-12: *EN Pin Sequencing.*

When the EN pin voltage is below the lower EN threshold, the MIC21LV32 goes into Shutdown mode. When in Shutdown mode, the MIC21LV32 stops switching and all internal control circuitry switches off to reduce the quiescent current. The EN pin, along with the PGOOD pin, can be used for sequencing multiple MIC21LV32 devices. It is recommended to power up VIN before the EN signal.

4.5.9 ADAPTIVE VOLTAGE POSITIONING (AVP), ALSO KNOWN AS DROOP FUNCTION (RECOMMENDED FOR CCM ONLY)

In some high-current applications, a requirement on a precisely controlled output impedance is imposed. This dependence of output voltage on load current is often termed, “droop”, “load line” regulation, or Adaptive Voltage Positioning (AVP).

The basic functionality of the AVP function is to achieve a controlled output resistance for the buck regulator, so that at 0A load, the output is +Ɛ% higher than the nominal voltage and at maximum load, the output is -Ɛ% related to nominal output value, as shown in Figure 4-13.

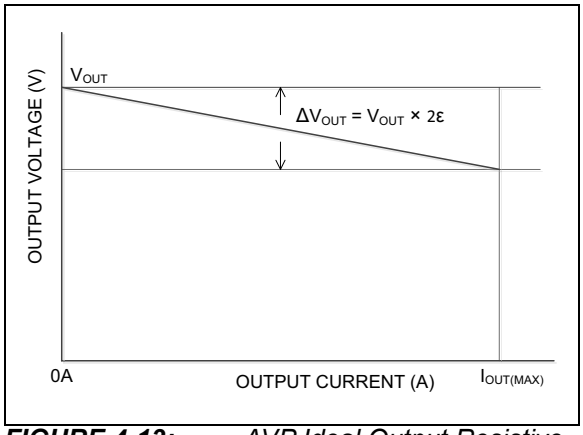


FIGURE 4-13: *AVP Ideal Output Resistive Characteristic.*

It is necessary to achieve the resistive characteristic above over the full frequency range of output loads.

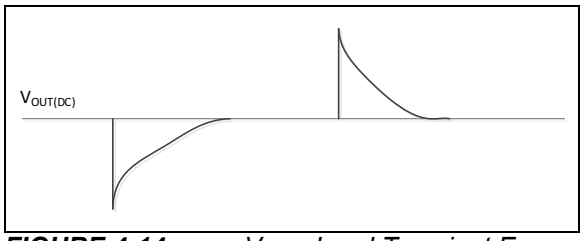


FIGURE 4-14: *V_{OUT} Load Transient Error without AVP/DROOP.*

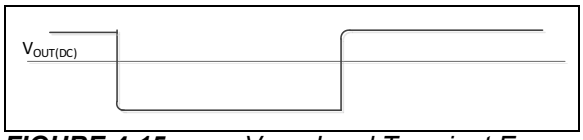


FIGURE 4-15: *V_{OUT} Load Transient Error with AVP/DROOP.*

Figure 4-14 and Figure 4-15 explain how the AVP design window of ±Ɛ can be used to reduce the amount of the output capacitor necessary to sustain the load transient. Alternatively, the AVP can be used to improve the error of the load transient if it is decided to keep the same output capacitor.

The DROOP pin is an analog output, which provides a voltage proportional to the output current in CCM according to the formula in Equation 4-20.

EQUATION 4-20:

$$V_{DROOP} = V_{CSH} - 1.2V = 8 \times R_{SENSE} \times I_L$$

Where:

V_{CSH} = Voltage at CSH Pin in CCM

R_{SENSE} = Current Sensing Resistance

I_L = Inductor Current per Phase

Because the current sensing range is ±120 mV, the output voltage range of V_{DROOP} is 0V to 0.96V.

The part of the schematic to implement the AVP for a 5V output is shown in Figure 4-16. The underlying assumption is that the current sense is done using sense resistors independent of temperature.

The sizing starts with the conditions: V_{DROOP} = 0V for I_{OUT} = 0A and V_{DROOP} = 600 mV for I_{OUT} = $I_{OUT(MAX)}$. Depending on the voltage drop across the sense resistors at $I_{OUT(MAX)}$, the DROOP pin can have a different value than 600 mV. We hypothesized that $V_{DROOP(IOUTMAX)}$ = 600 mV.

Step 1: Sizing the resistors for getting (1+Ɛ) × V_{OUT} at I_{OUT} = 0A. Because V_{DROOP} = 0, we have V_{OUT} according to Equation 4-21:

EQUATION 4-21:

$$V_{OUT} = \left(1 + \frac{R_{FBT}}{R_{FBB1} + R_{FBB2} \backslash\backslash R_{DROOP}}\right) \times V_{REF}$$

As a first approximation, consider choosing R_{FBB2} small enough so that $R_{FBB2} || R_{DROOP} \approx R_{FBB2}$, and we size R_{FBB1}, R_{FBB2} and R_{FBT} to get the correct 5.00V injection and stability.

Step 2: Sizing the resistors to have the trip of V_{OUT} × 2Ɛ from I_{OUT} = 0A to I_{OUT} = $I_{OUT(MAX)}$ or from V_{DROOP} = 0V to V_{DROOP} = 600 mV.

Then,

EQUATION 4-22:

$$2\mathcal{E} = \frac{\Delta V_{FBS}}{V_{REF}} = \frac{n_D \times V_{DROOP(MAX)}}{V_{REF}} \times \frac{R_{FBB2}}{R_{FBB2} + R_{DROOP}} \times \frac{R_{FBT}}{R_{FBT} + R_{FBB1} + R_{FBB2} \backslash\backslash R_{DROOP}}$$

Where:

n_D = Number of 2-Phase Controller Devices ($n_D = 1,2,3,4$)

If R_{DROOP} >> R_{FBB2} in Equation 4-22, then we can simplify the equation as shown in Equation 4-23 and re-arrange as Equation 4-24:

EQUATION 4-23:

$$2\mathcal{E} = \frac{n_D \times V_{DROOP(MAX)}}{V_{REF}} \times \frac{R_{FBB2}}{R_{FBB2} + R_{DROOP}} \times \frac{R_{FBT}}{R_{FBT} + R_{FBB1} + R_{FBB2}}$$

EQUATION 4-24:

$$R_{DROOP} = R_{FBB2} \times \left(\frac{n_D}{2\mathcal{E}} \times \frac{V_{DROOP(MAX)}}{V_{REF}} \times \frac{R_{FBT}}{R_{FBT} + R_{FBB1} + R_{FBB2}} - 1\right)$$

Step 3: The R_{FBB1} is slightly adjusted to get V_{OUT} × (1 + Ɛ) for I_{OUT} = 0A. The result is in Figure 4-16.

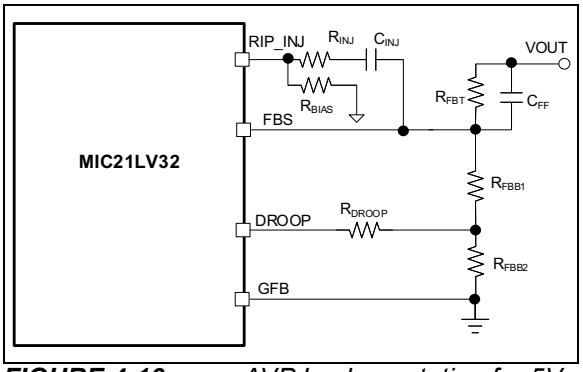


FIGURE 4-16: *AVP Implementation for 5V Output with 2% AVP Range for DROOP Pin Range 0V to 600 mV.*

Equation 4-23 and Equation 4-24 can also have the exact solution, the main difficulty being to find standard resistors of 0.1% to respect the initial positioning of +Ɛ for I_{OUT} = 0A and the 2Ɛ move down for $I_{OUT(MAX)}$.

The example above was based on temperature-independent current sensing using sense resistors. In case the bottom FET is used, the V_{DROOP} is defined as:

EQUATION 4-25:

$$V_{DROOP} = V_{CSH} - 1.2V = 8 \times R_{DSON(LS)} \times I_L$$

Where:

$R_{DSON(LS)}$ = Low-Side MOSFET Turn-On Resistance

Considering the sensing current range of 120 mV, it results that the operating maximum voltage value is:

EQUATION 4-26:

$$V_{DROOP(MAXOP)} = 120\,mV \times 8 = 0.96V$$

Since $R_{DSON(LS)}$ increases to about 2x at 125°C related to the value at 25°C, it is necessary to choose R_{DSON} × $I_{OUT(MAX)}$ < 60 mV at 25°C in order to respect the sensing range over temperature.

To desensitize the AVP related to the temperature variation of R_{DSON}, a resistance network with an NTC resistor needs to be used, as shown in Figure 4-17 on the next page.

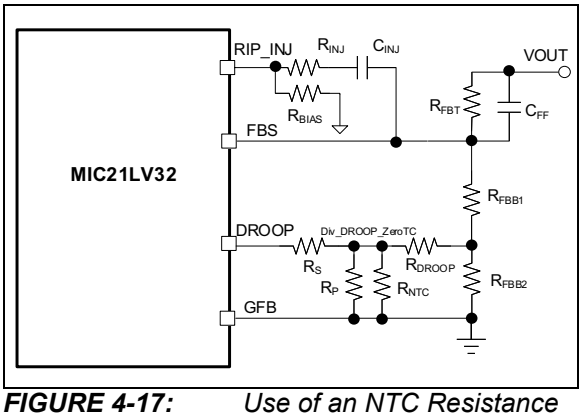


FIGURE 4-17: *Use of an NTC Resistance to Compensate the R_{DSON} Temperature Coefficient on the DROOP Pin.*

The idea in Figure 4-17 is that increasing DROOP voltage with temperature at the $I_{OUT(MAX)}$ (positive temperature coefficient) is compensated by the R_{NTC} (negative temperature coefficient) to keep the node of the divider, Div_DROOP_ZeroTC, constant versus temperature.

The rest of the calculations are similar to the aforementioned case where the sensing current was temperature-insensitive. In case the AVP is not necessary, a 10 kΩ, 1 nF series RC filter to ground can be used to have a reading of the filtered output current.

4.5.10 MULTIPHASING (STACKING)

The MIC21LV32 can be configured for multiphase operation up to eight phases. The MIC21LV32 has four pins allocated for multiphasing. The APO pin of the host controller is connected to the NPI pin of the next secondary controller. The host and secondary CSH, ONR pins are connected together. Once the host finishes the on requests, it passes the control to the next secondary through the APO pin. The current share bus will maintain equal current sharing between host and secondary controllers.

The ONR is a bidirectional pin. The desired secondary controller's FBS pin is connected to VDD to program the controller as secondary. This will make the ONR pin of the secondary controller become input only. Secondary controllers accept ONR from the host controller and serve the on-time request.

Figure 4-18 shows two MIC21LV32 devices connected in a 4-phase configuration. The NPI and APO pins of the MIC21LV32 are connected in a daisy chain to form a stackable power supply up to eight phases.

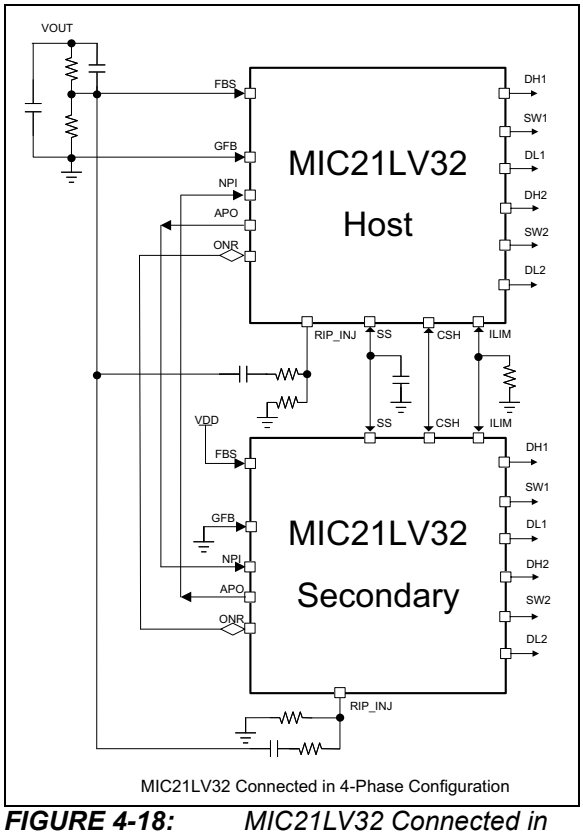


FIGURE 4-18: *MIC21LV32 Connected in 4-Phase Configuration.*

In order to get a stricter control over behavior if one member of the daisy chain is damaged or going to be damaged, or is in short or thermal shutdown, several measures were implemented.

1. The host is the only one programming the ILIM. The secondaries are just reading the voltage on ILIM; as a common point, they do not have any programming current coming out.
2. The soft start pin is driven up with 1.2 µA from all members of the daisy chain. When any of the members of the daisy chain pulls down the SS pin in case of thermal shutdown, or short circuits more than seven cycles, a new automatic restart is triggered on the falling edge of SS. Any of the daisy chain members can keep low closed to 0 in the SS pin, and in that case, all members are in High-Z and wait until SS is released to go up. To illustrate if one member has the LDO not coming up, this will keep the SS pin in low.

3. To ensure that some timing mismatch between chips is not creating a disorderly start, the delay in the block, BiasReadyGen, is 3 ms for the host and 1.5 ms (half) for the secondaries. The 3 ms and 1.5 ms timeframes are the result of the activity of a local oscillator and counter.

   This way, if there is a slight difference between different chips coming up, the secondaries are ready when the host is waking up after 3 ms.
4. The logic input pin, NPI (Next Phase In), of each part in the daisy chain has a 136 kΩ resistor to ground externally near the pin in the application. This way, if the input is floating because of a bad connection in the production line, it will be pushed to 0V, which will stop any activity from the chip to start. Also, NPI is active only on the rising edge. If it is floating and with no rising edge detected, the activity will stop.
5. When in daisy chain, the logic pin, ONR (On Request), from the host as output is going in each secondary ONR pin configured as an input. In order to accommodate different VDD rails from different secondaries and not to inject too much current in one of the secondaries from the host, the ONR pin as logic output has a 1 kΩ pull-up resistor inside. This way, the output ONR is short-protected ~ 5 mA to ground and the strength of the injection in the VDD rail of each secondary is 2k = 1k + 1k. Special precautions are designed inside so that this small injection will not trigger latch-up.
6. Only the error amplifier of the host controller regulates the output and feedback. The secondaries are only serving the ONR coming using the logic pins, NPI and APO, in sequence. The secondaries also inject ripple in the feedback in order to allow correct phasing and regulation. All members in the daisy chain are sharing the CSH pin to allow correct (equal) current sharing.
7. If droop feature is required in multi-phase operation, connect all the droop setting resistors from the DROOP pins of all members in the daisy chain to the lower bottom feedback resistor of the host controller to achieve loadline setting as in dual-phase operation.

4.5.11 FREQUENCY PROGRAMMING

The switching frequency per phase in CCM in two-phase operation can be programmed by Equation 4-27 below.

EQUATION 4-27:

$$R_{FREQ} = \frac{20.1 \times 10^9}{f_{SW\_PH}}$$

Where:

R_{FREQ} = Resistor Connects from FREQ Pin to AGND.

4.5.12 THERMAL SHUTDOWN

When the junction temperature of the MIC21LV32 reaches +160°C or above, the buck converter goes into thermal shutdown. When the junction temperature falls below +140°C, the MIC21LV32 buck converter soft starts again.

5.0 APPLICATION INFORMATION

5.1 Inductor Selection

Certain values for inductance, peak and RMS currents are required to select the output inductor. The input and output voltages, as well as the inductance value, determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value, and therefore, a larger and more expensive inductor. Higher switching frequencies allow the use of a small inductance, but increase power dissipation in the inductor core and MOSFET switching loss. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum DC output current contributed per phase. The inductance value of the inductor in each phase channel is calculated by Equation 5-1:

EQUATION 5-1:

$$L = \frac{V_{OUT} \times (Eff \times V_{IN(MAX)} - V_{OUT}) \times N_{PH}}{Eff \times V_{IN(MAX)} \times f_{SW} \times 0.2 \times I_{OUT(MAX)}}$$

Where:

- f_{SW} = Switching Frequency, 500 kHz
- 0.2 = Ratio of AC Ripple Current to Maximum DC Output Current Contributed per Phase
- $V_{IN(MAX)}$ = Maximum Power Stage Input Voltage
- N_{PH} = Total Number of Phases
- Eff = Efficiency of the Buck Converter
- $I_{OUT(MAX)}$ = Maximum DC Output Current

The peak-to-peak inductor current ripple in each phase is:

EQUATION 5-2:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (Eff \times V_{IN(MAX)} - V_{OUT})}{Eff \times V_{IN(MAX)} \times f_{SW} \times L}$$

The peak inductor current per phase is equal to the maximum average output current per phase, plus one half of the peak-to-peak inductor current ripple, as given in Equation 5-3.

EQUATION 5-3:

$$I_{L\_PH(PK)} = I_{OUTPH(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

$$I_{OUTPH(MAX)} = \frac{I_{OUT(MAX)}}{n}$$

Where:

- $I_{OUTPH(MAX)}$ = Maximum Average DC Output Current Contributed per Phase
- $I_{OUT(MAX)}$ = Maximum Output Current
- n = Total Number of Phases

The RMS inductor current in each phase is used to calculate the I^2R losses in the inductor per phase.

EQUATION 5-4:

$$I_{L\_PH(RMS)} = \sqrt{I_{OUTPH(MAX)}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

Maximizing efficiency requires selecting the proper core material and minimizing the winding resistance. The high-frequency operation of the MIC21LV32 requires the use of ferrite materials for all but the most cost-sensitive applications. Lower cost iron powder cores may be used, but the increase in core loss reduces the efficiency of the buck converter. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor size. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-5:

EQUATION 5-5:

$$P_{INDUCTOR(Cu)} = I_{L\_PH(RMS)}^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used must be at the operating temperature for accurate power dissipation estimation, as calculated in Equation 5-6 on the next page:

EQUATION 5-6:

$$R_{WINDING(HT)} = R_{WINDING(20^oC)} \times [1 + 0.0042 \times (T_H - T_{20^oC})]$$

Where:

- T_H = Temperature of Wire Under Full Load
- $T_{20°C}$ = Ambient Room Temperature
- $R_{WINDING(20°C)}$ = Room Temperature Winding Resistance (usually specified by the manufacturer)

5.2 Output Capacitor Selection

The output capacitor is usually determined by its capacitance and Equivalent Series Resistance (ESR). Voltage and RMS current capability are two other important factors in selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple voltage in steady state, while the total output capacitance must be large enough to sustain and maintain the output voltage during load transient to meet the desired load transient output voltage requirement.

To determine the required output capacitance for a two-phase buck converter in steady state, peak-to-peak output ripple current as seen by the output capacitors must be known. The peak-to-peak output ripple current for single-phase, two-phase, four-phase, six-phase and eight-phase buck converter is shown in Figure 5-1. The graph shows that peak-to-peak output ripple current, normalized by the maximum value, is a function of the duty cycle. Since each channel is 180 degrees out of phase with the other for a two-phase buck converter, the two-phase peak-to-peak output ripple current is less than that for a single-phase converter and the ripple current effective frequency is doubled, as seen by the output capacitor. This is the ripple reduction effect of two-phase operation. In addition, at 50% duty cycle, the inductor ripple currents from each channel cancel each other and the output ripple current is close to zero.

More ripple reduction can be achieved similarly for multiphase operation by stacking MIC21LV32 devices up to 4 devices together for multiphase operation from 4-phase up to 8-phase.

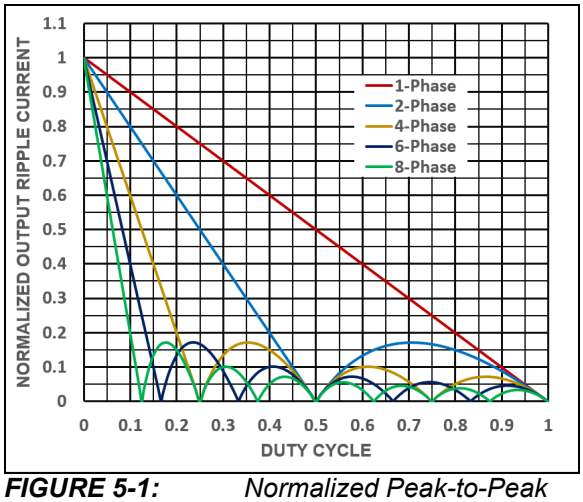


FIGURE 5-1: *Normalized Peak-to-Peak Output Ripple Current vs. Duty Cycle.*

The peak-to-peak output ripple current shown in Figure 5-1 is normalized by the maximum value, which is used as the normalizing factor for simplifying the calculation of output ripple current.

The peak-to-peak output ripple current maximum value and normalizing factor is calculated by Equation 5-7.

EQUATION 5-7:

$$\Delta I_{OPP(MAX)} = \frac{V_{OUT}}{L \times f_{SW}}$$

The approximate peak-to-peak output ripple current of a given multiphase buck converter at a given duty cycle can be determined from the corresponding normalized value for the given multiphase buck converter in Figure 5-1, multiplied by the normalizing factor, as shown in Equation 5-8 below.

EQUATION 5-8:

$$\Delta I_{OPP} = \Delta I_{OPP(NORMALIZED)} \times \Delta I_{OPP(MAX)}$$

Where:

$\Delta I_{OPP(NORMALIZED)}$ = Normalized Peak-to-Peak Output Ripple Current Value for Given Multiphase Buck Converter at Given Duty Cycle in Figure 5-1

The total output ripple voltage is a combination of the ripple voltages caused by the ESR and output capacitance. The output ripple voltage of the two-phase buck converter in steady state can then be determined from Equation 5-9.

EQUATION 5-9:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{OPP}}{16 \times C_{OUT} \times f_{SW}}\right)^2 + (\Delta I_{OPP} \times ESR_{COUT})^2}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-Peak Output Ripple Voltage
ΔI_{OPP} = Peak-to-Peak Output Ripple Current
C_{OUT} = Output Capacitance
f_{SW} = Switching Frequency per Phase
ESR_{COUT} = ESR of Output Capacitor

The minimum output capacitance required for a two-phase buck converter in steady state can be estimated by Equation 5-10.

EQUATION 5-10:

$$C_{OUT} \geq \frac{\Delta I_{OPP}}{16 \times \Delta V_{OUT(PP)} \times f_{SW}}$$

To meet the load transient requirement, the output capacitance must also fulfill the criteria in Equation 5-11. The output capacitance value chosen must meet the criteria in both equations.

EQUATION 5-11:

$$C_{OUT} \geq \frac{\Delta I_{LOAD}}{\Delta V_{OUT(TRANS)} \times \pi \times f_{CO}}$$

Where:

ΔI_{LOAD} = Output Load Current Step in Load Transient

$\Delta V_{OUT(TRANS)}$ = Output Voltage Change in Load Transient

f_{CO} = Crossover Frequency, Equal to About $f_{SW}/10$

The maximum value of the overall ESR of the output capacitor in steady state is calculated in Equation 5-12.

EQUATION 5-12:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{OPP}}$$

The maximum overall ESR value of the output capacitor must also meet the load transient requirement and is calculated in Equation 5-13. Then, the lower value must be chosen for the output capacitor ESR.

EQUATION 5-13:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(TRANS)}}{\Delta I_{LOAD}}$$

As described in **Section 4.1 "Control Architecture"**, the MIC21LV32 requires at least 20 mV peak-to-peak ripple at the FBS pin to make the g_m amplifier and the error comparator behave properly.

Also, the output voltage ripple should be in phase with the inductor current.

Therefore, the output voltage ripple caused by the output capacitor's value should be much smaller than the ripple caused by the output capacitor's ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method must be applied to provide enough feedback voltage ripple. Please refer to **Section 4.4 "Ripple Injection Circuit Components Selection"** for more details.

The voltage rating of the output capacitor should be 25% greater than the maximum output voltage. The output capacitor RMS current is calculated in Equation 5-14.

EQUATION 5-14:

$$I_{COUT(RMS)} = \frac{\Delta I_{OPP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is calculated in Equation 5-15.

EQUATION 5-15:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.3 Input Capacitor Selection

In addition to high-frequency ceramic capacitors, a larger bulk capacitance, either ceramic or aluminum electrolytic, should be used to help attenuate ripple on the input and to supply current to the input during large output current transients. The input capacitor for the power stage input V_{IN} should be selected for ripple voltage at V_{IN}, capacitance, ESR, ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents caused by turning the input supply on. A tantalum input capacitor's voltage rating must be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. Due to the ripple cancellation effect of the two-phase buck converter, the input ripple voltage and ripple current are smaller than those of the single-phase converter, and the effective ripple frequency seen by the input capacitor is twice the switching frequency. The input ripple voltage depends on the output current and input capacitor's capacitance and ESR. The steady state input voltage ripple can be estimated by Equation 5-16.

EQUATION 5-16:

$$\Delta V_{IN} \approx \frac{I_{OUT} \times \left(D - \frac{k}{n}\right) \times \left[\frac{1}{n} - \left(D - \frac{k}{n}\right)\right]}{n \times f_{SW} \times C_{IN}} + \frac{I_{OUT}}{n} \times ESR_{CIN}$$

Where:

I_{OUT} = Total Output Current

D = Duty Cycle per Phase

n = Total Number of Phases (n = 2,4,6,8)

k = 0,1,2,3,.... for D > k/n and k < n

f_{SW} = Switching Frequency per Phase

C_{IN} = Total Input Capacitance

ESR_{CIN} = Equivalent Series Resistance of Input Capacitor

The capacitance of the input capacitor can be determined in Equation 5-17.

EQUATION 5-17:

$$C_{IN} \geq \frac{I_{OUT} \times \left(D - \frac{k}{n}\right) \times \left[\frac{1}{n} - \left(D - \frac{k}{n}\right)\right]}{n \times f_{SW} \times \Delta V_{IN}}$$

Where:

k = 0,1,2,3,.... for D > k/n and k < n

n = Total Number of Phases (n = 2,4,6,8)

The ESR of the total input capacitance can be determined in Equation 5-18:

EQUATION 5-18:

$$ESR_{CIN} \leq \Delta V_{IN} \times \frac{n}{I_{OUT}}$$

The input capacitor must be rated for the input current ripple. The rated RMS value of the input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low, the RMS current rating of the input capacitor can be estimated from Equation 5-19:

EQUATION 5-19:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{\left(D - \frac{k}{n}\right) \times \left[\frac{1}{n} - \left(D - \frac{k}{n}\right)\right]}$$

Where:

$I_{OUT(MAX)}$ = Maximum Output Current

k = 0,1,2,3,.... for D > k/n and k < n, Maximum Integer Less than n×D

n = Total Number of Phases (n = 2,4,6,8)

The graph in Figure 5-2 shows the normalized RMS input capacitor current vs. duty cycle for single-phase, two-phase, four-phase, six-phase and eight-phase buck converter operation. Data are normalized to the output current.

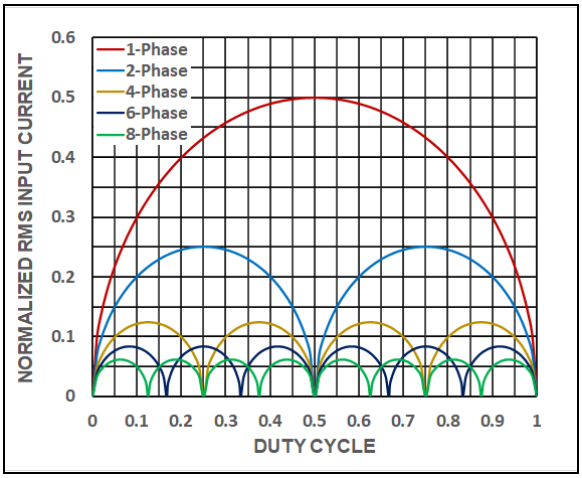


FIGURE 5-2: *Normalized RMS Input Capacitor Current vs. Duty Cycle.*

For a given multiphase buck converter operating at duty cycle D, the input capacitor RMS current can also be determined from the graph in Figure 5-2, together with Equation 5-20 below.

EQUATION 5-20:

$$I_{CIN(RMS)} = I_{CINRMS(NORM)} \times I_{OUT(MAX)}$$

Where:

$I_{CINRMS(NORM)}$ = Normalized RMS Input Capacitor Current at given Duty Cycle for Given Multi-Phase Buck Converter from Figure 5-2

The power dissipated in the input capacitor can then be computed from Equation 5-21:

EQUATION 5-21:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

The voltage rating of the input capacitor must be high enough to withstand the high input voltage. The recommended voltage rating is at least 1.25 times the maximum input voltage.

5.4 Switch Power MOSFET Selection

The following parameters are important for MOSFET selection:

- Voltage rating
- Current rating
- On-resistance
- Total gate charge

The voltage rating for both the high-side and low-side MOSFETs in the buck converter is essentially equal to the power stage input voltage, V_{IN}. A safety factor of 30% should be added to the $V_{IN(MAX)}$, while selecting the voltage rating of the MOSFETs to account for voltage spikes due to circuit parasitic elements, as shown in Equation 5-22.

EQUATION 5-22:

$$V_{DS(RATING)} \geq V_{IN(MAX)} \times 1.3$$

The peak switch current for both the high-side and low-side MOSFET in the buck converter is the same, and is equal to the peak inductor current in each phase, as shown in Equation 5-23 on the next page.

EQUATION 5-23:

$$I_{SWHS(PK)} = I_{SWLS(PK)} = \frac{I_{OUT(MAX)}}{n} + \frac{\Delta I_{L(PP)}}{2}$$

Where:

$I_{OUT(MAX)}$ = Maximum Output Current

n = Total Number of Phases

$\Delta I_{L(PP)}$ = Peak-to-Peak Inductor Current per Phase

The RMS current rating of the high-side power MOSFET in each phase channel is approximated in Equation 5-24.

EQUATION 5-24:

$$I_{SWHS(RMS)} = \frac{I_{OUT(MAX)}}{n} \times \sqrt{D_{MAX}}$$

Where:

D_{MAX} = Maximum Duty Cycle

The maximum duty cycle of each phase channel is calculated in Equation 5-25:

EQUATION 5-25:

$$D_{MAX} = \frac{V_{OUT(MAX)}}{Eff \times V_{IN(MIN)}}$$

Where:

$V_{OUT(MAX)}$ = Maximum Output Voltage

$V_{IN(MIN)}$ = Minimum Input Voltage

Eff = Efficiency of Buck Converter

The RMS current rating of the low-side power MOSFET in each phase channel is calculated in Equation 5-26.

EQUATION 5-26:

$$I_{SWLS(RMS)} = \frac{I_{OUT(MAX)}}{n} \times \sqrt{1 - D_{MAX}}$$

Where:

D_{MAX} = Maximum Duty Cycle

The conduction loss of the high-side power MOSFET in each phase channel is calculated in Equation 5-27.

EQUATION 5-27:

$$P_{COND(HS)} = I_{SWHS(RMS)}^2 \times R_{DSON(HS)}$$

Where:

$R_{DSON(HS)}$ = High-Side MOSFET On-Resistance

The conduction loss of the low-side power MOSFET in each phase channel is calculated in Equation 5-28.

EQUATION 5-28:

$$P_{COND(LS)} = I_{SWLS(RMS)}^2 \times R_{DSON(LS)}$$

Where:

$R_{DSON(LS)}$ = Low-Side MOSFET On-Resistance

The switching loss of the high-side power MOSFET in each phase channel is estimated in Equation 5-29.

EQUATION 5-29:

$$P_{SWL(HS)} = V_{IN(MAX)} \times \frac{I_{OUT(MAX)}}{2n} \times (t_R + t_F) \times f_{SW}$$

$$t_R = Q_{G(HS)} \times \frac{(R_{ONDHH} + R_{G(HS)})}{V_{DD} - V_{TH(HS)}}$$

$$t_F = Q_{G(HS)} \times \frac{(R_{ONDHL} + R_{G(HS)})}{V_{TH(HS)}}$$

$$Q_{G(HS)} = 0.5 \times Q_{GSHS} + Q_{GDHS}$$

Where:

t_R = High-Side MOSFET Turn-On Transition Time

t_F = High-Side MOSFET Turn-Off Transition Time

$Q_{G(HS)}$ = Switching Gate Charge of High-Side MOSFET

Q_{GSHS} = Gate-to-Source Charge of High-Side MOSFET

Q_{GDHS} = Gate-to-Drain Charge of High-Side MOSFET

R_{ONDHH} = High-Side Gate Driver Pull-up Resistance

R_{ONDHL} = High-Side Gate Driver Pull-Down Resistance

$R_{G(HS)}$ = Gate Resistance of High-Side MOSFET

$V_{TH(HS)}$ = High-Side MOSFET Gate-to-Source Threshold Voltage

The high-side MOSFET output capacitance discharge loss can be calculated in Equation 5-30.

EQUATION 5-30:

$$P_{COSS(HS)} = 0.5 \times C_{OSS(HS)} (V_{IN(MAX)})^2 \times f_{SW}$$

Where:

$C_{OSS(HS)}$ = High-Side MOSFET Output Capacitance

The total power dissipation of the high-side power MOSFET in each phase channel is the sum of the conduction loss, the switching loss and the MOSFET output capacitance discharge loss, as shown in Equation 5-31.

EQUATION 5-31:

$$P_{D(HS)} = P_{COND(HS)} + P_{SWL(HS)} + P_{COSS(HS)}$$

The high-side power MOSFET in each phase channel selected must be capable of handling the total power dissipation. To improve efficiency and minimize the power loss, the power MOSFET should be selected with low on-resistance and optimum gate charge.

On the other hand, the power dissipation in the low-side power MOSFET in each phase channel is mainly contributed to by the conduction loss and there is no switching loss for the low-side MOSFET in the buck converter since the body diode of the low-side MOSFET is forward-biased before the turn-on, and after the turn-off of the low-side MOSFET, which makes

the voltage across the low-side MOSFET equal to the body diode's forward voltage during the turn-on and turn-off transition.

Apart from the conduction loss, low-side MOSFET body diode forward conduction loss, body diode reverse recovery loss and low-side MOSFET output capacitance discharge loss also contribute to the power dissipation in the low-side power MOSFET in each phase channel.

The low-side MOSFET body diode forward conduction loss during dead time is calculated by Equation 5-32.

EQUATION 5-32:

$$P_{BDDT(LS)} = \frac{2 \times I_{OUT(MAX)}}{n} \times V_{F(BD)} \times t_{DT} \times f_{SW}$$

Where:

$V_{F(BD)}$ = Forward Voltage of Low-Side MOSFET Body Diode

t_{DT} = Dead Time, which is about 20 ns

The low-side MOSFET body diode reverse recovery loss is calculated by Equation 5-33.

EQUATION 5-33:

$$P_{BDQRR(LS)} = V_{IN(MAX)} \times Q_{RR(BDLS)} \times f_{SW}$$

Where:

$Q_{RR(BDLS)}$ = Reverse Recovery Charge of Low-Side MOSFET Body Diode

The low-side MOSFET output capacitance discharge loss can be calculated in Equation 5-34.

EQUATION 5-34:

$$P_{COSS(LS)} = 0.5 \times C_{OSS(LS)}(V_{IN(MAX)})^2 \times f_{SW}$$

Where:

$C_{OSS(LS)}$ = Low-Side MOSFET Output Capacitance

The total power dissipation of the low-side power MOSFET in each phase channel is estimated in Equation 5-35.

EQUATION 5-35:

$$P_{D(LS)} = P_{COND(LS)} + P_{BDDT(LS)} + P_{BDQRR(LS)} + P_{COSS(LS)}$$

Since low-side MOSFETs can be accidentally turned on by the high dV/dt signal at switching node, low-side MOSFETs with high C_{GS}/C_{GD} ratio and low internal gate resistance should be chosen to minimize the effect of dV/dt inducted turn-on.

5.5 Bootstrap Capacitor

The MIC21LV32 device's high-side gate drive circuits are designed to switch the N-Channel external MOSFETs. The MIC21LV32 shows two external boot-strap diodes and each one is between the PVDD and BST pins of each phase channel. These circuits supply energy to the high-side gate drive circuits with one for each phase. A low-ESR ceramic capacitor should be connected between the BST pin and the SW pin of each phase channel (refer to the **"Typical Application Circuits"**). The bootstrap capacitors between the BST and the SW pins, C_{BST1} and C_{BST2}, are charged while the respective low-side MOSFET is turned on. When the respective high-side MOSFET driver is turned on, energy from C_{BSTx} is used to turn the MOSFET on. A minimum of 0.1 µF low-ESR ceramic capacitor is recommended between the BSTx and SWx pins. The required value of C_{BSTx} can be calculated using Equation 5-36.

EQUATION 5-36:

$$C_{BSTx} = \frac{Q_{G(HS)}}{\Delta V_{CBSTx}}$$

Where:

$Q_{G(HS)}$ = Gate Charge of High-Side MOSFET in Each Phase

ΔV_{CBSTx} = Delta Voltage Drop Across C_{BST} in Each Phase, Generally 50 mV to 100 mV

5.6 Setting Output Voltage

The MIC21LV32 requires two resistors to set the output voltage, as shown in Figure 5-3.

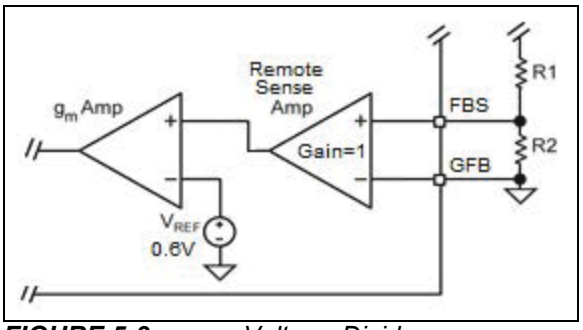


FIGURE 5-3: *Voltage-Divider Configuration.*

The output voltage is determined by Equation 5-37.

EQUATION 5-37:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{REF} = 0.6V

A typical value of R1 can be between 3 kΩ and 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it decreases the efficiency of the buck converter, especially at light loads. After R1 is selected, R2 can be calculated using the formula found in Equation 5-38.

EQUATION 5-38:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}}$$

5.7 AVP Droop Load Line Resistance

The AVP droop load line resistance can be calculated by Equation 5-39.

EQUATION 5-39:

$$R_{LOADLINE} = \frac{\Delta V_{OUT(DROOP)}}{\Delta I_{L(PK)}} = \frac{4 \times R_{SENSE}}{1 + \frac{R_{DROOP}}{R_{FBB2}}} \times \left(1 - \frac{V_{REF}}{V_{OUT}}\right) \times \frac{V_{OUT}}{V_{REF}}$$

Where:

- $\Delta V_{OUT(DROOP)}$ = Change in Output Voltage with Load
- $\Delta I_{L(PK)}$ = Total Change in Peak Inductor Current for All Phases for a Given Change in Load Current
- R_{SENSE} = Current Sense Resistance
- V_{REF} = Reference Voltage (0.6V typical)
- V_{OUT} = Output Voltage
- R_{DROOP} = Resistance of Droop Setting Resistor Connected at the DROOP Pin
- R_{FBB2} = Lower Bottom Feedback Resistance Value

5.8 Power Dissipation in MIC21LV32

The MIC21LV32 features two Low-Dropout (LDO) regulators to supply power at the PVDD pin from either VIN or EXTVDD, depending on the voltage at the EXTVDD pin. PVDD powers MOSFET drivers and the VDD pin, which powers the internal circuitry and is recommended to connect to PVDD through a low-pass filter. In the applications where the output voltage is 5V and above (up to 14V), it is recommended to connect EXTVDD to the output to reduce the power dissipation in the MIC21LV32, in order to reduce the MIC21LV32 junction temperature and to improve the system efficiency. The power dissipation in the MIC21LV32 depends on the internal LDO being in use, gate charge of the external MOSFETs and switching frequency. The power dissipation and the junction temperature of the MIC21LV32 can be estimated using Equation 5-40, Equation 5-41 and Equation 5-42.

Power dissipation in the MIC21LV32 is calculated in Equation 5-40 when EXTVDD is not used.

EQUATION 5-40:

$$P_{IC} = V_{IN} \times (I_{G(TOTAL)} + I_Q)$$

$$I_{G(TOTAL)} = (Q_{G(HS1)} \times Q_{G(LS1)} + Q_{G(HS2)} + Q_{G(LS2)}) f_{SW}$$

Where:

- $I_{G(TOTAL)}$ = Total Average Gate Drive Current for All Phases
- I_Q = Quiescent Current of MIC21LV32
- $Q_{G(HS1)}$, $Q_{G(LS1)}$ = Gate Charge of High-Side and Low-Side MOSFETs in Phase 1
- $Q_{G(HS2)}$, $Q_{G(LS2)}$ = Gate Charge of High-Side and Low-Side MOSFETs in Phase 2

Power dissipation in the MIC21LV32 is calculated in Equation 5-41 when EXTVDD is used.

EQUATION 5-41:

$$P_{IC} = V_{EXTVDD} \times (I_{G(TOTAL)} + I_Q)$$

Where:

- V_{EXTVDD} = Voltage at EXTVDD Pin ($4.7V \le V_{EXTVDD} \le 14V$ typically)
- $I_{G(TOTAL)}$ = Total Average Gate Drive Current for All Phases
- I_Q = Quiescent Current of MIC21LV32

The junction temperature of the MIC21LV32 can be estimated using Equation 5-42.

EQUATION 5-42:

$$T_J = P_{IC} \times \theta_{JA} + T_A$$

Where:

- T_J = Junction Temperature of MIC21LV32
- T_A = Ambient Temperature
- P_{IC} = Power Dissipation of MIC21LV32
- θ_{JA} = Junction-to-Ambient Thermal Resistance of MIC21LV32 (34°C/W typical)

The maximum recommended operating junction temperature for the MIC21LV32 is 125°C. Using the output voltage of the same switching converter when it is between 4.7V (typical) and 14V, as the voltage at the EXTVDD pin, significantly reduces the power dissipation inside the MIC21LV32. This reduces the junction temperature rise as illustrated further.

For a typical case of:
V_{IN} = 36V, V_{OUT} = 5V, $I_{G(TOTAL)}$ = 20 mA, I_Q = 5 mA and maximum ambient temperature, T_A = 85°C.

When the EXTVDD is not used, the MIC21LV32 junction temperature is calculated as shown in Equation 5-43.

EQUATION 5-43:

$$P_{IC} = 36V \times (20\ mA + 5\ mA)$$

$$P_{IC} = 0.9W$$

$$T_J = 0.9W \times 34ºC/W + 85ºC$$

$$T_J = 115.6ºC$$

When the EXTVDD is used and the 5V output of the MIC21LV32 buck converter is used as the input to the EXTVDD pin, the MIC21LV32 junction temperature is calculated as shown in Equation 5-44. The junction temperature is significantly reduced from 115.6°C to 89.3°C when the EXTVDD is used.

EQUATION 5-44:

$$P_{IC} = 5V \times (20\ mA + 5\ mA)$$

$$P_{IC} = 0.125W$$

$$T_J = 0.125W \times 34ºC/W + 85ºC$$

$$T_J = 89.3ºC$$

5.9 Thermal Measurements

It is a good idea to measure the IC's case temperature to make sure it is within its operating limits. Although this might seem an elementary task, it is easy to get false results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, which results in a lower case temperature measurement.

There are two methods of temperature measurement: using a smaller thermal couple wire or using an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heatsinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to ensure that the thermal couple junction makes good contact with the case of the IC. Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor IC. However, an IR thermometer with a 1 mm spot size is a good choice for measuring the hottest point on the case. An optional stand can be used to make it easy to hold the beam on the IC for long periods of time. In addition, a more advanced, convenient and accurate infrared thermal camera can be used, although such equipment is much more expensive.

6.0 PCB LAYOUT GUIDELINES

Note:	To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. Use star ground technique between AGND and PGND, and minimize trace length for high-current paths.

Follow these guidelines to ensure proper operation of the MIC21LV32 two-phase buck converter.

6.1 Integrated Circuit

- The 2.2 µF ceramic capacitor, which is connected to the VDD pin, must be located right at the IC. The VDD pin is very noise-sensitive, so the placement of the capacitor is critical. Use wide traces to connect to the VDD, PVDD and PGND pins.
- Connect a 2.2 µF ceramic capacitor to the EXTVDD pin, which must be located right at the IC.
- Connect the Analog Ground pin (AGND) directly to the ground planes. Do not route the AGND pin to the PGND pad on the top layer.
- Use thick traces and minimize trace length for the input and output power lines.
- Keep the analog and power grounds separate, and connected at only one location.

6.2 Input Capacitor

- Use parallel input capacitors to minimize effective ESR and ESL of input capacitor.
- Place input capacitors next to the high-side power MOSFETs for each phase channel.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Connect the V_{IN} supply to the VIN pin through a 1.2Ω resistor and connect a 1 µF ceramic capacitor from the VIN pin to the PGND pin. Keep both the VIN pin and PGND connections short.
- Place several vias to the ground plane, close to the input capacitors' ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U-type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- In hot-plug applications, use an electrolytic bypass capacitor to limit the overvoltage spike seen on the input supply when power is suddenly applied.

6.3 Inductor

- Keep the inductor connection to the switch node (SW1, SW2) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW1, SW2) away from the Feedback (FBS) pin.
- Connect the CSPx pin and CSNx pin directly to the drain and source of the low-side power MOSFET, respectively, and route the CSP and CSN traces together for each phase channel to accurately sense the voltage across the low-side MOSFET to achieve accurate current sensing.
- To minimize noise, place a ground plane under the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. There should be sufficient vias on the power traces to conduct high current between the inductor and the IC and output load. It does not matter whether the IC or inductor is on the top or bottom, as long as there is enough heatsink and air flow to keep the power components within their temperature limits. Place the input and output capacitors on the same side of the board as the IC.

6.4 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

6.5 MOSFETs

- MOSFET gate drive traces must be short and wide. The ground plane should be the connection between the MOSFET source and PGND.
- Choose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance to minimize the effect of dV/dt inducted turn-on.
- Use a 4.5V rated V_{GS} MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET.

6.6 V_{OUT} Remote Sense

- The remote sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, MOSFETs and other high dV/dt or di/dt sources.

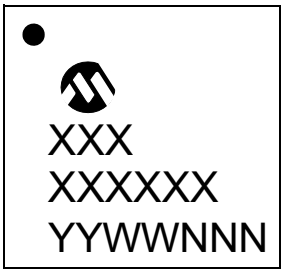
6.7 RC Snubber

- If it is needed, place a RC snubber on either side of the board and as close to the SW pin as possible.

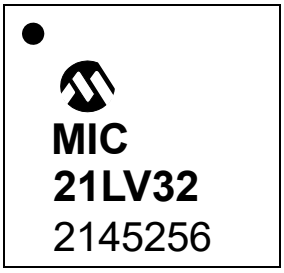
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

32-Lead VQFN (5 mm x 5 mm)



Example

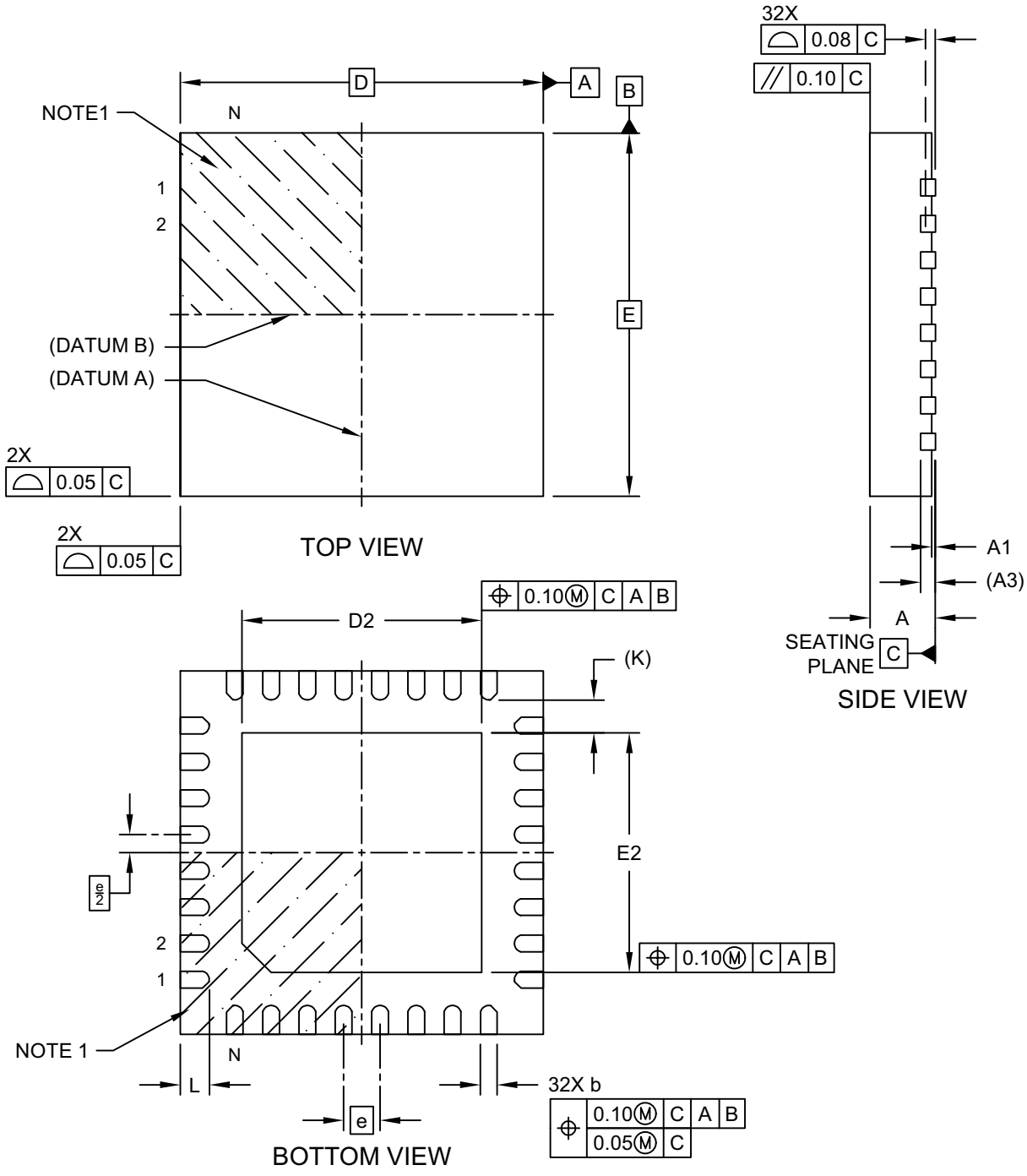


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

32-Lead Very Thin Quad Flat, No Lead Package (QLA) - 5x5x0.9 mm Body [VQFN] With 3.3 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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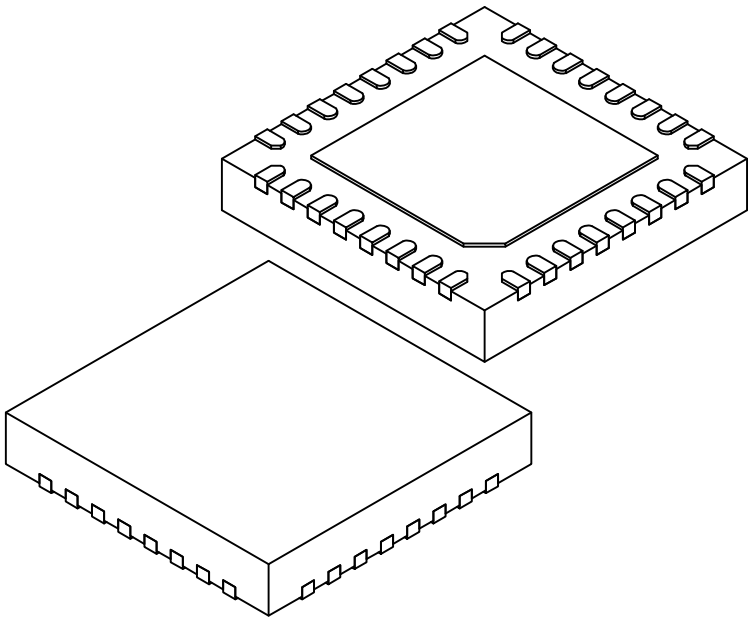
32-Lead Very Thin Quad Flat, No Lead Package (QLA) - 5x5x0.9 mm Body [VQFN] With 3.3 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.25	3.30	3.35
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.25	3.30	3.35
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.45 REF	

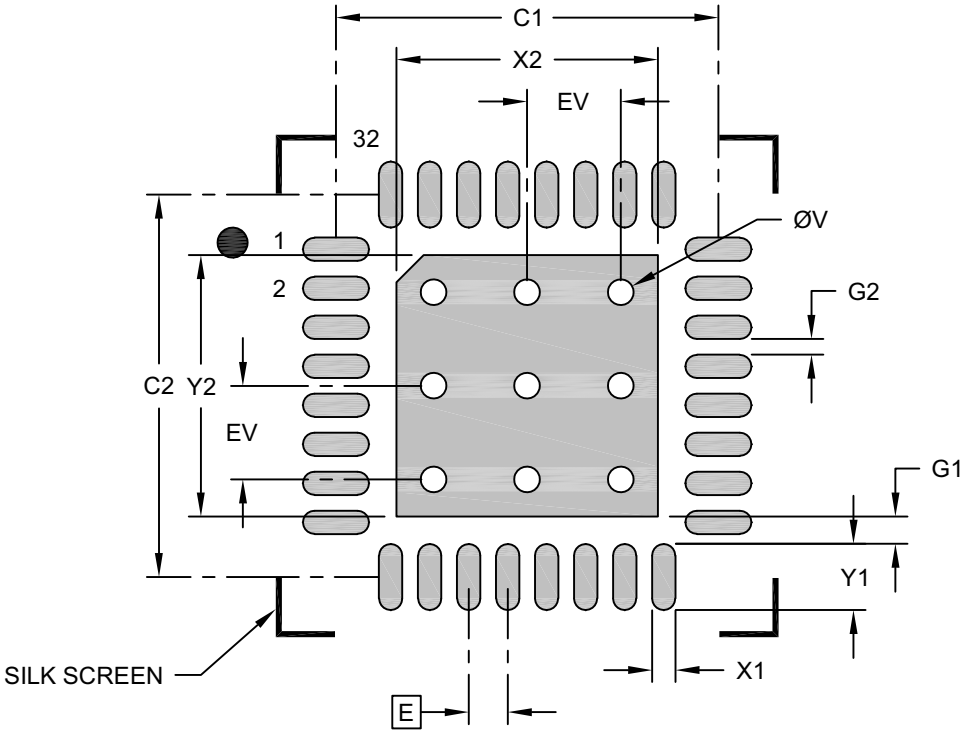
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1285 Rev A Sheet 2 of 2

32-Lead Very Thin Quad Flat, No Lead Package (QLA) - 5x5x0.9 mm Body [VQFN] With 3.3 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.35
Optional Center Pad Length	Y2			3.35
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.35		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		0.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3285 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (September 2022)

- Updated document layout.
- Minor corrections throughout.
- Updated Applications, General Description, **Section 4.5.10 “Multiphasing (Stacking)”** and **Section 5.2 “Output Capacitor Selection”** to include additional information.
- Updated **Section 1.0 “Electrical Characteristics”**, **Section 3.0 “Pin Descriptions”**, **Section 4.0 “Functional Description”**, **Section 5.0 “Application Information”** and **Section 7.0 “Packaging Information”** to better describe the part.
- Updated the Electrical Characteristics(1) table.
- Updated the following figures: Typical Application Circuits, Functional Block Diagram, Figure 2-34, Figure 2-35, Figure 4-4, Figure 4-5, Figure 4-11, Figure 4-13, Figure 4-18, Figure 5-1 and Figure 5-2.
- Updated the following equations: Equation 4-4, Equation 4-22, Equation 4-23, Equation 4-24, Equation 4-26, Equation 5-8, Equation 5-16, Equation 5-17, Equation 5-19, Equation 5-20, Equation 5-25, Equation 5-39, Equation 5-43 and Equation 5-44.

Revision A (March 2021)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	-XX(1)
Device	Junction Temperature Range	Package	Media Type

Device:	MIC21LV32:	36V Dual Phase, Advanced COT Buck Controller Stackable for Multiphase Operation	
Junction Temperature Range:	Y	=	–40°C to +125°C, RoHS-Compliant
Package:	ML	=	32-Lead, 5 mm x 5 mm VQFN
Media Type:	TR	=	3300/Reel

Examples:

a) MIC21LV32YML-TR: 36V Dual Phase, Advanced COT Buck Controller Stackable for Multiphase Operation, –40°C to +125°C Junction Temperature Range, 32-Lead 5 mm x 5 mm VQFN Package, 3300/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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