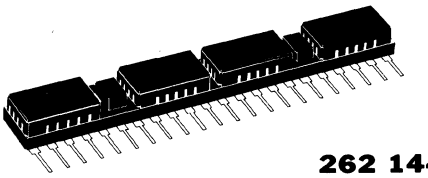


MH6404AD1-15

262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

The MH6404AD1 is 65 536-word x 4 bit dynamic RAM and consists of four industry standard 64 K x 1 dynamic RAMs in leadless chip carrier.

The mounting of leadless chip carriers on a ceramic single in-line package provides any application where high densities and large quantities of memory are required.

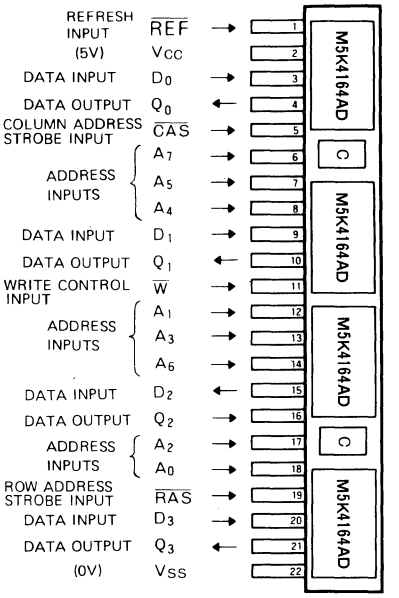
FEATURES

- High speed

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH6404AD1-15	150	260	600

- Utilizes industry standard 64K RAMs in leadless chip carriers
- 22 pin Single In-line Package
- Single +5V (±10%) supply operation
- Low stand by power dissipation ..... 88 mW(max)
- Low operating power dissipation:
  MH6404AD1-15 990mW(max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22μF x 2) decoupling capacitors
- 128 refresh cycles (every 2ms) A_7 Pin is not need for refresh
- Pin 1 controls automatic-and self-refresh mode

PIN CONFIGURATION (TOP VIEW)

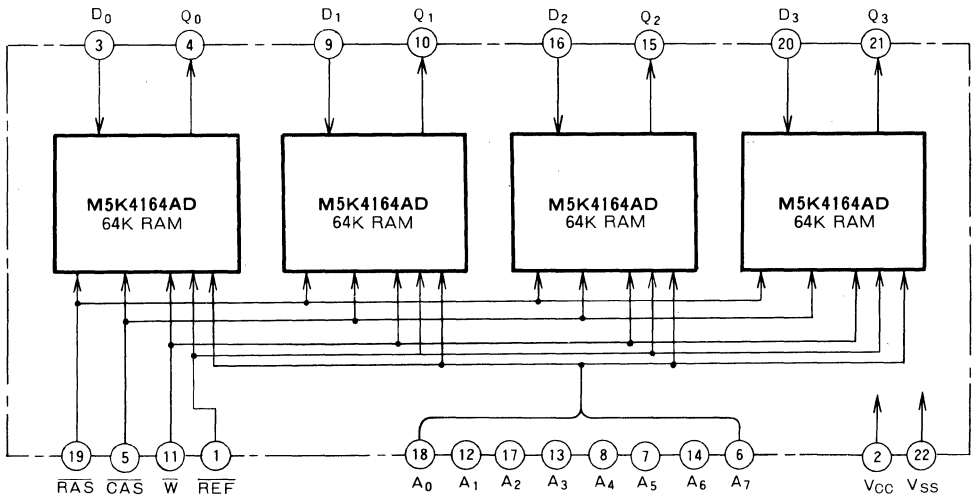


Outline 22S5

APPLICATION

- Main memory unit for computers
- Refresh memory for CRT

BLOCK DIAGRAM



FUNCTION

The MH6404AD1 provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs							Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	$\overline{REF}$	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	NAC	VLD	YES	Page mode identical
Write	ACT	ACT	ACT	VLD	APD	APD	NAC	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	NAC	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	NAC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	APD	DNC	NAC	VLD	YES	
Automatic refresh	NAC	DNC	DNC	DNC	DNC	DNC	ACT	OPN	YES	
Self refresh	NAC	DNC	DNC	DNC	DNC	DNC	ACT	OPN	YES	
Hidden automatic refresh	NAC	ACT	DNC	DNC	DNC	DNC	ACT	VLD	YES	
Hidden self refresh	NAC	ACT	DNC	DNC	DNC	DNC	ACT	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	NAC	OPN	NO	

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.

SUMMARY OF OPERATIONS

Addressing

To select 4 of the 262144 memory cells in the MH6404AD1 the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS-CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS-CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS-CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Date to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is storobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for set-up and hold times.

Data Output Control

The outputs of the MH6404AD1 are in the high-impedance state when $\overline{CAS}$ is high. When the are memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the outputs entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The outputs will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the MH6404AD1, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, inputs and outputs can be connected directly to give a common I/O data bus.

2. Data Output Hold

The data outputs can be held between read cycles, without lenghening the cycle time. This enebles extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the MH6404AD1 must be refreshed every 2 ms to maintain data. The methods of refreshing for the MH6404AD1 are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

3. Automatic Refresh

Pin1 ($\overline{REF}$) has two special functions. The MH6404AD1 has a refresh address counter, refresh address multiplexer and refresh timer for these operations. Automatic refresh is initiated by bringing $\overline{REF}$ low after $\overline{RAS}$ has precharged and is used during standard operation just like $\overline{RAS}$-only refresh, except that sequential row addresses from an external counter are no longer necessary.

At the end of automatic refresh cycle, the internal refresh address counter will be automatically incremented. The output state of the refresh address counter is initiated by some eight $\overline{REF}$, $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycle after power is applied. Therefore, a special operation is not necessary to initiate it.

$\overline{RAS}$ must remain inactive during $\overline{REF}$ activated cycles. Likewise, $\overline{REF}$ must remain inactive during $\overline{RAS}$ generated cycle.

4. Self-Refresh

The other function of pin 1 ($\overline{REF}$) is self-refresh. Timing for self-refresh is quite similar to that for automatic refresh. As long as $\overline{RAS}$ remains high and $\overline{REF}$ remains low, the MH6404AD1 will refresh itself. This internal sequence repeats a synchronously every 12 to 16 μs. After 2 ms, the on-chip refresh address counter has advanced through all the row addresses and refreshed the entire memory. Self-refresh is primarily intended for trouble free power-down operation.

For example, when battery backup is used to maintained data integrity in the memory. $\overline{REF}$ may be used to place the device in the self-refresh mode with no external timing signals necessary to keep the information alive.

In summary, the pin 1 (REF) refresh function gives the user a feature that if free, save him hardware on the board, and in fact, will simplify his battery backup procedures, increase his battery life, and save him overall cost while giving him improved system performance.

There is an internal pullup resister ($\approx$800KΩ) on pin 1, so if the pin 1 ($\overline{REF}$) function is not used, pin 1 may be left open (not connect) without affecting the normal operations.

5. Hidden Refresh

A features of the MH6404AD1 is that refresh cycle may be performed while maintaining valid data at the output pins by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, automatic refresh and self-refresh, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the MH6404AD1 is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the MH6404AD1 as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The MH6404AD1 operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycle is necessary after power is applied to the device before memory operation is achieved.

262 144-BIT (65 536-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25℃	4000	mW
Topr	Operating free-air temperature range		0～70	℃
Tstg	Storage temperature range		−55～150	℃
Tsld	Soldering temperature time		260・10	℃・sec

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1. All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta＝0～70℃, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}＝−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, All other pins＝0V	−40		40	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note3, 4)	MH6404AD1-15	$\overline{RAS}$, $\overline{CAS}$ cycling t_{CR}＝t_{CW}＝min output open			180	mA
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$＝V_{IH} output open			16	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	MH6404AD1-15	$\overline{RAS}$ cycling $\overline{CAS}$＝V_{IH} $t_{C(\overline{REF})}$＝min, output open			140	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note3, 4)	MH6404AD1-15	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$ cycling t_{CPG}＝min, output open			140	mA
$I_{CC5(AV)}$	Average supply current from V_{CC}, automatic refreshing (Note 3)	MH6404AD1-15	$\overline{RAS}$＝V_{IH}, $\overline{REF}$ cycling $t_{C(\overline{REF})}$＝min, output open			140	mA
$I_{CC6(AV)}$	Average supply current from V_{CC}, self refreshing		$\overline{RAS}$＝V_{IH}, $\overline{REF}$＝V_{IL} output open			32	mA
$C_{I(A)}$	Input capacitance, address inputs		V_I＝V_{SS} f＝1MHz V_i＝25mVrms			35	pF
$C_{I(D)}$	Input capacitance, data input					10	pF
$C_{I(W)}$	Input capacitance, write control input					40	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					50	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					50	pF
$C_{I(\overline{REF})}$	Input capacitance, $\overline{REF}$ input					50	pF
C_O	Output capacitance		V_O＝V_{SS}, f＝1MHz, V_i＝25mVrms			15	pF

Note 2: Current flowing into an IC is positive; out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC5(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

(T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted. See notes 5, 6 and 7)

Symbol	Parameter		Alternative Symbol	MH6404AD1-15 Limits Min	MH6404AD1-15 Limits Max	Unit
t_{CRF}	Refresh cycle time		t_{REF}		2	ms
$t_{w(RASH)}$	$\overline{RAS}$ high pulse width		t_{RP}	100		ns
$t_{w(RASL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	150	10000	ns
$t_{w(CASL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	75	∞	ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	(Note 8)	t_{CPN}	35		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$		t_{CSH}	150		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$		t_{RSH}	75		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$	(Note 9)	t_{CRP}	−20		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$	(Note 10)	t_{RCD}	30	75	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$		t_{ASR}	0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$		t_{ASC}	0		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$		t_{RAH}	20		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$		t_{CAH}	25		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$		t_{AR}	95		ns
t_{THL} t_{TLH}	Transition time		t_T	3	35	ns

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL}=t_{TLH}=5ns$.
7: Reference levels of input signals are V_{IH}min and V_{IL}max. Reference levels for transition time are also between V_{IH} and V_{IL}.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$.)
10: Operation within the $t_{d(RAS-CAS)}$max limit insures that $t_{a(RAS)}$max can be met. $t_{d(RAS-CAS)}$max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)}min = t_{h(RAS-RA)}min + 2t_{THL(t_{TLH})} + t_{su(CA-CAS)}min$.

SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Read Cycle

Symbol	Parameter		Alternative Symbol	MH6404AD1-15 Limits Min	MH6404AD1-15 Limits Max	Unit
t_{CR}	Read cycle time		t_{RC}	260		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$		t_{RCS}	0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$	(Note 11)	t_{RCH}	0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$	(Note 11)	t_{RRH}	20		ns
$t_{dis(CAS)}$	Output disable time	(Note 12)	t_{OFF}	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time	(Note 13)	t_{CAC}		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time	(Note 14)	t_{RAC}		150	ns

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
Note 12: $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}
Note 13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max. Test conditions; Load=2T TL, C_L=100pF
Note 14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$max. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)}$max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load=2T TL, C_L=100pF

Write Cycle

Symbol	Parameter		Alternative Symbol	MH6404AD1-15 Limits Min	MH6404AD1-15 Limits Max	Unit
t_{CW}	Write cycle time		t_{RC}	260		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$	(Note 17)	t_{WCS}	−5		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$		t_{WCH}	45		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$		t_{WCR}	95		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write		t_{RWL}	45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write		t_{CWL}	45		ns
$t_{w(W)}$	Write pulse width		t_{WP}	45		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$		t_{DS}	0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$		t_{DH}	45		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$		t_{DHR}	95		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Alternative Symbol	MH6404AD1-15 Limits Min	Limits Max	Unit
t_{CRW}	Read-write cycle time	(Note 15)	t_{RWC}	280		ns
t_{CRMW}	Read-modify-write cycle time	(Note 16)	t_{RMWC}	310		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write		t_{RWL}	45		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write		t_{CWL}	45		ns
$t_{w(W)}$	Write pulse width		t_{WP}	45		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$		t_{RCS}	0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write	(Note 17)	t_{RWD}	120		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write	(Note 17)	t_{CWD}	60		ns
$t_{su(D-W)}$	Data-in setup time before write		t_{DS}	0		ns
$t_{h(W-D)}$	Data-in hold time after write		t_{DH}	45		ns
$t_{dis(CAS)}$	Output disable time		t_{OFF}	0	40	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time	(Note 13)	t_{CAC}		75	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time	(Note 14)	t_{RAC}		150	ns

Note 15: t_{CRW} min is defined as $t_{CRW}\,\text{min} = t_{d(RAS-W)} + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16: t_{CRMW} min is defined as $t_{CRMW}\,\text{min} = t_{a(RAS)}\,\text{max} + t_{h(W-RAS)} + t_{w(RAS-H)} + 3t_{TLH(tTHL)}$

17: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}$ min, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}$ min and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}$ min a read-write cycle is performed, and the data of the selected address will be read out on the data output.
For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	MH6404AD1-15 Limits Min	Limits Max	Unit
t_{CPGR}	Page-mode read cycle time	t_{PC}	145		ns
t_{CPGW}	Page-Mode write cycle time	t_{PC}	145		ns
t_{CPGRW}	Page-Mode read-write cycle time	—	180		ns
t_{CPGRMW}	Page-Mode read-modify-write cycle time	—	195		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	60		ns

Automatic Refresh Cycle

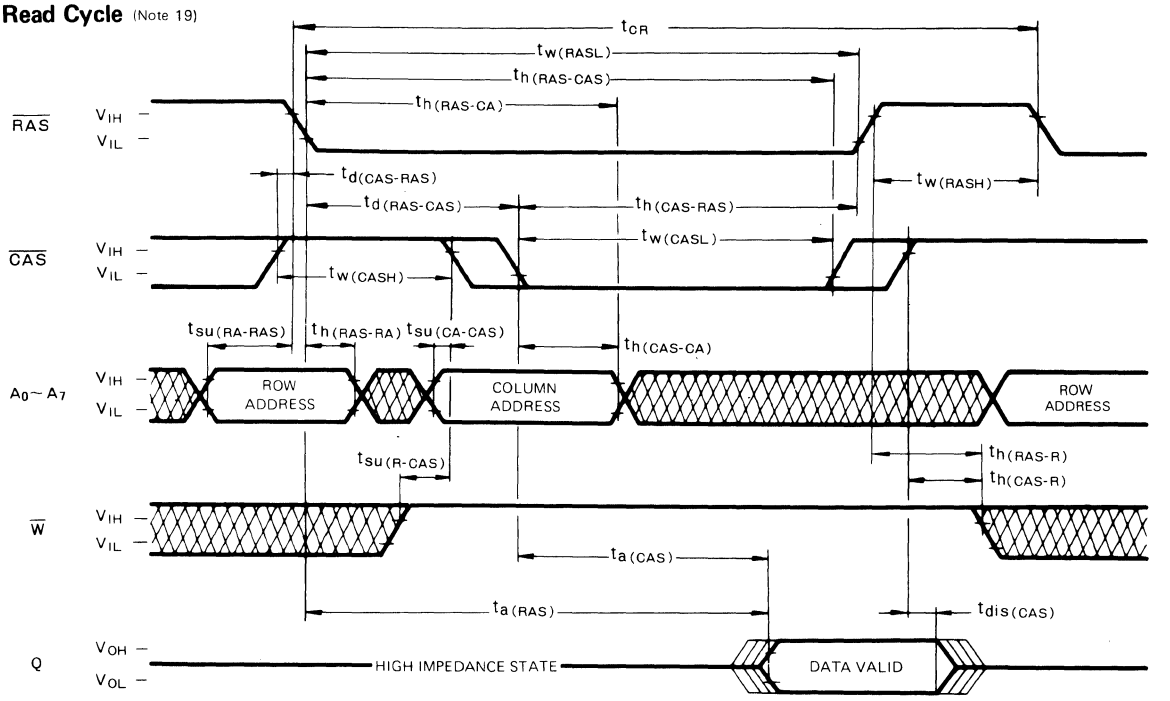
Symbol	Parameter	Alternative Symbol	MH6404AD1-15 Limits Min	Limits Max	Unit
$t_{C(REF)}$	Automatic Refresh cycle time	t_{FC}	260		ns
$t_{d(RAS-REF)}$	Delay time, $\overline{RAS}$ to $\overline{REF}$	t_{RFD}	100		ns
$t_{w(REFL)}$	$\overline{REF}$ low pulse width	t_{FP}	60	8000	ns
$t_{w(REFH)}$	$\overline{REF}$ high pulse width	t_{FI}	30		ns
$t_{d(REF-RAS)}$	Delay time, $\overline{REF}$ to $\overline{RAS}$	t_{FSR}	30		ns
$t_{su(REF-RAS)}$	$\overline{REF}$ pulse setup time before $\overline{RAS}$	t_{FRD}	295		ns

Self-Refresh Cycle

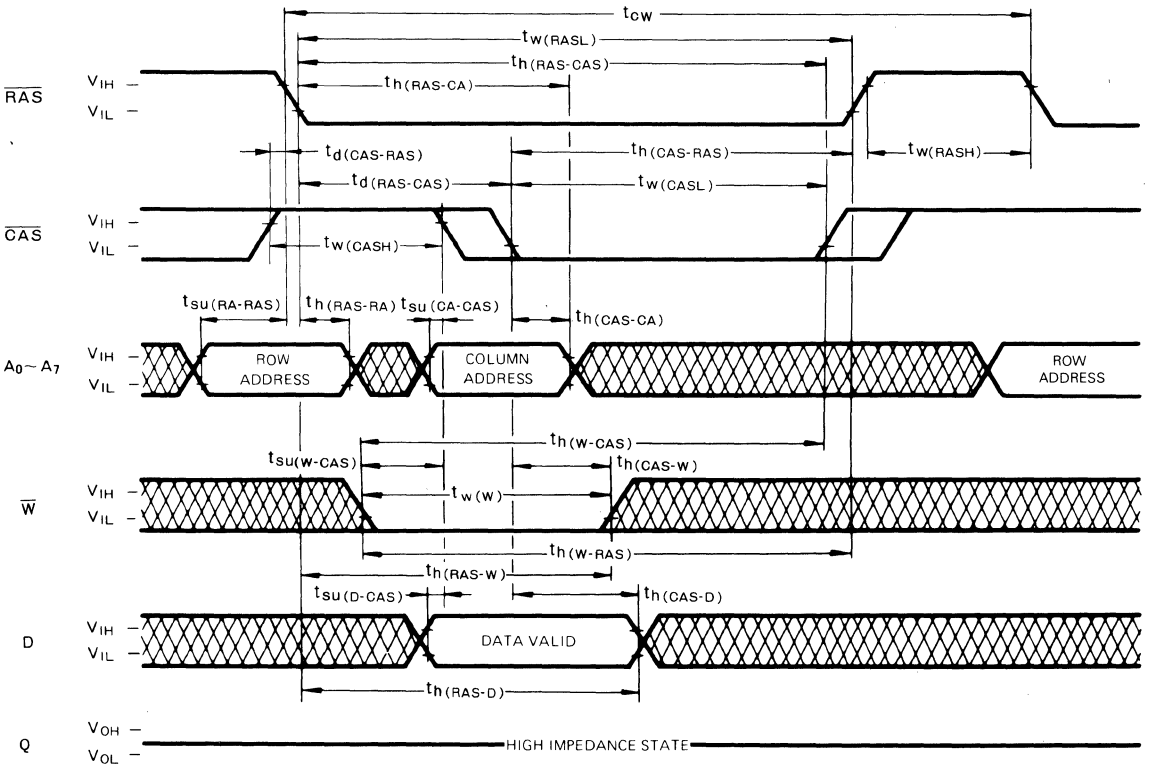
Symbol	Parameter	Alternative Symbol	MH6404AD1-15 Limits Min	Limits Max	Unit
$t_{d(RAS-REF)}$	Delay time, $\overline{RAS}$ to $\overline{REF}$	t_{RFD}	90		ns
$t_{w(REFL)}$	$\overline{REF}$ low pulse width	t_{FBP}	8000	∞	ns
$t_{d(REF-RAS)}$	Delay time, $\overline{REF}$ to $\overline{RAS}$	t_{FBR}	310		ns

TIMING DIAGRAMS (Note 18)

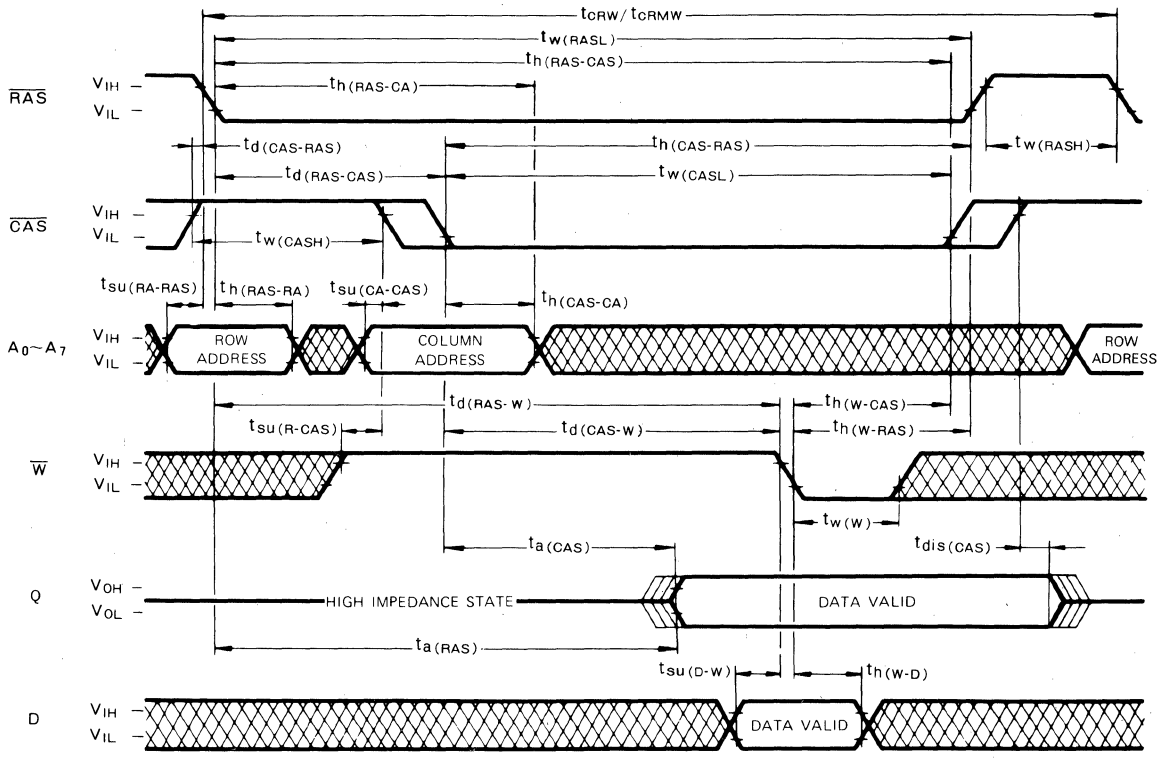
Read Cycle (Note 19)



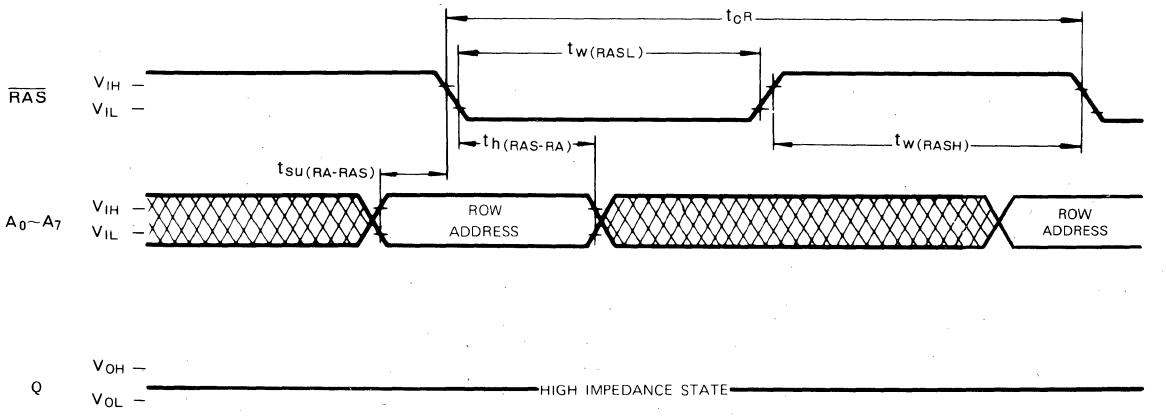
Write Cycle (Early Write) (Note 19)



Read-Write and Read-Modify-Write Cycles (Note 19)



RAS-Only Refresh Cycle (Note 20)



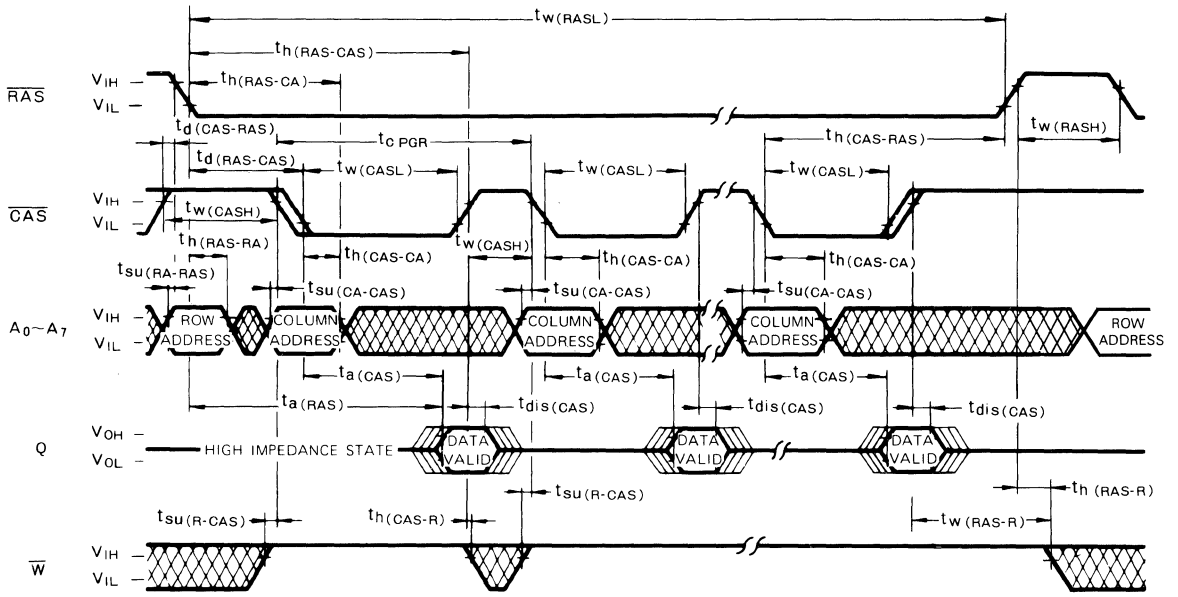
Note 18 — Indicates the don't care input

The center-line indicates the high-impedance state

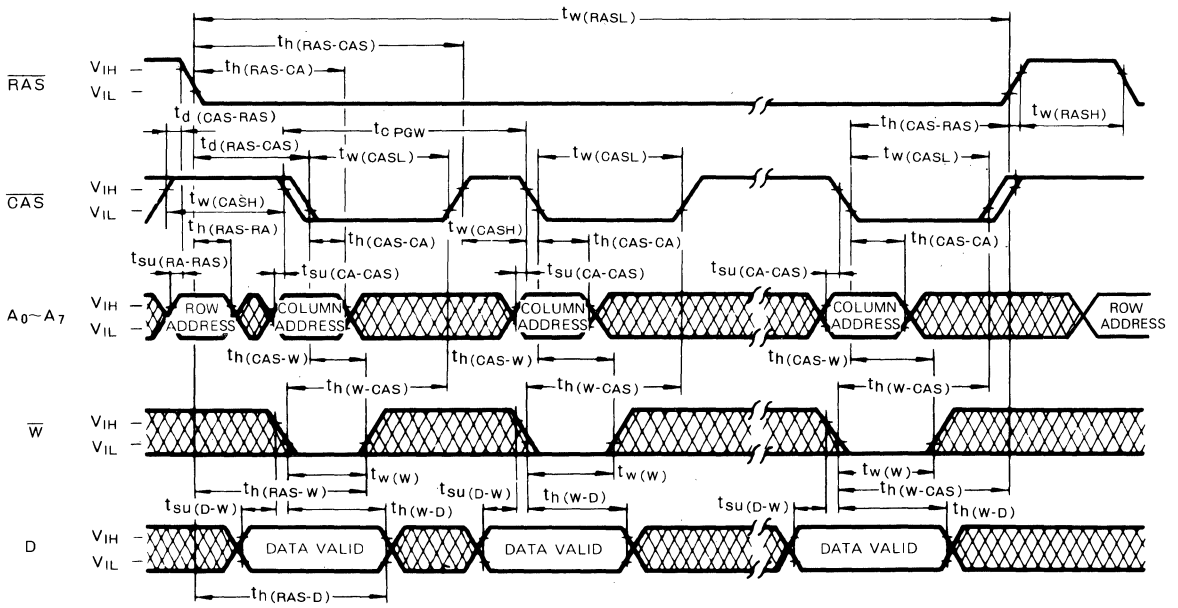
Note 19. $\overline{REF} = V_{IH}$

20. $\overline{CAS} = \overline{REF} = V_{IH}$, $\overline{W}$, D = don't care.
A_7 may be V_{IH} or V_{IL}.

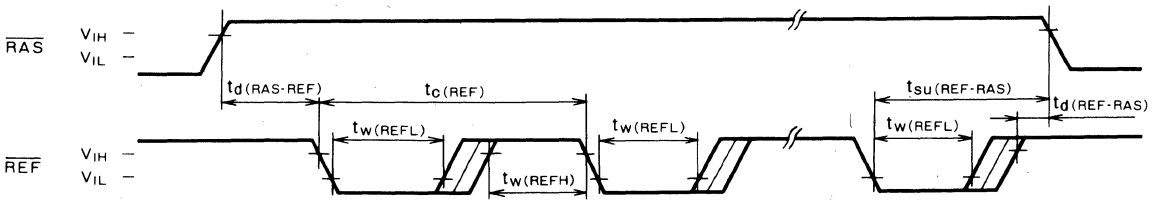
Page-Mode Read Cycle (Note 19)



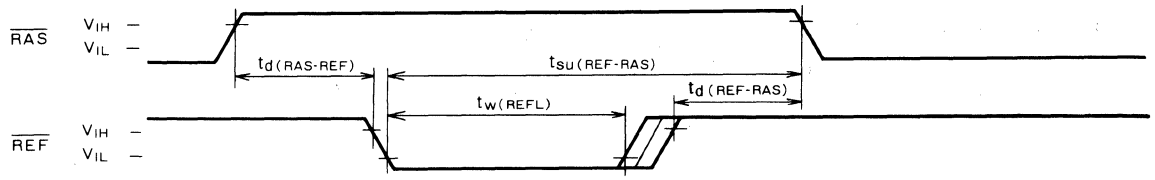
Page-Mode Write Cycle (Note 19)



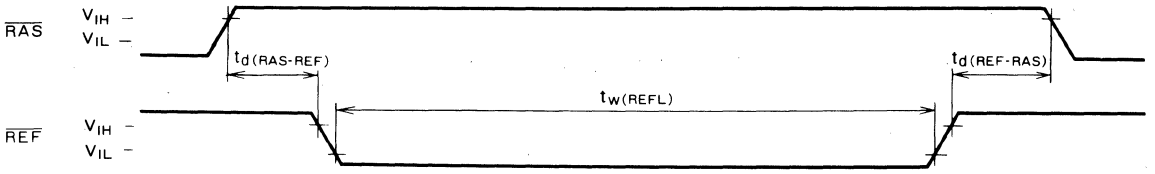
Automatic Pulse Refresh Cycle (Multiple Pulse) (Note 21)



Automatic Pulse Refresh Cycle (Single Pulse) (Note 21)

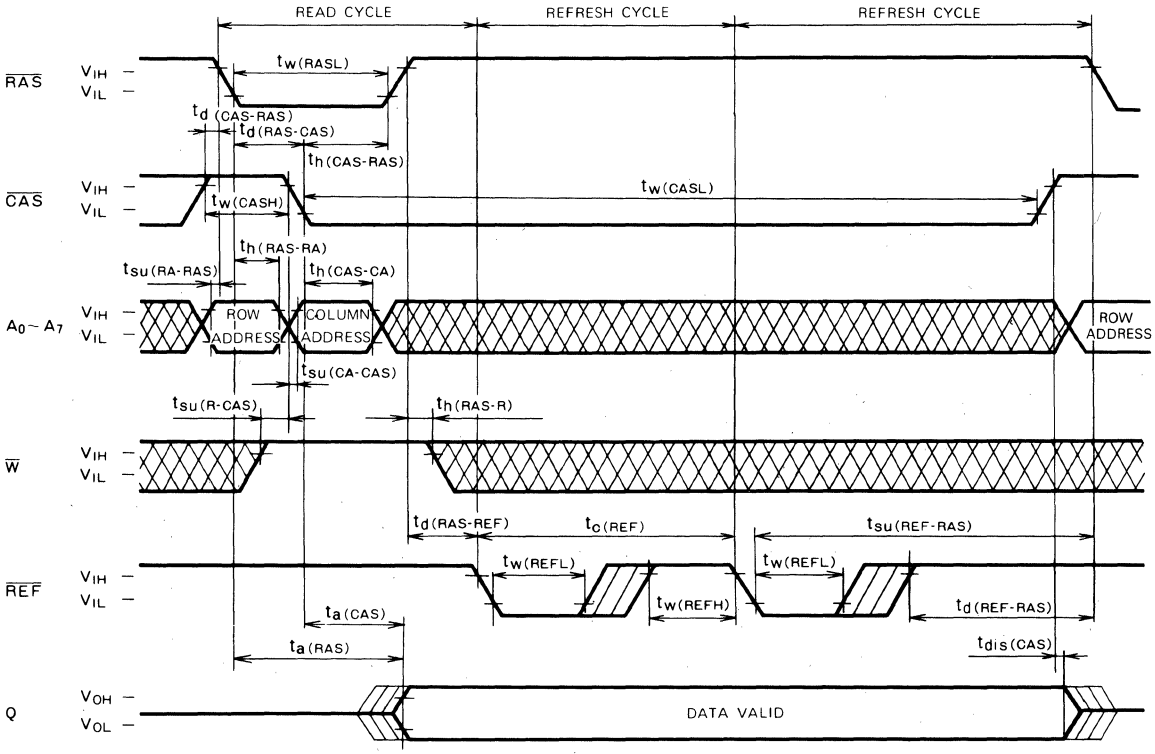


Self-Refresh Cycle (Note 21)

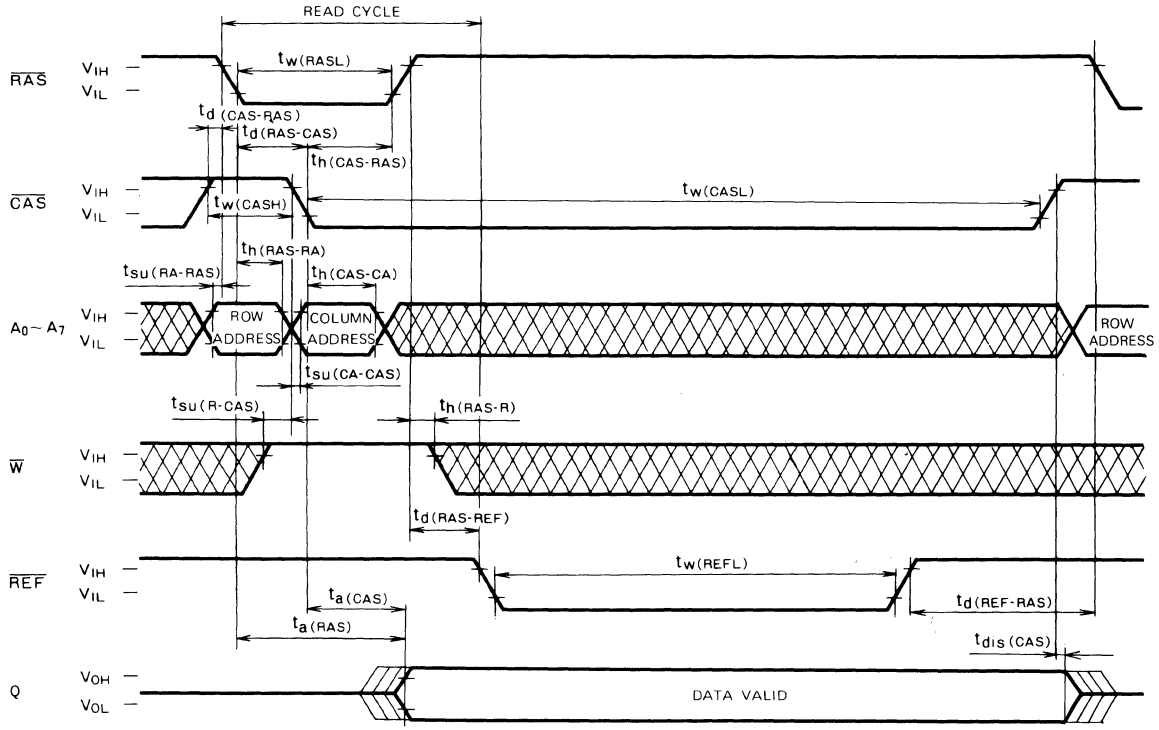


(Note 21) $\overline{CAS}$, Addresses, D and $\overline{W}$ are don't care.

Hidden Automatic Pulse Refresh Cycle



Hidden Self-Refresh Cycle (Note 22)



Note 22: If the pin 1 ($\overline{REF}$) function is not used, pin 1 may be left open (not connect).

Hidden Refresh Cycle (Note 19)