

MGFG5H1503

13.75 – 14.5 GHz BAND / 20W

Description

The MGFG5H1503, a 20W 4-stage GaN MMIC Power Amplifier including a linearizer, is designed as a driver amplifier for a 50W Internally Matched FET MGFK47G3745A.

Features

- High output power: 43dBm
- Input and output matched to 50Ohm
- DC block capacitors built in
- 0.25um GaN HEMT Technology
- Independently adjustable bias pins
- Compact metal package with screw holes

Application

- Transmitter for Ku-band SATCOM

Quality

- General & Industrial

Absolute Maximum Ratings (Ta=25°C)

Symbol	Parameter	Ratings	Unit
Vd	Drain to Source Voltage	30	V
Vg	Gate to Source Voltage	-10	V
VI	Linearizer Voltage	10	V
Pin	RF Input Power	30	dBm
Vd_on	Drain to Source Voltage under RF operation	27	V
Tch	Channel Temperature	230	°C
Tstg	Storage Temperature	-55 to 125	°C

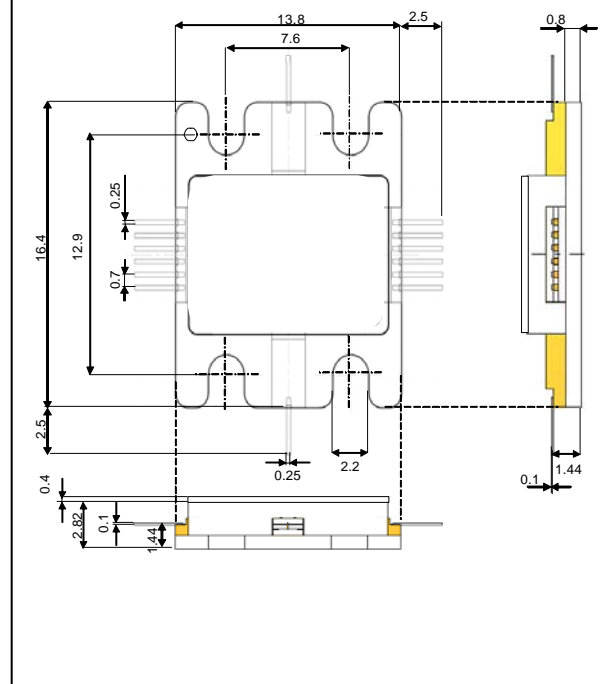
*1: Tc=25°C

Recommended Operating Conditions

Symbol	Parameter	Typ.	Unit
Vd	Drain Voltage	24	V
IdqB	Drain Current of buffer amp. without RF Drive	180	mA
Idq1	Drain Current of 1st stage without RF Drive	360	mA
Idq2	Drain Current of 2ndstage without RF Drive	720	mA
Idq3	Drain Current of 3rd stage without RF Drive	1440	mA
Vg	Gate Voltage	-2.7 to -1.7	V
VI	Control Voltage of Linearizer	0	V
Tch	Channel Temperature	≤175	°C

Outline Drawing

Unit: millimeter



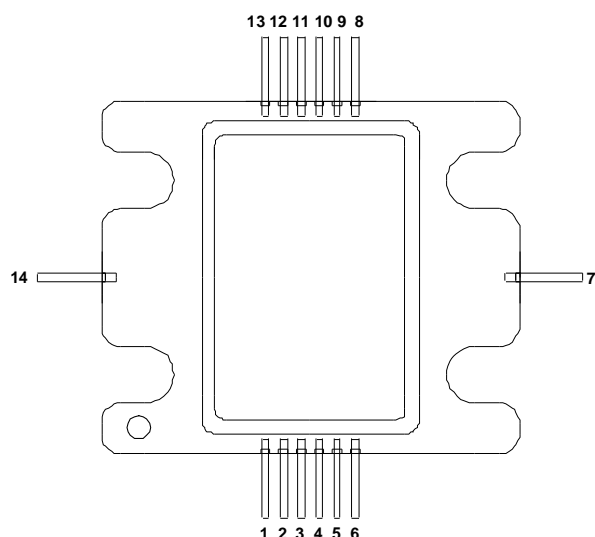
Electrical Characteristics

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Vg(off)	Gate to source cut-off voltage	Vd=24V, IdB=1.2mA Id1=2.4mA, Id2=4.8mA, Id3=9.6mA	-5	-	-2	V
Freq.	Operational Frequency	Vd=24V, VI=0V	13.75	-	14.5	GHz
Psat *1	Saturated Power	IdqB=180mA, Idq1=360mA,	41	43	-	dBm
Glp *2	Linear Power Gain	Idq2=720mA, Idq3=1440mA,	18	20	-	dB
IM3 *3	3 rd Order Intermodulation Distortion	*1: Pin=27dBm *2: Pin=0dBm *3: Pout=34dBm (SCL)			-25	dBc
Rth(ch-c) *4	Thermal resistance	ΔV_f method	-	1.2	1.5	°C/W

*4 :Channel-case

ESD *5	Class 0	Human Body Model (HBM) *5 : Standard: JEDEC
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Specifications are subject to change without notice.



Pin Number	Symbol	Description
1	VdB	Drain Voltage of Buffer Stage
2	Vd1	Drain Voltage of 1st Stage
3	Vg2	Gate Voltage of 2nd Stage
4	Vd2	Drain Voltage of 2nd Stage
5	Vg3	Gate Voltage of 3rd Stage
6	Vd3	Drain Voltage of 3rd Stage
7	Pout	RF Output
8	Vd3	Drain Voltage of 3rd Stage
9	Vg3	Gate Voltage of 3rd Stage
10	Vd2	Drain Voltage of 2nd Stage
11	Vd1	Drain Voltage of 1st Stage
12	VgB1	Gate Voltage of 1st Stage and Buffer Stage
13	VI	Control Voltage of Linearizer
14	Pin	RF Input

VI: Control voltage to optimize distortion characteristics such as AMAM, AMPM, and IMD.

Vg3 and Vd1,2,3 must be biased from both sides as follows:

Vd1: 2 and 11
Vd2: 4 and 10
Vg3: 5 and 9
Vd3: 6 and 8

Pin Configuration

Keep safety first in your circuit designs!

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