MGF1601

FOR MICROWAVE POWER AMPLIFIERS

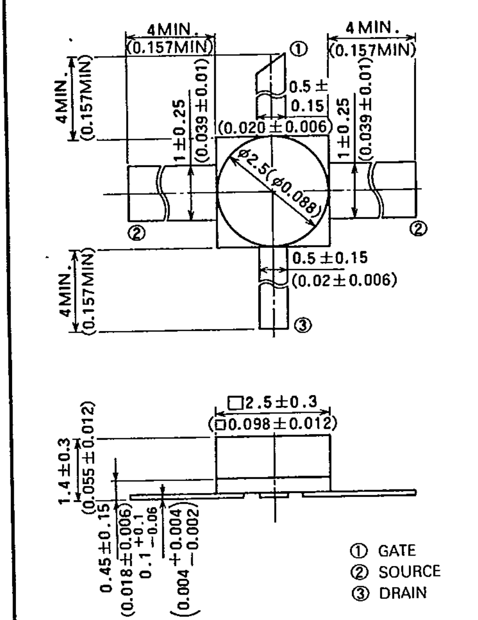
DESCRIPTION
The MGF1601, medium-power GaAs FET with an N-channel Schottky gate, is designed for use in S- to X-band amplifiers and oscillators.

FEATURES
- High output power at 1 dB gain compression
  P_{1dB} = 150 mW (TYP.) @f = 8 GHz
- High linear power gain
  G_{LP} = 8 dB (TYP.) @f = 8 GHz
- High reliability and stability

APPLICATIONS
S- to X-band medium-power amplifiers and oscillators.

QUALITY GRADE
- GG

OUTLINE DRAWING
Unit: millimeters (inches)



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Symbol	Parameter	Rating	Unit
V_{GDO}	Gate to drain voltage	−8	V
V_{GSO}	Gate to source voltage	−8	V
I_D	Drain current	250	mA
I_{GR}	Reverse gate current	−0.6	mA
I_{GF}	Forward gate current	1.5	mA
P_T	Total power dissipation	1	W
Tch	Channel temperature	150	°C
Tstg	Storage temperature	−55～+150	°C
Rth (ch-c)	Thermal resistance	125	°C/W

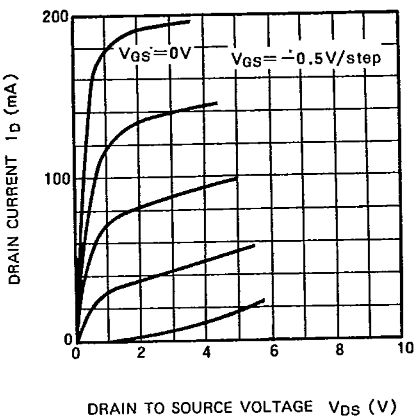
ELECTRICAL CHARACTERISTICS (Ta=25°C)

Symbol	Parameter	Conditions		Limits			Unit
				Min	Typ	Max	
$V_{(BR)GDO}$	Gate to drain breakdown voltage	$I_G=-200\mu A$		−8			V
$V_{(BR)GSO}$	Gate to source breakdown voltage	$I_G=-200\mu A$		−8			V
I_{GSS}	Gate to source leakage current	$V_{GS}=-3V$, $V_{DS}\doteq 0V$				20	μA
I_{DSS}	Saturated drain current	$V_{GS}=0V$, $V_{DS}\doteq 3V$		150	200	250	mA
$V_{GS(off)}$	Gate to source cut-off voltage	$V_{DS}=3V$, $I_D=100\mu A$		−1		−4.5	V
gm	Transconductance	$V_{DS}=3V$, $I_D=100mA$		60	90		mS
G_{LP}	Linear power gain	$V_{DS}=6V$, $I_D=100mA$	f= 8 GHz	6	8		dB
			f=12GHz		6		
P_{1dB}	Output power at 1 dB gain compression	$V_{DS}=6V$, $I_D=100mA$	f= 8 GHz	120	150		mW
			f=12GHz		100		

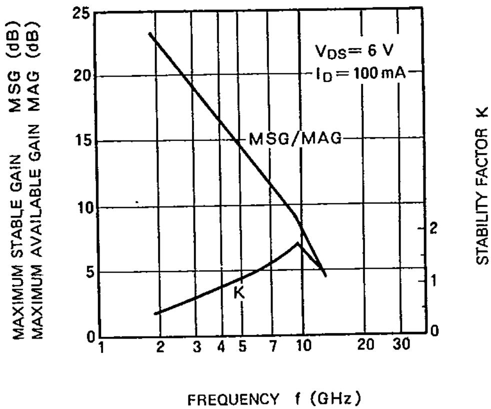
FOR MICROWAVE POWER AMPLIFIERS

TYPICAL CHARACTERISTICS (Ta=25°C)

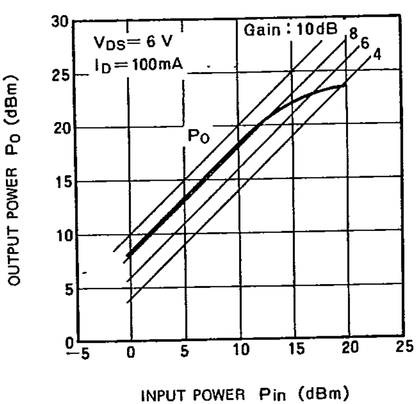
I_D vs. V_{DS}



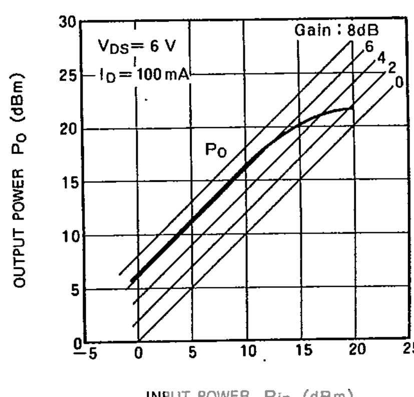
MSG, MAG, & K vs. f



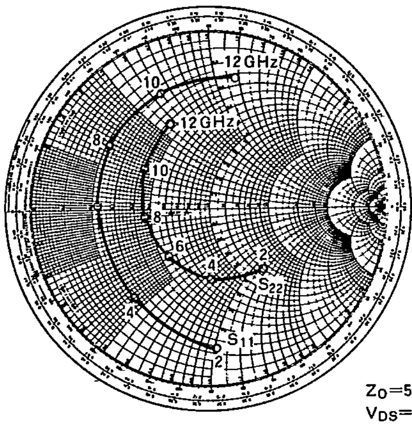
P_O vs. P_{in} (f = 8 GHz)



P_O vs. P_{in} (f = 12GHz)

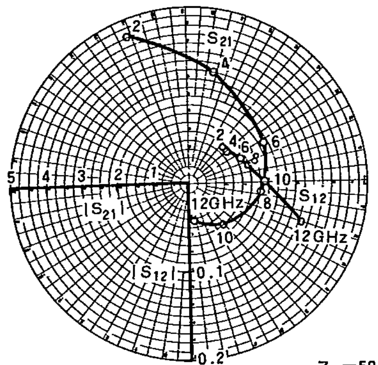


S_{11}, S_{22} vs. f



Z_O=50 Ω
V_{DS}= 6 V
I_D=100mA

S_{12}, S_{21} vs. f



Z_O=50 Ω
V_{DS}= 6 V
I_D=100mA

S PARAMETERS (T_a=25°C, V_{DS}=6V, I_D=100mA)

f (GHz)	S Parameters (TYP.)							
	S_{11}		S_{12}		S_{21}		S_{22}	
	Magn.	Angle (deg.)	Magn.	Angle (deg.)	Magn.	Angle (deg.)	Magn.	Angle (deg.)
2	0.813	−88.4	0.056	44.8	4.467	111.4	0.459	−48.7
4	0.672	−129.5	0.056	41.1	3.428	77.6	0.406	−90.0
6	0.660	177.8	0.064	24.8	2.661	29.1	0.364	−130.5
8	0.682	148.1	0.071	17.9	2.042	−9.3	0.378	−170.3
10	0.690	112.5	0.083	0	1.501	−51.2	0.380	148.5
12	0.696	79.3	0.135	−20.4	1.155	−81.2	0.382	114.9

HANDLING PRECAUTIONS FOR GaAs FETs

1. Check of Electrical Characteristics

(1) Measurement of DC Characteristics by Curve Tracer
Many curve tracers, if not properly grounded, exhibit a high leakage current from the high-voltage transformer, which can be a prime cause of failure or degradation of the FET. Measurement of the DC characteristics using a curve tracer is therefore not recommended. However, when tests using a curve tracer are required, first of all, check that the curve tracer is grounded to earth.

(2) Measurement of RF Characteristics
Before measurement, check that the measuring instruments are grounded to earth. Many instruments to measure RF characteristics such as RF power meters, network analyzers and so on, if not properly grounded to earth, sometimes allow a high AC leakage of up to several tens volts, which can be a cause of failure or degradation of the FET.

2. Installation of GaAs FET

When GaAs FET is soldered on a microstrip circuit, the following should be attended to,
(1) The ceramic cap of the FET package is fixed by resin. Therefore, avoid stress to the FET package.
(2) Properly ground the soldering iron to earth.
Leakage current from the soldering iron could cause failure or degradation of the FET.
(3) Solder the FET as promptly as possible at a low temperature. For a criterion, soldering in less than 5 seconds at a temperature of less than 250°C is recommended for each soldering process.

3. Bias Procedure and Conditions

When GaAs FET is biased, the following procedure is recommended.
(1) Slowly adjust the gate to source voltage V_{GS}, to about -1 V.
(2) Gradually increase the drain to source voltage, V_{DS}, from zero to a desired value.
(3) Adjust the drain current, I_D, to a desired value by controlling the gate to source voltage, V_{GS}.
When bias is released, the reverse procedure is recommended.
Be careful that the FET is not operated under conditions exceeding absolute maximum ratings.

4. Guaranteed Characteristics

All the graphic characteristics illustrated in this catalog are typical examples. The characteristics of individual devices as specified in the tables of absolute maximum ratings and electrical characteristics are guaranteed under the specified conditions.