8/16-bit Data Bus Flash Memory Card

MF82M1-GMCAVXX
MF84M1-GMCAVXX
MF88M1-GMCAVXX
MF816M-GMCAVXX
MF820M-GMCAVXX
MF832M-GMCAVXX
MF82M1-GNCAVXX
MF84M1-GNCAVXX
MF88M1-GNCAVXX
MF816M-GNCAVXX
MF820M-GNCAVXX
MF832M-GNCAVXX

Connector Type

Two- piece 68-pin

DESCRIPTION

The MF8XXX-GMCAVXX is a flash memory card which uses eight-megabit or sixteen megabit flash electrically erasable and programmable read only memory IC's as common memory and a 64-kilobit electrically erasable and programmable read only memory as attribute memory.
The MF8XXX-GNCAVXX is a flash memory card which uses eight-megabit or sixteen megabit flash electrically erasable and programmable read only memory IC's.

FEATURES

- 68 pin JEIDA/PCMCIA
- 8/16 controllable data bus width
- Buffered interface
- TTL interface level
- Program/erase operation by software command control
- 100,000 program/erase cycles
- Write protect switch
- Operating temperature =0 to 70°C
- .No Vpp required (5V Vcc only operation)

APPLICATIONS

- Notebook computers Printers
- Industrial machines

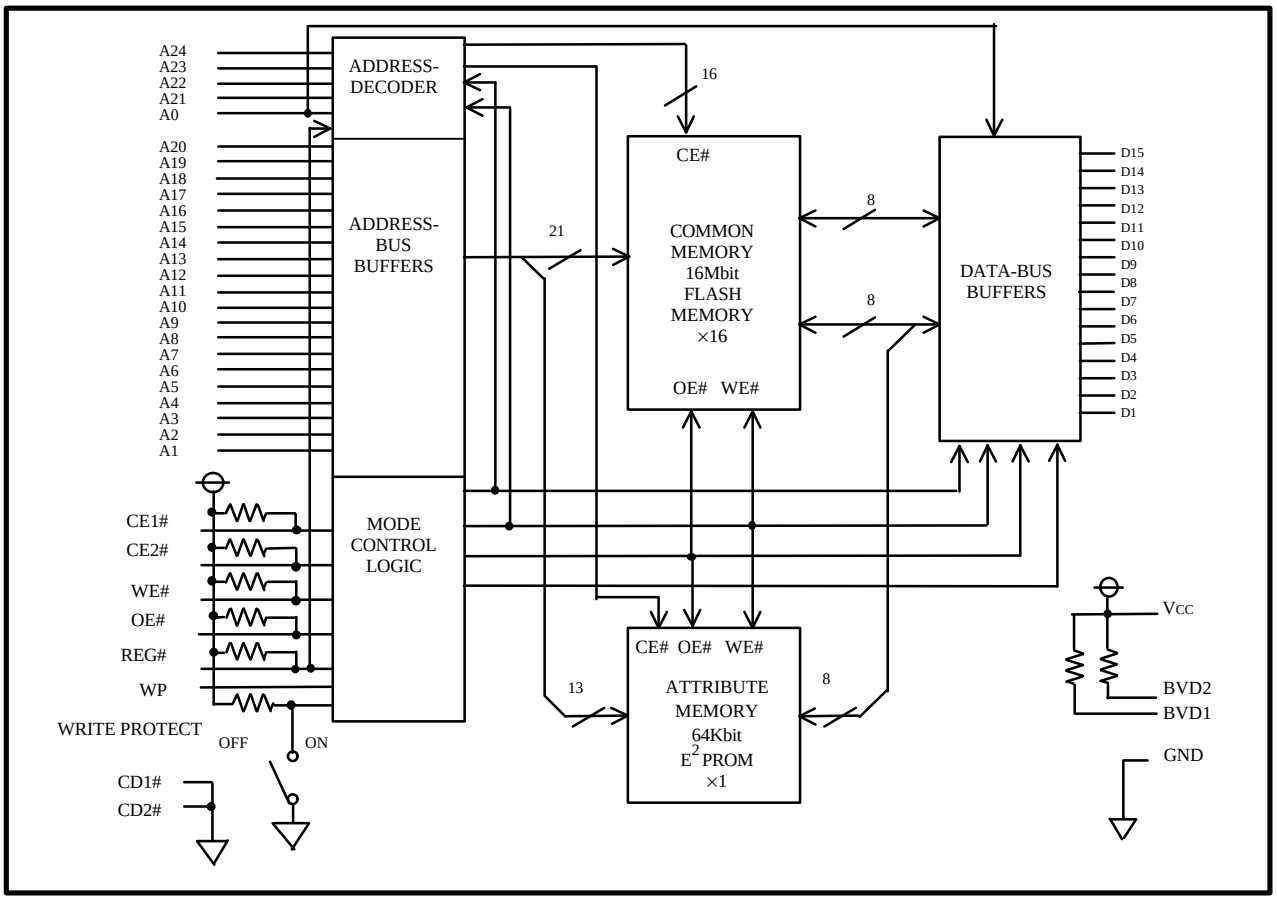
PRODUCT LIST

Item / Type name	Memory capacity	Attribute memory	Data bus width(bits)	Access time (ns)	Memory IC's	Outline drawing
MF82M1-GMCAVXX	2MB	Yes	8/16	150	8Mbit	68P-013
MF84M1-GMCAVXX	4MB				16Mbit	
MF88M1-GMCAVXX	8MB					
MF816M-GMCAVXX	16MB					
MF820M-GMCAVXX	20MB					
MF832M-GMCAVXX	32MB					
MF82M1-GNCAVXX	2MB	No(FFh)			8Mbit	
MF84M1-GNCAVXX	4MB				16Mbit	
MF88M1-GNCAVXX	8MB					
MF816M-GNCAVXX	16MB					
MF820M-GNCAVXX	20MB					
MF832M-GNCAVXX	32MB					

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3	Data I/O	36	CD1#	Card detect 1
3	D4		37	D11	Data I/O
4	D5		38	D12	
5	D6		39	D13	
6	D7		40	D14	
7	CE1#	Card enable 1	41	D15	
8	A10	Address input	42	CE2#	Card enable 2
9	OE#	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A9		45	NC	
12	A8		46	A17	Address input
13	A13		47	A18	
14	A14		48	A19	
15	WE#	Write enable	49	A20	
16	NC	No connection	50	A21	A21 (NC for ≤ 2 MB types)
17	VCC	Power supply voltage	51	VCC	Power supply voltage
18	NC	No connection	52	NC	No connection
19	A16	Address input	53	A22	A22 (NC for ≤ 4 MB types)
20	A15		54	A23	A23 (NC for ≤ 8 MB types)
21	A12		55	A24	A24 (NC for ≤ 16 MB types)
22	A7		56	NC	No connection
23	A6		57	NC	
24	A5		58	NC	
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	REG#	Attribute memory select
28	A1		62	BVD2	Battery voltage detect 2
29	A0		63	BVD1	Battery voltage detect 1
30	D0	Data I/O	64	D8	Data I/O
31	D1		65	D9	
32	D2		66	D10	
33	WP	Write protect	67	CD2#	Card detect 2
34	GND	Ground	68	GND	Ground

BLOCK DIAGRAM (MF832M-GMCAVXX)



FUNCTIONAL DESCRIPTION

The operating mode of the card is determined by five active low control signals (REG#, CE1#, CE2#, OE#, WE#), and control registers located in each memory IC.

Common memory function

When the REG# signal is set to a high level common memory is selected.

-Read mode

When each memory IC in the card are switched, the control registers of each memory IC are set to read only mode.
Operation of the card then depends on the four possible combinations of CE1# and CE2# (note WE# should be set to a high level when the device is in read mode except during combination (4) where it's condition is unimportant) :

(1) If CE1# is set to a low level and CE2# is set to a high level, the card will work as an eight bit data bus width card. Data can be accessed via the lower half of the data bus (D0 to D7).
(2) If both CE1# and CE2# are set to a low level, data will be accessible via the full sixteen bit data bus width of the card. In this mode LSB of address bus (A0) is ignored.
(3) If CE1# is set to a high level and CE2# is set to a low level the odd bytes (only) can be accessed through upper half of the data bus (D8 to D15). This mode is useful when handling the odd (upper) bytes in a sixteen bit interface system. Note that A0 is also ignored in this operating condition.
(4) If CE1# and CE2# are set to a high level, the card will be in standby mode where it consumes low power. The data bus is kept high impedance.

When OE# is set to a low level data can be read from the card, depending on the address applied and the setting of CE1# and CE2# as mentioned above, except under combination (4) When OE# is set to a high level and WE# is set to a high level the card is in an output disable mode

-Write mode

By using the 4 combinations of CE1# and CE2# as described under Read only above the appropriate Data Out and Command/Data In bus selection can be made.

If OE# is set to a high level and WE# set to a low level, the control register will latch command data applied at the rising edge of the WE# signal. Note that more than one bus cycle may be required to latch the command and/or the related data-please refer to the Command Definition table.

If OE# is set to a low level and WE# is set to a high level the card data can be read from the card depending on the condition of the control register.

After latching the command data, the card will go into programming, erasure or other operation mode. For details please refer to the Command Definition table, each individual command's definition and the programming and erasure algorithms.

Attribute memory function

When the REG# signal is set to a low level attribute memory is selected.

GM series

The card includes a byte wide attribute memory consisting of 8K bytes of E^2PROM located at the even addresses when the card is in the 8 bit operating mode. It is located at sequential addresses on the lower half of the data bus when the card is in 16 bit operating mode i.e. A0 is ignored.

To access the attribute memory, first set CE1# and CE2#. Set CE1# to low level and CE2# to high level for 8 bit mode or CE1# and CE2# to low level for 16 bit mode. Then select the required address. Note please take care that in 8 bit mode A0 must be set low for attribute memory access i.e. an even address is applied. In 16 bit mode it is not important whether A0 is high or

low. Data can then be read by setting OE# to a low level with WE set to a high level.

Writing to the attribute memory can be achieved in byte mode only. To write to attribute memory set OE# to high level and WE# to low level. The data to be written will be latched at the rising edge of WE#. Then, unless WE# changes back
from high level to low level over 100 µs an automatic erase/program operation starts which will complete within 10ms.

Please also remember that for attribute memory A0 is not applicable and it should be set to low, even addressing only, in 8 bit mode or ignored for 16 bit mode.

GN series

The card then outputs FFh on the lower half of the data bus (D0 to D7) when the following conditions are applied;
(1)CE1#=low level,CE2#=high level,OE#=low level,WE#=high level,A0=low level.
(2)CE1#=low level,CE2#=low level,OE#=low level,WE#=high level.

Write protect mode

The card has a write protect switch on the opposite edge to the connector edge. When it is switched on, the card will be placed into a write protect mode, where data can be read from the card but it cannot be written to it. The WP output pin is set to a high level when the card is in write protect mode and V_{CC} is applied. When the card is not in write protect mode the WP output pin is set to a low level when V_{CC} is applied. By reading the state of the WP output the host system can easily check whether the card is in write protect mode or not.

FUNCTION TABLE (COMMON MEMORY)

Mode	REG#	CE2#	CE1#	OE#	WE#	A0	I/O (D15 to D8)	I/O (D7 to D0)
Standby	H	H	H	X	X	X	High-Z	High-Z
Read A(16-bit)	H	L	L	L	H	X	Odd byte data out	Even byte data out
Read B(8-bit)	H	H	L	L	H	L	High-Z	Even byte data out
	H	H	L	L	H	H	High-Z	odd byte data out
Read C(8-bit)	H	L	H	L	H	X	Odd byte data out	High-Z
Write A(16-bit)	H	L	L	H	L	X	Command or odd byte data in	Command or even byte data in
Write B(8-bit)	H	H	L	H	L	L	High-Z	Command or even byte data in
	H	H	L	H	L	H	High-Z	Command or odd byte data in
Write C(8-bit)	H	L	H	H	L	X	Command or odd byte data in	High-Z
Output disable	H	X	X	H	H	X	High-Z	High-Z

Note 1 : H=V_{IH}, L=V_{IL}, X=V_{IH} or V_{IL}, High-Z= High-impedance
To operate refer to the command definition, algorithms and so on.

FUNCTION TABLE (ATTRIBUTE MEMORY)

GM series

Mode	REG#	CE2#	CE1#	OE#	WE#	A0	I/O (D15 to D8)	I/O (D7 to D0)
Standby	L	H	H	X	X	X	High-Z	High-Z
Read A(16-bit)	L	L	L	L	H	X	Data out(not valid)	Even byte data out
Read B	L	H	L	L	H	L	High-Z	Even byte data out
(8-bit)	L	H	L	L	H	H	High-Z	Data out(not valid)
Read C(8-bit)	L	L	H	L	H	X	Data out(not valid)	High-Z
Write A(16-bit)	L	L	L	H	L	X	Odd byte data in (not valid)	Even byte data in
Write B	L	H	L	H	L	L	High-Z	Even byte data in
(8-bit)	L	H	L	H	L	L	High-Z	Odd byte data in (not valid)
Write C(8-bit)	L	L	H	H	L	X	Odd byte data in (not valid)	High-Z
Output disable	L	X	X	H	H	X	High-Z	High-Z

GN series

Mode	REG#	CE2#	CE1#	OE#	WE#	A0	I/O (D15 to D8)	I/O (D7 to D0)
Standby	L	H	H	X	X	X	High-Z	High-Z
Read A(16-bit)	L	L	L	L	H	X	Data out(not valid)	Data out (FFh)
Read B	L	H	L	L	H	L	High-Z	Data out (FFh)
(8-bit)	L	H	L	L	H	H	High-Z	Data out(not valid)
Read C(8-bit)	L	L	H	L	H	X	Data out(not valid)	High-Z
Output disable	L	X	X	H	H	X	High-Z	High-Z

Note 2 : H=V_{IH}, L=V_{IL}, X=V_{IH} or V_{IL}, High-Z= High-impedance

COMMAND DEFINITION

The corresponding memories of the card are set to read/write mode and the operation is controlled by the software command written in the control register.

COMMAND DEFINITION TABLE

Command	Bus cycles	First bus cycle			Second bus cycle			
		Mode	Address	Data in	Mode	Address	Data in	Data out
Read/Reset	1	Write	ZA	FFh(FFFFh)	-	-	-	-
Programme setup/ Programme	2	Write	PA	40(4040)h	Write	PA	PD	-
Erase Setup/ Erase Confirm	2	Write	BA	20(2020)h	Write	BA	D0(D0D0)h	-
Programme Suspend/Resume	2	Write	PA	B0(B0B0)h	Write	PA	D0(D0D0)h	-
Erase Suspend/ Resume	2	Write	BA	B0(B0B0)h	Write	BA	D0(D0D0)h	-
Read Status Register	2	Write	ZA	70(7070)h	Read	ZA	-	RD
Clear Status Register	1	Write	ZA	50(5050)h	-	-	-	-
Read Device Identifier Code	2	Write	ZA	90(9090)h	Read	DIA	-	DID

Note 3: Indicates the basic functions of commands and should not write another commands.
Refer to the algorithms to operate.
Signal status is defined in function table and bus status.
Parenthesized data shows the data for 16 bit mode operation.
ZA=an address of a memory zone (Please refer to the memory zone)
PA=Programming address
PD=Programming data
BA=An address of a memory block (Please refer to the memory block)
RD=Data of status Register
DIA=Device identifier address
000000h for manufacturer code 000002h for device code
DID=Device identifier data
2MB=manufacturer code : 89 (8989)h device code : A6h (A6A6)h
Others=manufacturer code : 89 (8989)h device code : AA (AAAA)h

Read/Reset

The memory in the card is switched to read mode by writing FFh (FFFFh for 16 bit operation) into the control resister. This mode is maintained until the contents of register are changed. This mode needs to be written to every memory zone to which access is required.

Programme Setup/Programme

The setup programme command sets up the card for programming. It is applied when 40h (4040h for 16 bit operation) is written to control register. Programming will take place automatically after latching the address and data which are applied at the rising edge of WE#.
The completion of programme can be confirmed by reading status register.
(For details please refer to the algorithm)

Erase Setup/Erase confirm

The erase setup is a command to set up the memory block for erasure. Writing setup erase command 20h (2020h for 16 bit operation) in the control register followed by erase confirm command D0h (D0D0h for 16 bit operation) will initiate a erasure operation. Erasing will take place automatically after the rising edge of WE# controlled by a internal timer. The completion of erase can be confirmed by reading status register. (For details please refer to the algorithm)
These commands will not erase all the data of a memory card and should be repeated for all the required memory blocks. At an eight bit access mode it should be noticed that the erasure of a memory block will result in odd byte or even byte erasure.

Erase Suspend/Erase Resume
The erase suspend command B0h (B0B0h for 16 bit operation) is a command to generate erase interruption and to read data from another block of selected memory zone. By writing in the control register erase resume command D0h (D0D0h for 16 bit operation), the memory block will continue the erase operation.
These commands must be executed in erase algorithm.
(For details please refer to the algorithm)

Read Status Register
The Read status register is a command to read the status register's data and to make sure programme or erase operations complete successfully. The data of status register can be read after writing 70h (7070h for 16 bit operation) in the control register. The register's read data is latched on the falling edge of OE#. At programme or erase, the status register's data must be read to verify the results.

Clear Status Register
The clear status register command will clear data of status register. It is applied when 50h (5050h for 16 bit operation) is written to the control register. If an error occurred during programme or erase, the status register must be cleared before retrying programme or erase.

Read Device Identifier Codes
The read device identifier codes command is implemented by writing 90h (9090h for 16 bit operation) to the command register. After writing the command, manufacturer code can be read at the address of 000000h of the zone and device code can be read at the address 000002h of the zone. Each card uses the same type of memory throughout and each memory zone will respond the same code.
(Do not apply high voltage to A10 pin in order to try and read the device identifier codes as this will result in the card being destroyed.)

STATUS REGISTER
When operating programme or erase, it is necessary to read status register data and to transact these bit. Each memory IC used in this card has internal status register to make sure programme or erase operations complete successfully.

7 (15) BIT	6 (14) BIT	5 (13) BIT	4 (12) BIT	3 (11) BIT	2 (10) BIT	1,0 (9,8) BIT
Programme/ Erase Status Bit	Erase Suspend Bit	Erase Error Bit	Programme Error Bit	Vcc Error Bit	Programme Suspend Bit	Reserved

Note 4: ( ) ; for 16 bit operation

Bit ; Field name

7(15) BIT ; Programme/Erase Status Bit
0=Busy (in programming/erasing) 1=Ready

6(14) BIT ; Erase Suspend Bit
1=Erase Suspended

5(13) BIT ; Erase Error Bit
1=Erase Error

4(12) BIT ; Programme Error Bit
1=Programme Error

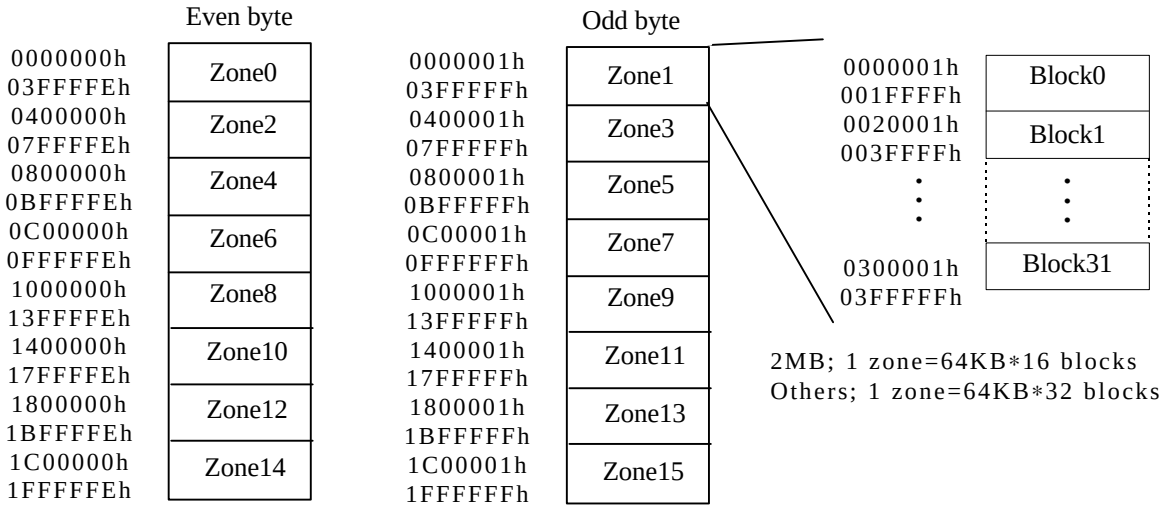
3(11) BIT ; Vcc Error
1=Error of voltage at Vcc

2(10) BIT ; Programme Suspend Bit
1=Programme Suspended

1,0(9,8) BIT ; Reserved for future

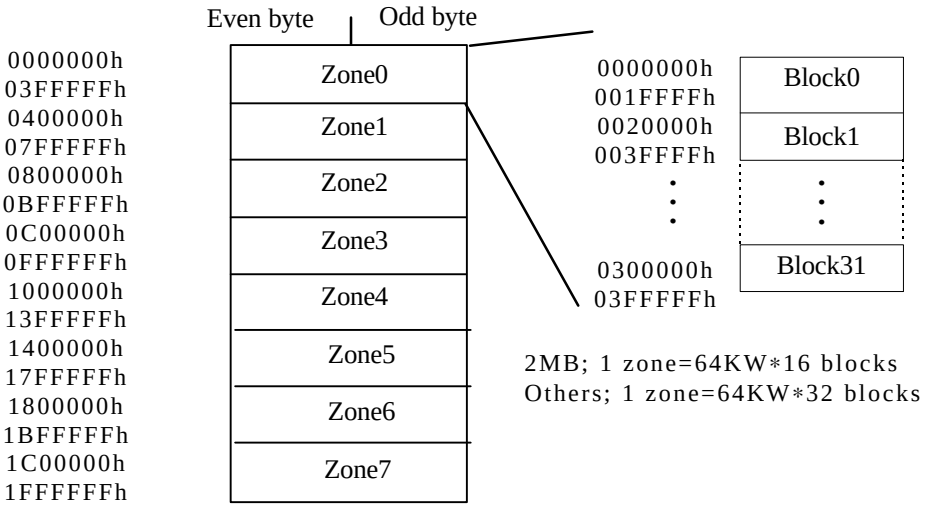
MEMORY ZONE AND BLOCK

8 bit mode



Note 5 : 2MB;1 zone=0h to 1FFFFFh address
Others;1 zone=0h to 3FFFFFh address
Zone 2 to 15 do not exist in 2MB
Zone 2 to 15 do not exist in 4MB
Zone 4 to 15 do not exist in 8MB
Zone 8 to 15 do not exist in 16MB
Zone 10 to 15 do not exist in 20MB

16 bit mode



Note 6 : 2MB;1 zone=0h to 1FFFFFh address
Others;1 zone=0h to 3FFFFFh address
Zone 1 to 7 do not exist in 2MB
Zone 1 to 7 do not exist in 4MB
Zone 2 to 7 do not exist in 8MB
Zone 4 to 7do not exist in 16MB
Zone 5 to 7 do not exist in 20MB

PROGRAMME ALGORITHM

PROGRAMME

8 bit Operation

Write the programme setup command (40h) to the address to be programmed. The next write sequence will initiate the programming operation which will end automatically as this period being controlled by an internal timer and the data will be programmed.
To make sure that the data is programmed correctly read data of the status register. The read status register command (70h) may or may not be applied to read the data after the programme data input. If the data is programmed step address and programme data according to the above sequence.
The next address to be programmed should be written with in a memory zone. After the last programming operation, write the reset command (FFh) in control register of the programmed memory zones.
When overwriting bits programmed as “0”, programme “1” or the device reliability is affected.

16 bit operation

The algorithm of 16 bit programming is almost same as the 8 bit programming. (Please refer to the algorithm and the status of bus at programming)

PROGRAMME SUSPEND

8 bit Operation

The programme suspend is a command to generate zone programme interruption in order to read or data from another block of the selected memory zone. It is necessary to write the erase suspend command (B0h) in the programme algorithm.
The execution of the programme suspend can be confirmed by reading data of the status register.
Then it is necessary to write the read command (FFh) in control register in order to read data, after reading the status register’s data.
After the programme resume command (D0h) is written in the control register, the memory zone will continue the programme operation.

16 bit Operation

Most of the algorithm of 16 bit programme suspending is same as the one of the 8 bit programme suspending.
(Please refer to the algorithm and the state of bus at programme suspending.)

ERASE ALGORITHM

ERASE

8 bit Operation

Write the erase setup command (20h) and erase confirm command (D0h) for the applicable block address.
An erasure operation will then commence which will be finished in 1.6s typical or less this being automatically controlled by an internal timer.
To make sure that the data is erased correctly and read data of the status register.
The read status register command (70h) may or may not be applied to read the data after the erase confirm command.
After erasure has completed write the reset command (FFh) to the control register, proceed to the erase operation for the next memory block.

16 bit Operation

Most of the algorithm of 16 bit erasure is same as the one of the 8 bit erasure.
(Please refer to the algorithm and the state of bus at erasure.)

ERASE SUSPEND

8 bit Operation

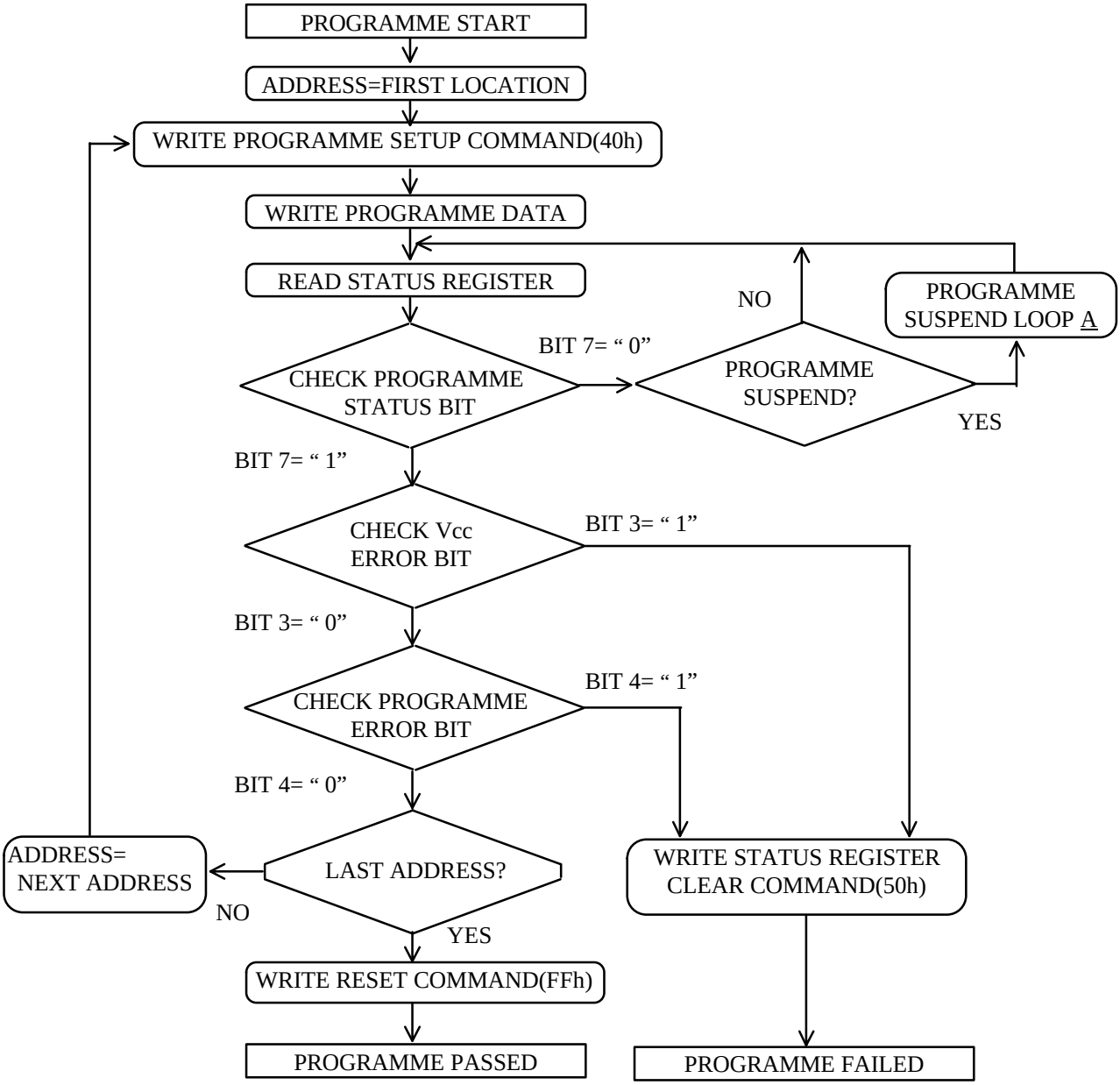
The erase suspend is a command to generate block erase interruption in order to read or programme data from another block of the selected memory zone. It is necessary to write the erase suspend command (B0h) in the erase algorithm.
The execution of the erase suspend can be confirmed by reading data of the status register.
Then it is necessary to write the read command (FFh) in control register in order to read data, after reading the status register’s data.
After the erase resume command (D0h) is written in the control register, the memory block will continue erase operation.

16 bit Operation

Most of the algorithm of 16 bit erase suspending is same as the one of the 8 bit erase suspending.
(Please refer to the algorithm and the state of bus at erase suspending.)

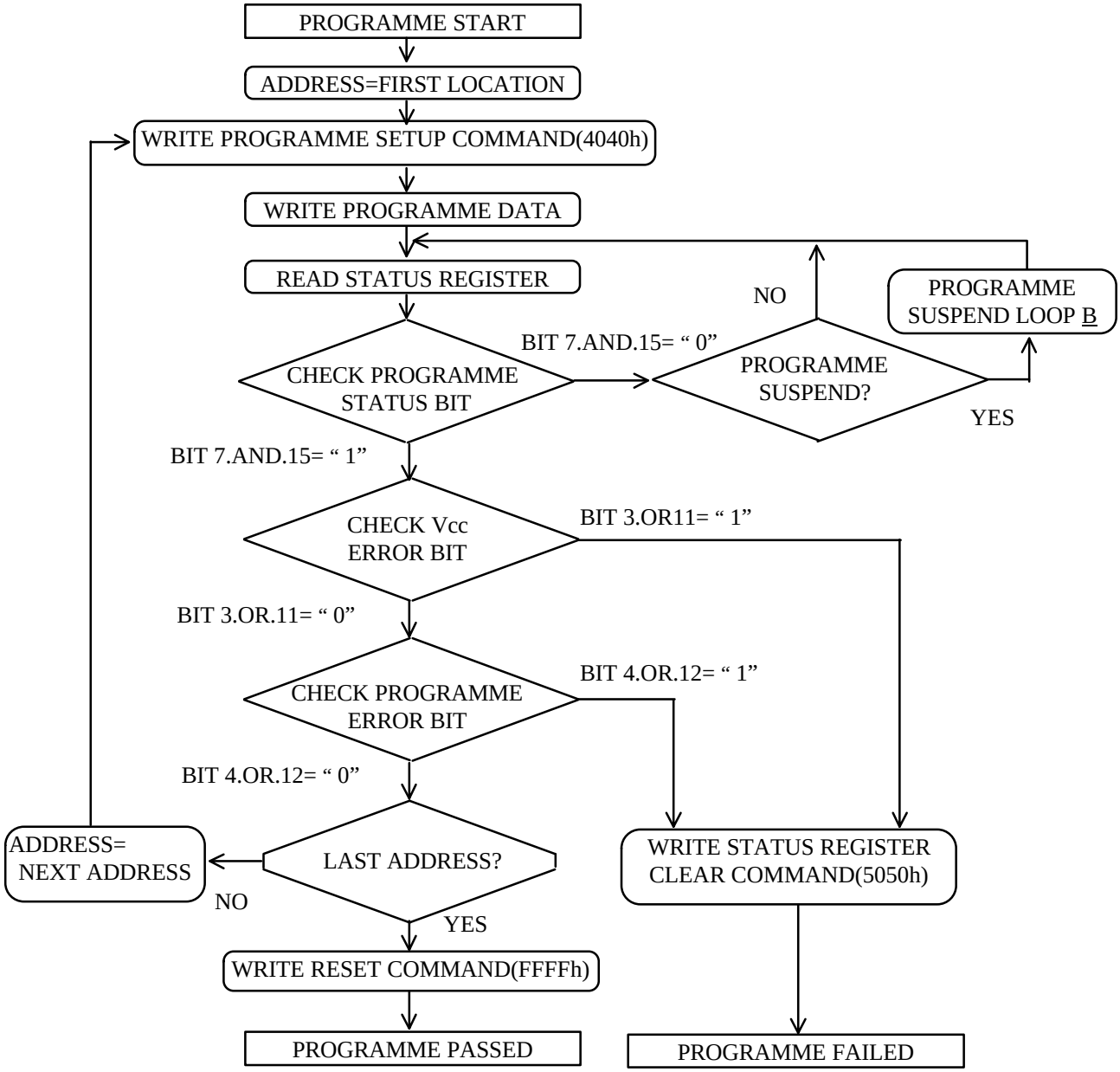
PROGRAMME ALGORITHM

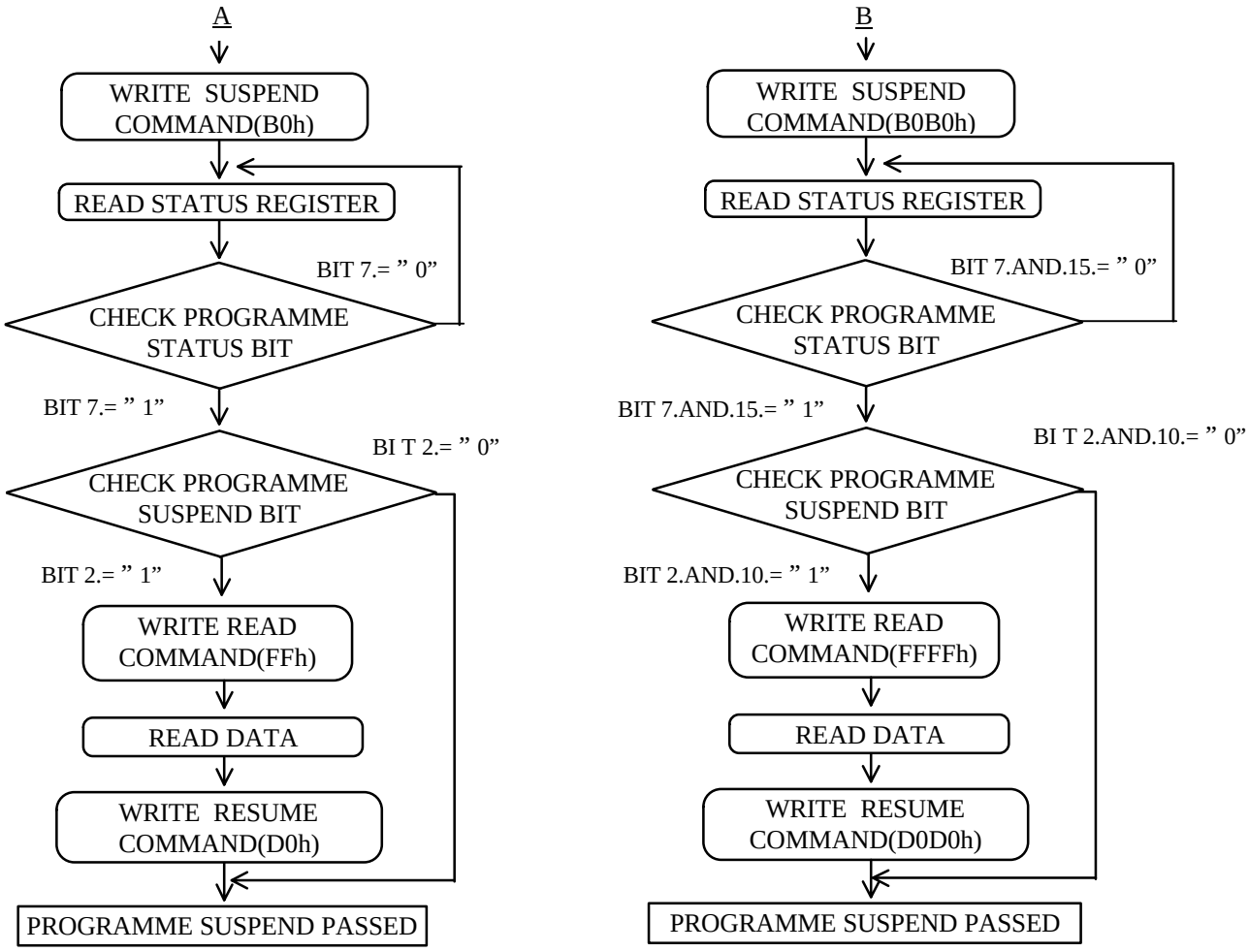
8 bit mode



PROGRAMME ALGORITHM

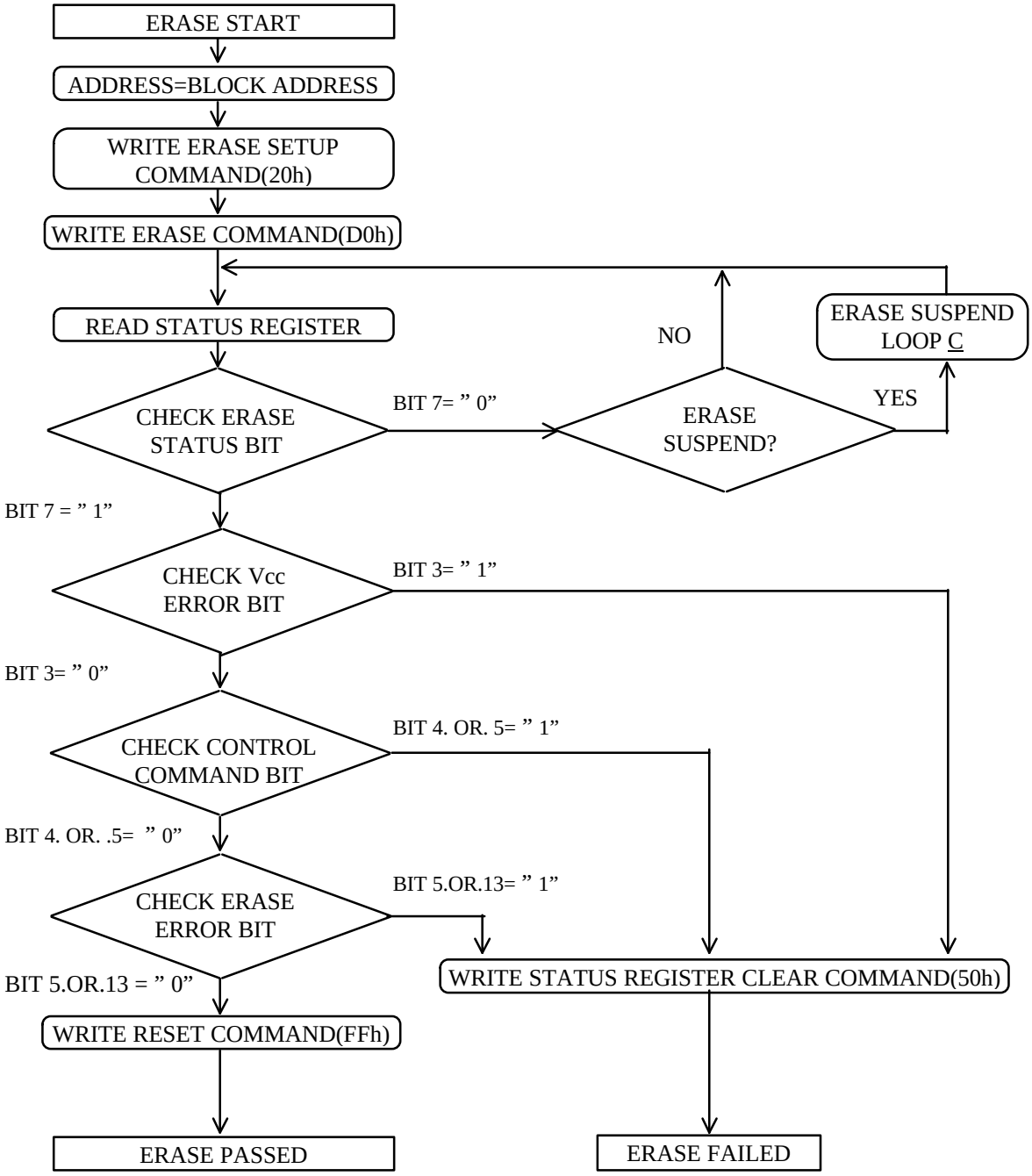
16 bit mode





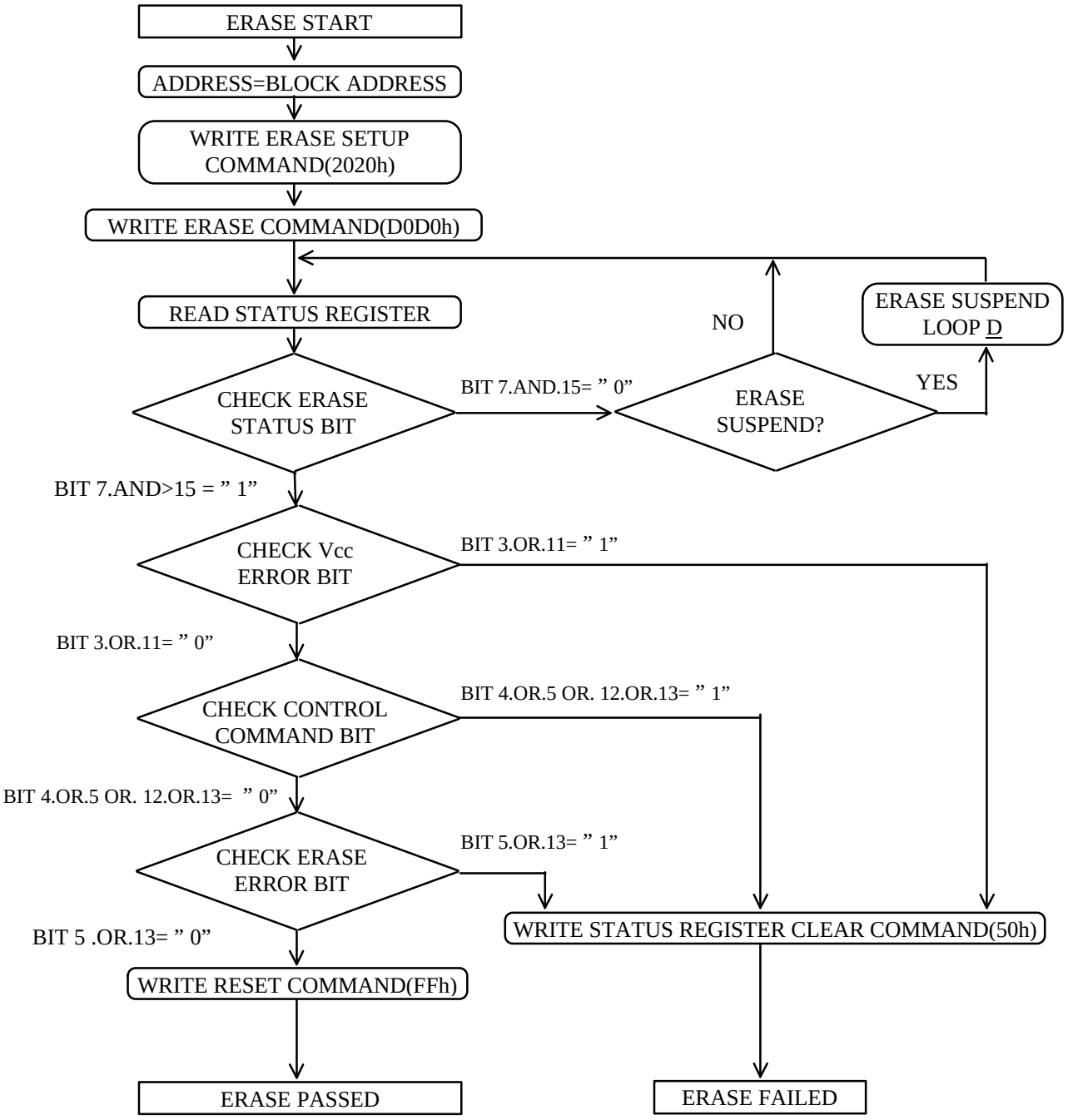
Note 7: If Vcc error bit is detected, try to programme again at Vcc level.
This is a programme algorithm for a memory zone and not for a card.
Reading data from the zone generating programme suspend.
.OR. : =Logical or ; .AND. : =Logical and

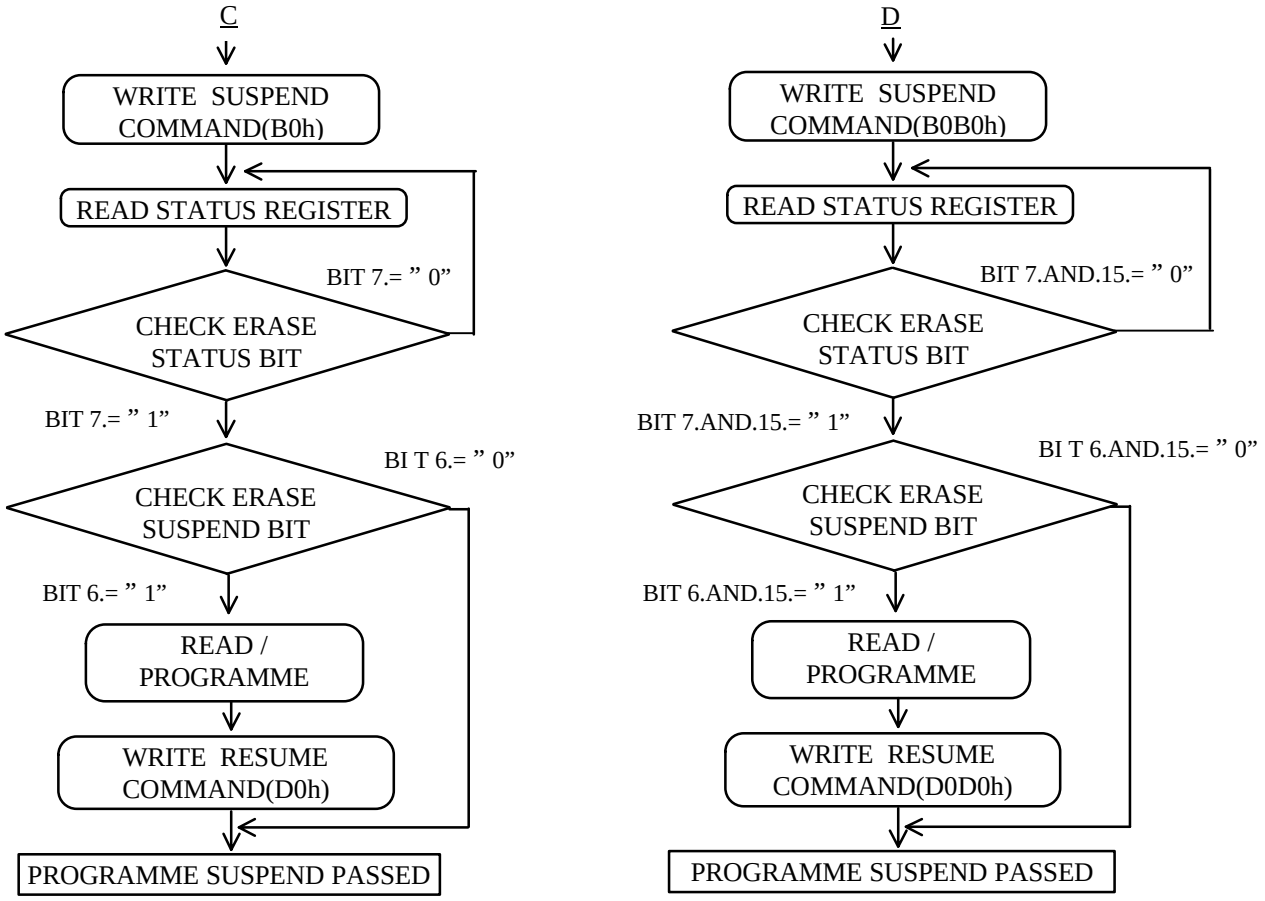
ERASE ALGORITHM
8 bit mode



ERASE ALGORITHM

16 bit mode





Note 8 : If Vcc error bit is detected, try to programme again at Vcc level.
This is an erase algorithm for a memory block and not for a card.
Reading data from blocks other than the suspended block in the zone generating erase suspend.
.OR. : =Logical or ; .AND. : =Logical and

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	V_{CC} Supply voltage	With respect to GND	-0.5 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{opr}	Operating temperature	Read/Write Operation	0 to 70	°C
T_{stg}	Storage temperature		-40 to 80	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 to 55°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	V_{CC} Supply voltage		4.75	5.0	5.25	V
V_{IH}	High input voltage		2.4		V_{CC}	V
V_{IL}	Low input voltage		0		0.8	V
N_{ACT}	Number of simultaneous activated memory zones/blocks	Programme			1	Zone
		Erase			1	Block

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			
			Min.	Typ.	Max.	
C_i	Input capacitance	V_I=GND, v_i=25mVrms, f=1 MHz, Ta=25°C			45	pF
C_o	Output capacitance	V_I=GND, v_o=25mVrms, f=1 MHz, Ta=25°C			45	pF

Note 9 : These parameters are not 100% tested.

ELECTRICAL CHARACTERISTICS

Ta= 0 to 55°C, VCC=5V+/-5%, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output current	I_{OH}=-0.1mA, BVDn		2.4			V
		I_{OH}=-1.0mA, Other outputs		2.4			
V_{OL}	Low output voltage	I_{OL}=2mA		0		0.4	V
I_{IH}	High input current	V_I=V_{CC} V				10	µA
I_{IL}	Low output voltage	V_I=0V	CE1#, CE2#, OE#, WE#, REG#	-10		-70	µA
			Other inputs			-10	
I_{OZH}	High output current in off state	CE1#=CE2#=V_{IH} or OE#=V_{IH},V_O(Dm)=V_{CC}				10	µA
I_{OZL}	Low output current in off state	CE1#=CE2#=V_{IH} or OE#=V_{IH}, V_O(Dm)=0V				-10	µA
I_{CC} 1・1	Active V_{CC} supply current 1	CE1#=CE2#=V_{IL}, Other inputs=V_{IH} or V_{IL}, Outputs=open			130	200	mA
I_{CC} 1・2	Active V_{CC} supply current 2	CE1#=CE2# ≤ 0.2V, Other inputs ≤ 0.2V or ≥ V_{CC}-0.2V, Outputs=open			110	180	mA
I_{CC} 2・1	Standby V_{CC} supply current 1	CE1#=CE2#=V_{IH}, Other inputs=V_{IH} or V_{IL}	2MB			6.0	mA
			4MB			6.0	
			8MB			10	
			16MB			18	
			20MB			22	
			32MB			34	
I_{CC} 2・2	Standby V_{CC} supply current 2	CE1#=CE2# ≥ V_{CC}-0.2V, Other inputs ≤ 0.2V or ≥ V_{CC}-0.2V	2MB		0.05	1.2	µA
			4MB		0.05	1.4	
			8MB		0.10	1.8	
			16MB		0.20	1.8	
			20MB		0.25	2.0	
			32MB		0.40	2.6	

Note 10 : Currents flowing into the card are taken as positive (unsigned).
Typical values are measured at V_{CC}=5.0V,Ta=25°C.
The card consumes active current at programming, erasure even if both CE1# and CE2# are high level.

SWITCHING CHARACTERISTICS (COMMON MEMORY) (Ta= 0 to 55°C, Vcc=5V+/-5%)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tcR	Read cycle time	150			ns
ta(A)	Address access time			150	ns
ta(CE)	Card enable access time			150	ns
ta(OE)	Output enable access time			75	ns
tdis(CE)	Output disable time (from CE#)			75	ns
tdis(OE)	Output disable time (from OE#)			75	ns
ten(CE)	Output enable time (from CE#)	5			ns
ten(OE)	Output enable time (from OE#)	5			ns
tv(A)	Data valid time after address change	0			ns

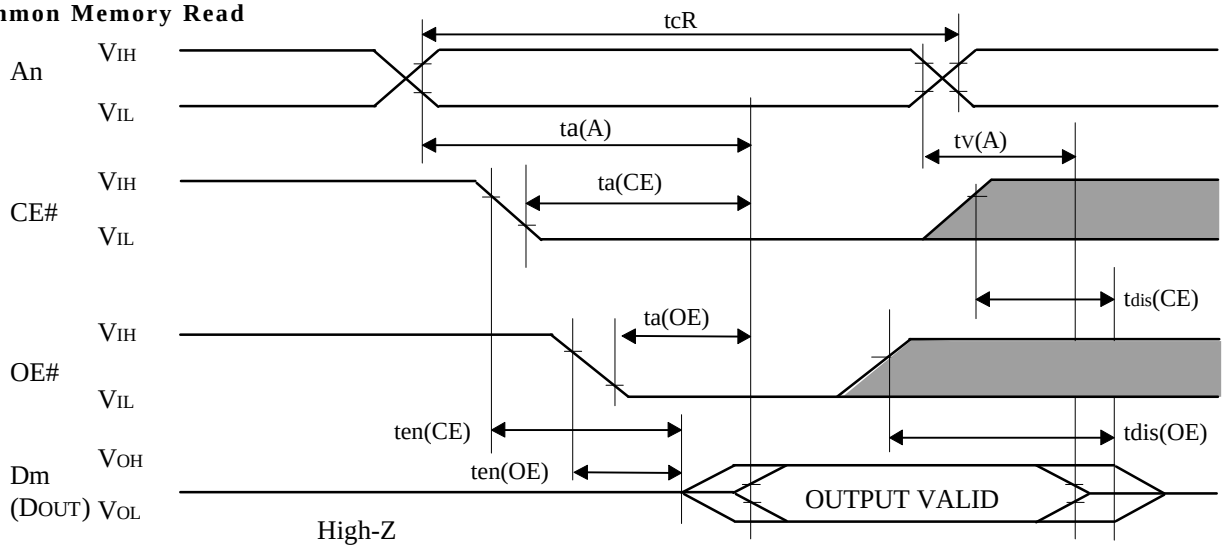
TIMING REQUIREMENTS (COMMON MEMORY) (Ta= 0 to 55°C, Vcc=5V+/-5%)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tcW	Write cycle time	150			ns
tSU(A)	Address setup time	20			ns
trec(WE)	Write recovery time	20			ns
tsu(D-WEH)	Data setup time	50			ns
th(D)	Data hold time	20			ns
tWRR	Write recovery time before read	0			ns
tsu(A-WEH)	Address setup time to write enable high	100			ns
tsu(CE)	Card enable setup time	20			ns
th(CE)	Card enable hold time	20			ns
tw(WE)	Write pulse width	80			ns
tWPH	Write pulse width high	40			ns
tDP	Duration of programming operation	6.5			µs
tDE	Duration of erase operation	900			ms

Note 11 : Refer to switching characteristics for read parameters

TIMING DIAGRAM

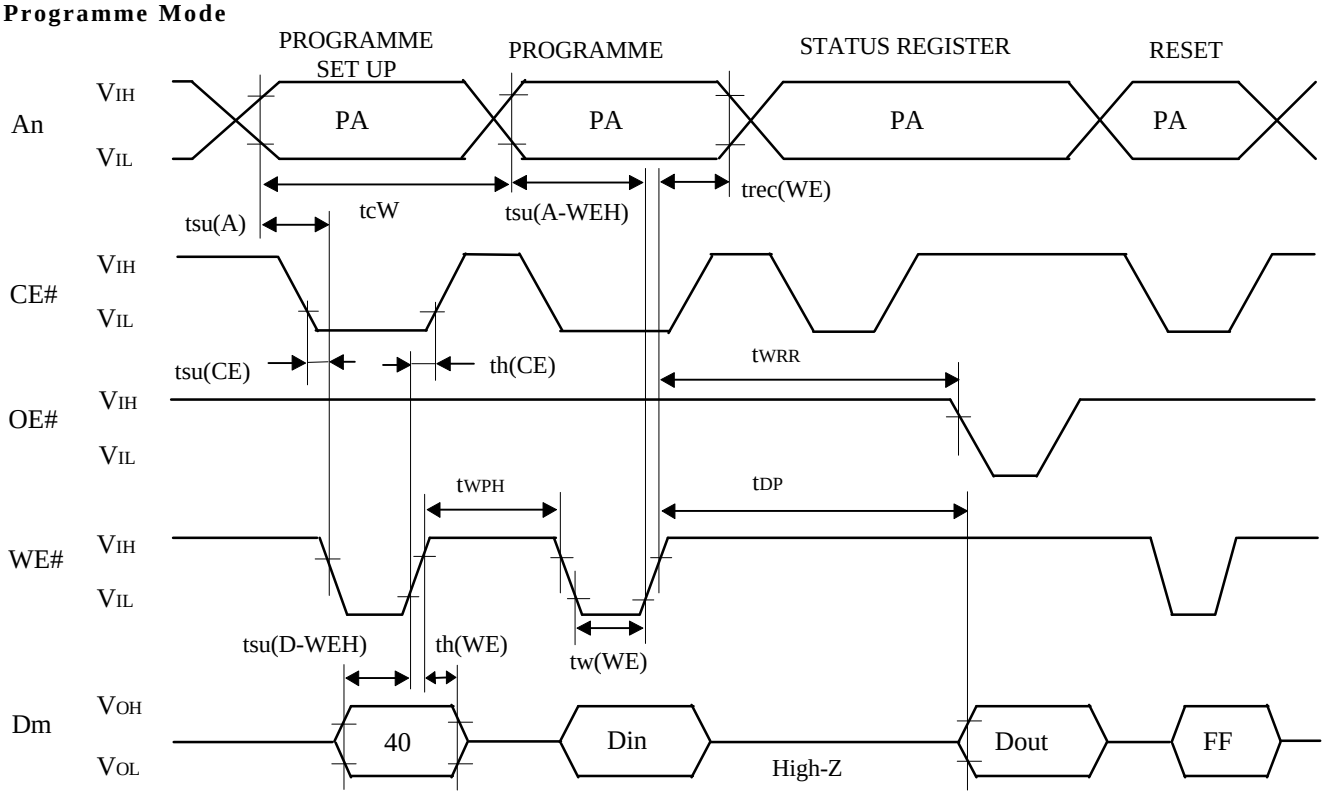
Common Memory Read



WE# ="H" level, REG# ="H" level

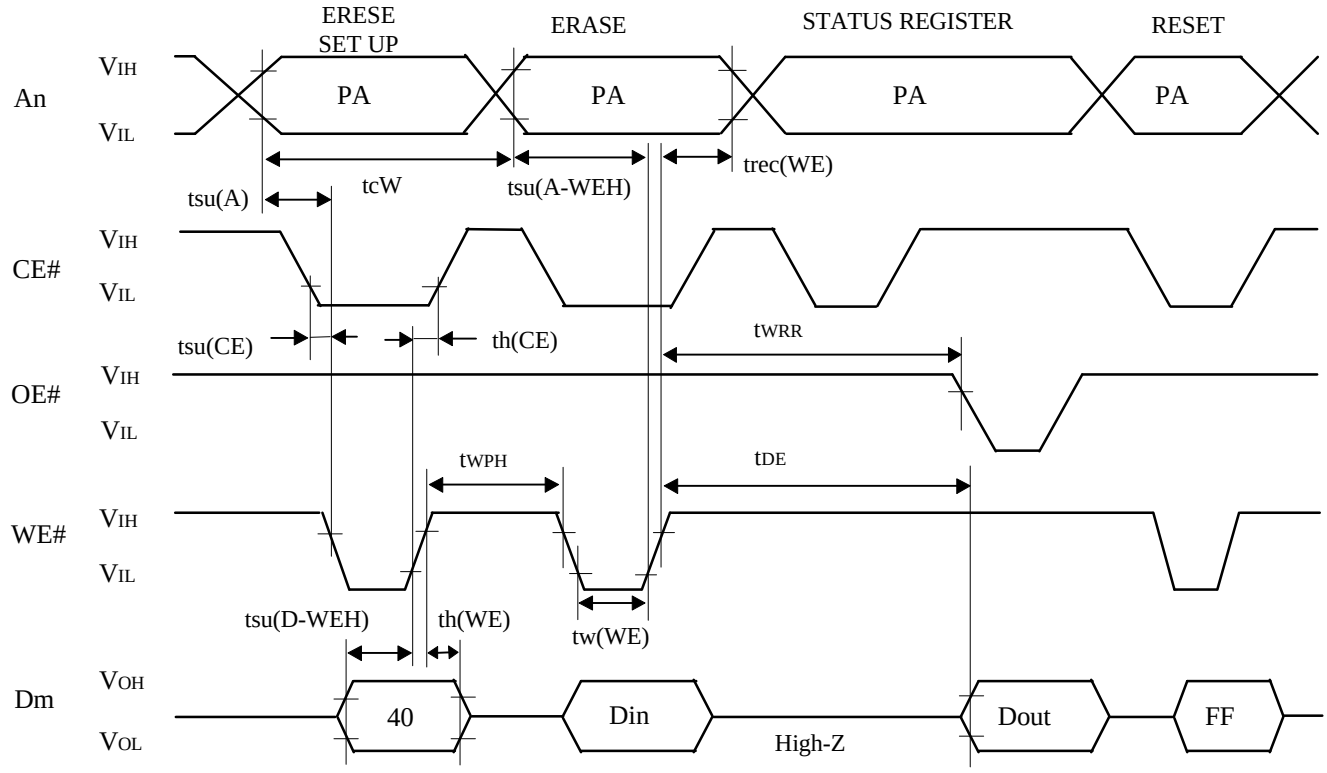
TIMING DIAGRAM (COMMON MEMORY)

Programme Mode



REG# ="H" level

Erase Mode



REG# ="H" level

SWITCHING CHARACTERISTICS (ATTRIBUTE MEMORY)

Read Cycle (Ta= 0 to 55°C, V_{CC}=5V+/-5%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tcRR	Read cycle time	300			ns
ta(A)R	Address access time			300	ns
ta(CE)R	Card enable access time			300	ns
ta(OE)R	Output enable access time			150	ns
tdis(dis)R	Output disable time (from CE#)			100	ns
tdis(OE)R	Output disable time (from OE#)			100	ns
ten(CE)R	Output enable time (from CE#)	5			ns
ten(CE)R	Output enable time (from OE#)	5			ns
tv(A)R	Data valid time after address change	0			ns

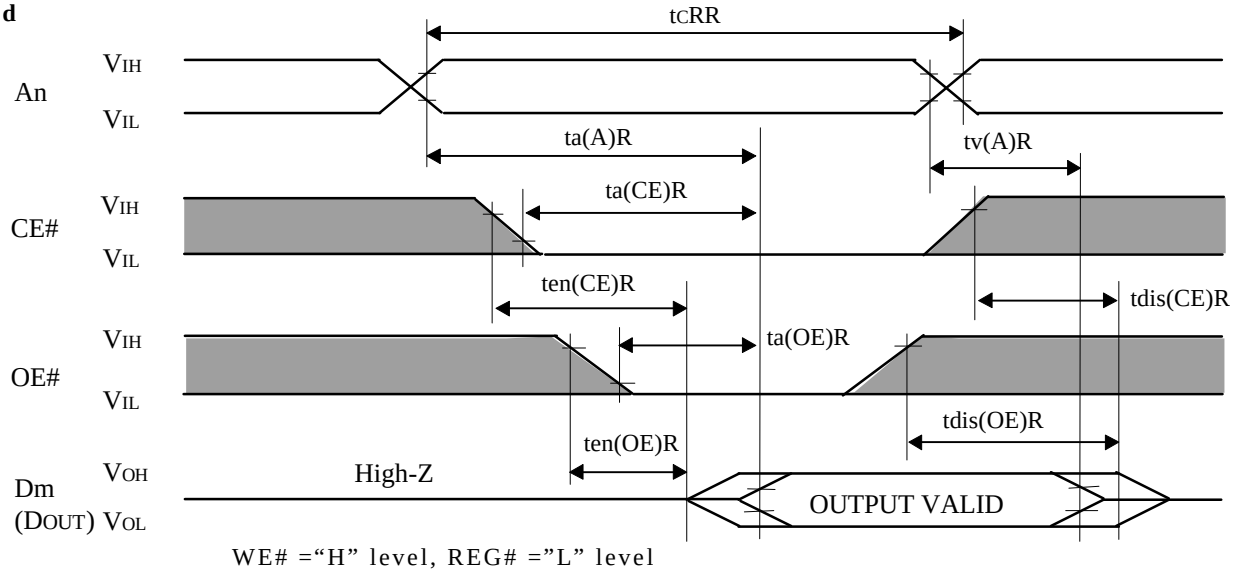
TIMING REQUIREMENTS (ATTRIBUTE MEMORY)

Write Cycle GM series only (Ta= 0 to 55°C, V_{CC}=5V+/-5%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}R	Address setup time	30			ns
t_{AH}R	Address hold time	30			ns
t_{CS}R	CE setup time	40			ns
t_{CH}R	CE hold time	30			ns
t_{DS}R	Data setup time	120			ns
t_{DH}R	Data hold time	40			ns
t_{OES}R	OE setup time	30			ns
t_{OEH}R	OE hold time	40			ns
t_{WP}R	Write pulse width	170			ns
t_{DL}R	Data latch time	120			ns
t_{BL}R	Byte load cycle time	100			µs
t_{WC}R	Write cycle time	10			ms

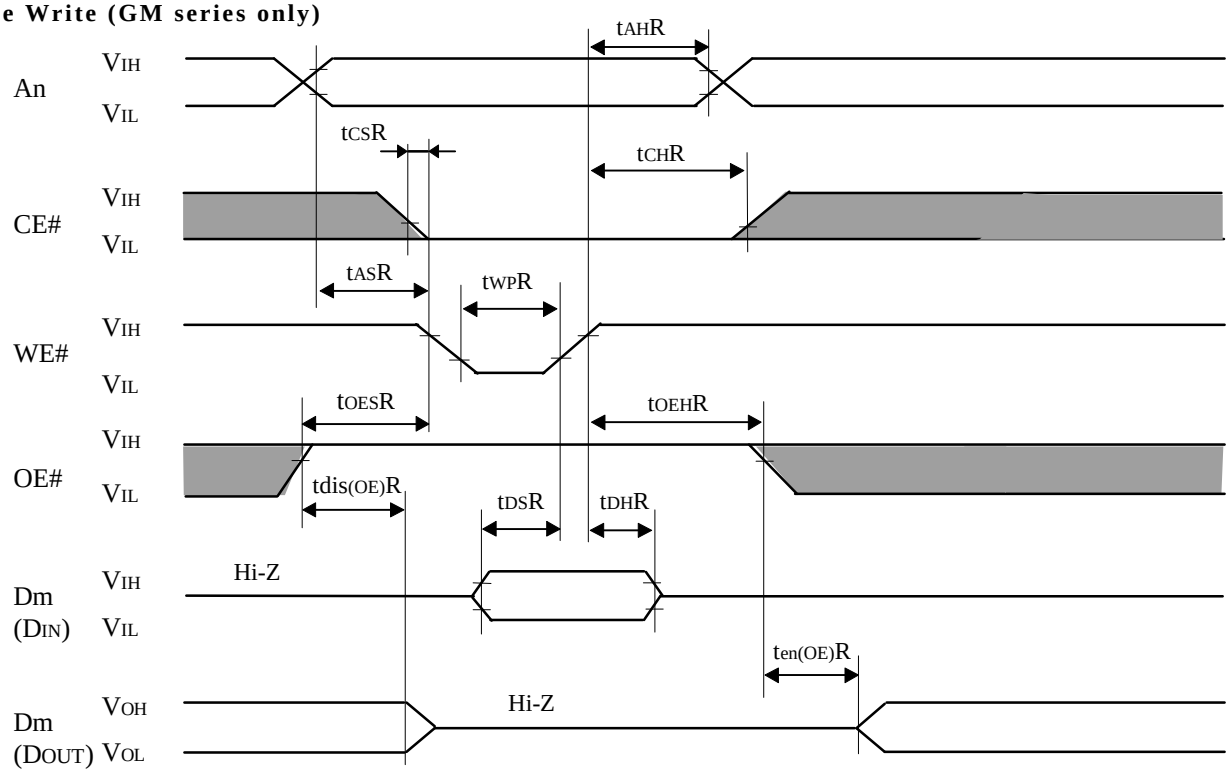
TIMING DIAGRAM (Attribute Memory)

Read



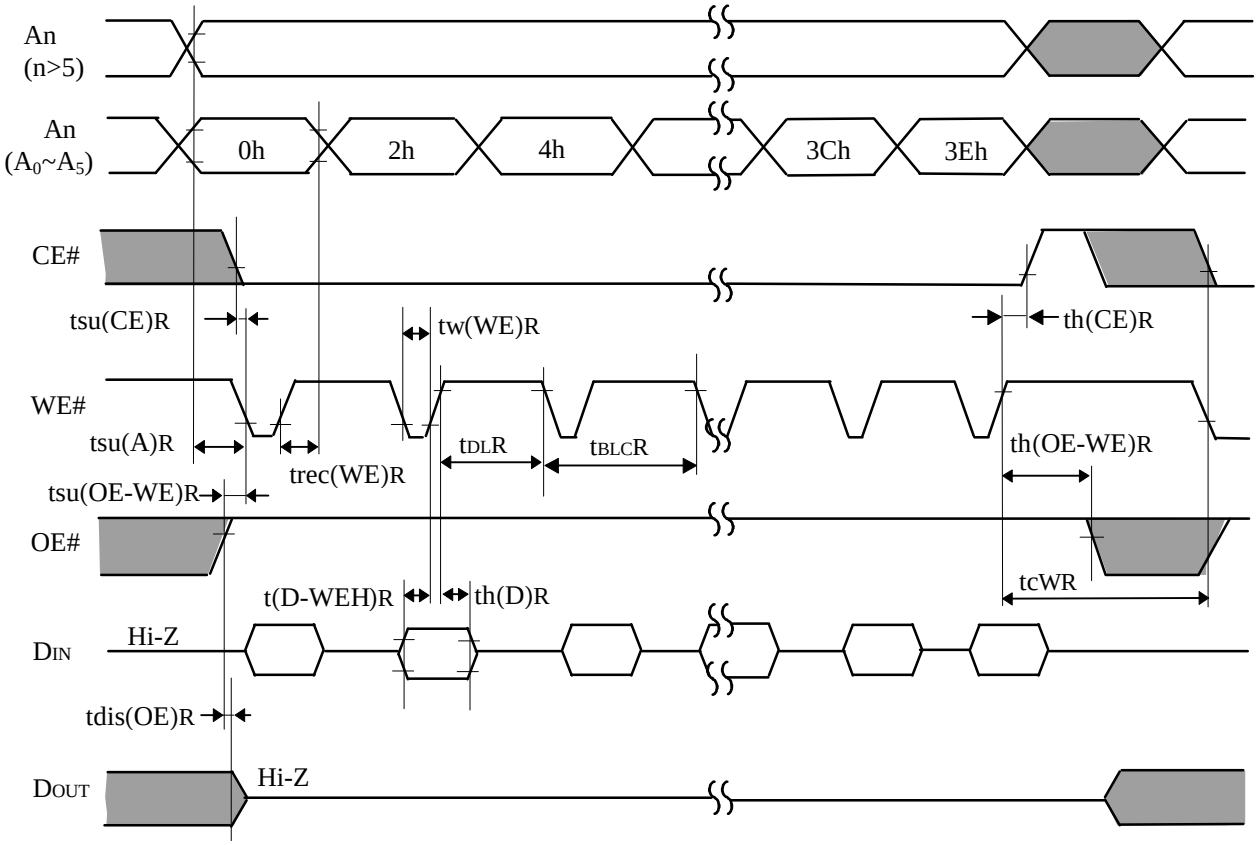
WE# ="H" level, REG# ="L" level

Byte Write (GM series only)



REG# ="L" level

PAGE MODE WRITE (GM series only)



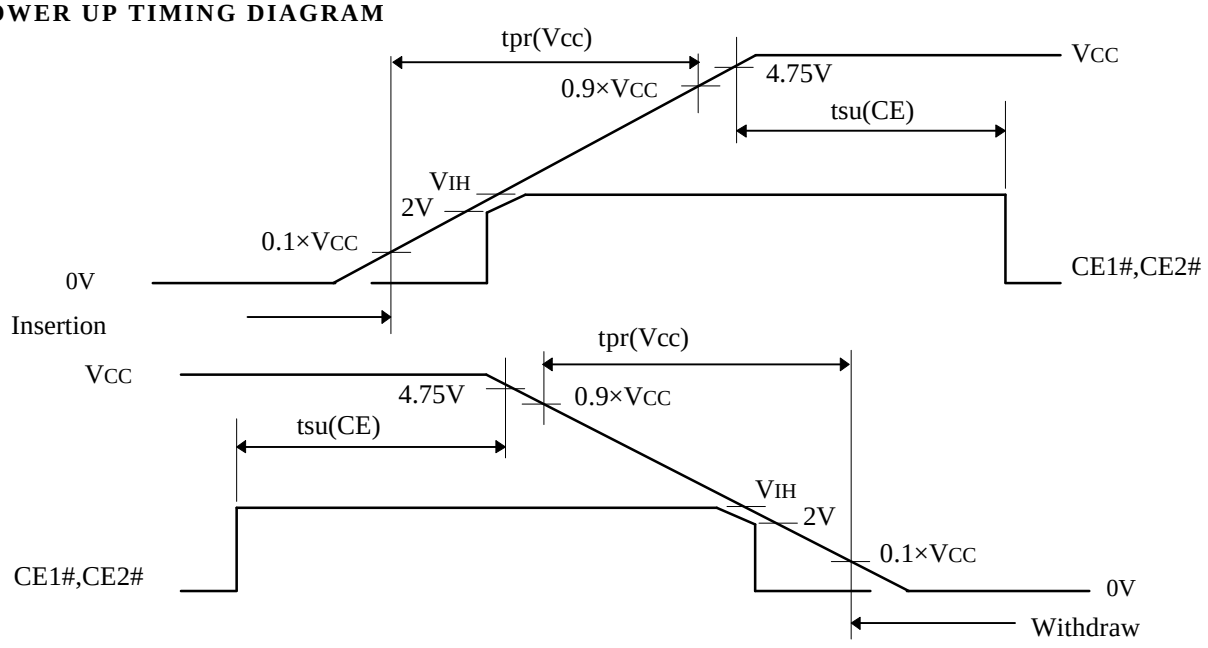
REG# ="L" level

Note 12 : AC Test Conditions
Input pulse levels : V_{IL}=0.4V, V_{IH}=2.8V
Input pulse rise, fall time : t_r=t_f=10ns
Reference voltage
Input : V_{IL}=0.8V, V_{IH}=2.4V
Output : V_{OL}=0.8V, V_{OH}=2.0V
(ten and t_{dis} are measured when output voltage is ± 500mV from steady state.)
Load : 100pF+ 1 TTL gate
5pF+ 1 TTL gate (at ten and t_{dis} measuring)
13 : The data write is performed during the interval when both CE# and WE# are "L" level.
14 : Do not apply inverted phase signal externally when Dm pin is in output mode.
15 : CE# is indicated as follows:
Read A/Write A : CE#=CE1#=CE2#
Read B/Write B : CE#=CE1#, CE2#="H" level
Read C/Write C : CE#=CE2#, CE1#="H" level
16: Indicates the don't care input.

RECOMMENDED POWER UP/DOWN CONDITIONS (Ta=0 to 55°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
Vi(CE)	CE input voltage	0V≤ V_{CC} <2V	0	V_I	V
		2V≤ V_{CC} < V_{IH}	V_{CC}-0.1	V_I	V
		V_{IH}≤ V_{CC}	V_{IH}	V_I	V
t_{su}(CE)	CE# setup time		5.0		ms
t_{rec}(CE)	CE# recovery time		1.0		µs
t_{pr}(VCC)	V_{CC} rise time		0.1	300	ms
t_{pf}(VCC)	V_{CC} fall time		3.0	300	ms

POWER UP TIMING DIAGRAM



BLOCK PROGRAM/ERASE TIME

Parameters	Limits		Unit
	Typ.	Max.	
Block erase time	1.1	10	s
Block program time	0.5	2.1	s

Note 17 : At Ta=25°C, Vcc=5V
Byte/word program time is about 8µs (typical), but not guaranteed.

⚠ Warning (if card with battery / card with auxiliary battery)

(1)Do not charge, short, disassemble, deform, heat, or throw the batteries into fire, as they may ignite, overheat, rupture or explode.
(2)Place the batteries out of the reach of children. If somebody swallows them, they should see a doctor immediately.
(3)When discarding or storing the batteries, wrap them individually with cellophane tape or other nonconductive material. If they are positioned in contact with any other metals or batteries, they may explode, rupture or leak electrolyte solution.

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