

64MX16 3.3V NAND Flash Memory Module

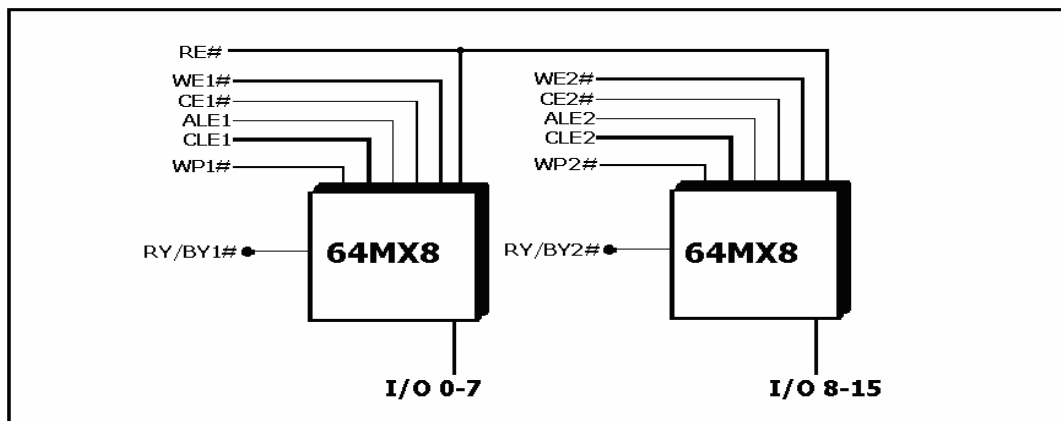
Features

- ❑ 3.3V±10% Supply/ Programming
- ❑ Access Time: 50ns (Page Read)
- ❑ Fast Page Write Cycle Time (200uSec)
- ❑ Package type:
 - 66-Pin Ceramic PGA 1.385" SQ
 - 66-Pin Ceramic PGA 1.080" SQ
- ❑ 60mA typical erase/program current
- ❑ 60mA active read current
- ❑ Embedded Program/Erase Algorithms
- ❑ Industrial & Military Screening
- ❑ 100,000 Erase/Program Cycles

Product Description

The MEF64M16ND is a 1024Megabit 3.3V NAND flash memory MCM, assembled in multilayered cofired ceramic package, designed for low noise and better ground bounce. Flowcharts of programming, byte write, block erase and other specifications are identical to "K9K1G08U0A" specifications and should be used as a reference.

Block Diagram



Pin Names

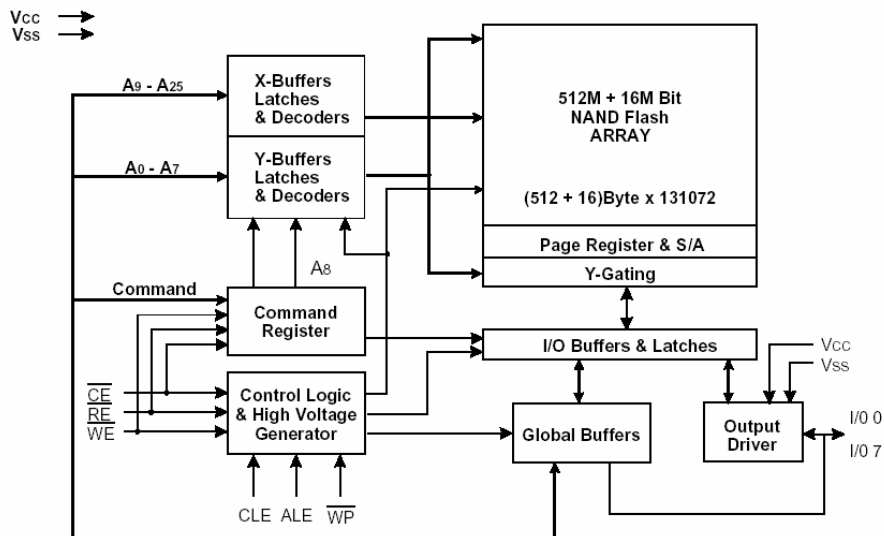
Pin Name	Pin Function
I/O0 ÷ I/O15	Address & Command Inputs & Data Inputs/Outputs
CLE1, CLE2	Command Latch Enables
ALE1, ALE2	Address Latch Enables
CE1#, CE2#	Chip Enables
WE1#, WE2#	Write Enables
RE# (or OE#)	Read Enable (or Output Enable)
WP1#, WP2#	Hardware write protect inputs
RY/BY1#, RY/BY2#	Ready/busy outputs
GND (or Vss)	Ground
Vcc	Power Supply (+3.3V \pm 10%)

Note: # Symbol means "Active Low" Signal

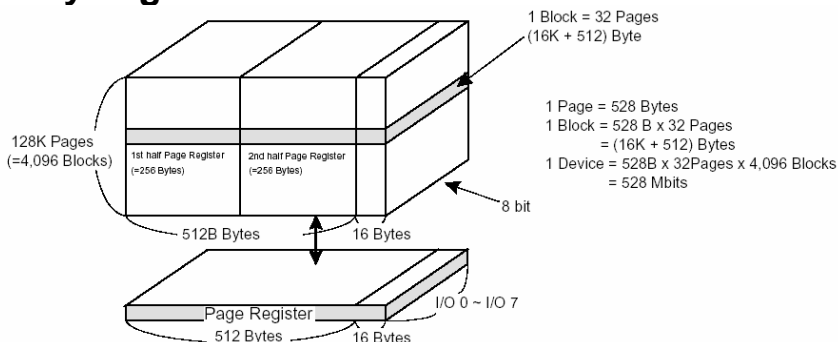
Pin Configuration for 66-Pin PGA (Top View)

	A	B	C	F	G	H
1	● I/O8	● WE2#	● I/O15	NC ●	VCC ●	GND ●
2	● I/O9	● CE2#	● I/O14	NC ●	NC ●	NC ●
3	● I/O10	● GND	● I/O13	NC ●	WP1# ●	VCC ●
4	● NC	● I/O11	● I/O12	NC ●	NC ●	NC ●
5	● CLE1	● RY/BY1#	● RE#	RY/BY2# ●	ALE2 ●	NC ●
6	● NC	● NC	● NC	NC ●	NC ●	NC ●
7	● CLE2	● NC	● WE1#	NC ●	NC ●	NC ●
8	● NC	● VCC	● I/O7	ALE1 ●	NC ●	WP2# ●
9	● I/O0	● CE1#	● I/O6	NC ●	NC ●	NC ●
10	● I/O1	● NC	● I/O5	NC ●	GND ●	NC ●
11	● I/O2	● I/O3	● I/O4	GND ●	NC ●	GND ●

Functional Block Diagram (8 Bit Mode)



Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	Column Address
2nd Cycle	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄	A ₁₅	A ₁₆	Row Address (Page Address)
3rd Cycle	A ₁₇	A ₁₈	A ₁₉	A ₂₀	A ₂₁	A ₂₂	A ₂₃	A ₂₄	
4th Cycle	A ₂₅	*L	*L	*L	*L	*L	*L	*L	

NOTE: Column Address: Starting Address of the Register.

00h Command (Read): Defines the starting address of the 1st half of the register.

01h Command (Read): Defines the starting address of the 2nd half of the register.

*A8 is set to "Low" or "High" by the 00h or 01h Command. (*L must be set to "Low")

Command Definitions

Function	1st. Cycle	2nd. Cycle	3rd. Cycle	Acceptable Command during Busy
Read 1	00h/01h ⁽¹⁾	-	-	
Read 2	50h	-	-	
Read ID	90h	-	-	
Reset	FFh	-	-	○
Page Program (True) ⁽²⁾	80h	10h	-	
Page Program (Dummy) ⁽²⁾	80h	11h	-	
Copy-Back Program(True) ⁽²⁾	00h	8Ah	10h	
Copy-Back Program(Dummy) ⁽²⁾	00h	8Ah	10h	
Block Erase	60h	D0h	-	
Multi-Plane Block Erase	60h--60h	D0h	-	
Read Status	70h	-	-	○
Read Multi-Plane Status	71h ⁽³⁾	-	-	○

NOTE:

1. The 00h command defines starting address of the 1st half of registers.

The 01h command defines starting address of the 2nd half of registers.

After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register (00h) on the next cycle.

2. Page Program (True) and Copy-Back Program (True) are available on 1 plane operation.

Page Program (Dummy) and Copy-Back Program (Dummy) are available on the 2nd, 3rd, 4th plane of multi plane operation.

3. The 71h command should be used for read status of Multi Plane operation.

Caution: Any undefined command inputs are prohibited except for above command set.

Absolute Maximum Ratings

Item	Rating
Supply Voltage Relative to GND	-0.5V to +4.6V
Voltage on Any Pin Relative to GND	-0.5V to Vcc +0.5V
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

NOTE:

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(Voltage reference to GND, MEF64M16: TA=0 to 70°C, MEF64M16: TA=-55 to +125°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V _{CC}	2.7	3.3	3.6	V
Supply Voltage	V _{SS}	0	0	0	V

Dc and Operating Characteristics (8 Bit Mode)

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	I _{CC1}	t _{RC} =50ns, CE=V _{IL} , I _{OUT} =0mA	-	10	30	mA
	Program	I _{CC2}	-	-	10	30	
	Erase	I _{CC3}	-	-	10	30	
Stand-by Current(TTL)		I _{SB1}	CE=V _{IH} , WP= 0V/V _{CC}	-	-	1	μA
Stand-by Current(CMOS)		I _{SB2}	CE=V _{CC} -0.2, WP = 0V/V _{CC}	-	10	50	
Input Leakage Current		I _{LI}	V _{IN} =0 to 3.6V	-	-	±10	
Output Leakage Current		I _{LO}	V _{OUT} =0 to 3.6V	-	-	±10	V
Input High Voltage		V _{IH}	-	2.0	-	V _{CC} +0.3	
Input Low Voltage, All inputs		V _{IL}	-	-0.3	-	0.8	
Output High Voltage Level		V _{OH}	I _{OH} =-400μA	2.4	-	-	mA
Output Low Voltage Level		V _{OL}	I _{OL} =2.1mA	-	-	0.4	
Output Low Current(R/B)		I _{OL} (R/B)	V _{OL} =0.4V	8	10	-	

AC Test Condition (8 Bit Mode)

(MEF64M16: TA=0 to 70°C, MEF64M16: TA=-55 to +125°C, V_{CC}=2.7V~3.6V unless otherwise)







Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (3.0V +/-10%)	1 TTL GATE and CL=50pF
Output Load (3.3V +/-10%)	1 TTL GATE and CL=100pF

Capacitance (TA=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{IL} =0V	-	10	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

Mode Selection

CLE	ALE	CE	WE	RE	WP	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(4clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input(4clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Sequential Read & Data Output	
L	L	L	H	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X ⁽¹⁾	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V _{CC} ⁽²⁾	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.

2. WP should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Sym-	Min	Typ	Max	Unit
Program Time		t _{PROG}	-	300	700	μs
Dummy Busy Time for Cache Program		t _{CBSY}		3	700	μs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	4	cycles
	Spare Array		-	-	4	cycles
Block Erase Time		t _{BERS}	-	2	3	ms

NOTE: Max time of t_{CBSY} depends on timing between internal program completion and data in

AC Timing Characteristics for Command/Address/Data Input

Parameter	Symbol	Min	Max	Unit
CLE setup Time	tCLS	0	-	ns
CLE Hold Time	tCLH	10	-	ns
CE setup Time	tCS	0	-	ns
CE Hold Time	tCH	10	-	ns
WE Pulse Width	tWP	25 ⁽¹⁾	-	ns
ALE setup Time	tALS	0	-	ns
ALE Hold Time	tALH	10	-	ns
Data setup Time	tDS	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	50	-	ns
WE High Hold Time	tWH	15	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation (8 Bit Mode)

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	12	μs
ALE to RE Delay(ID read)	tAR1	10	-	ns
ALE to RE Delay(Read cycle)	tAR2	50	-	ns
CLE to RE Delay	tCLR	50	-	ns
Ready to RE Low	tRR	20	-	ns
RE Pulse Width	tRP	30	-	ns
WE High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	50	-	ns
RE Access Time	tREA	-	35	ns
RE High to Output Hi-Z	tRHZ	-	30	ns
CE High to Output Hi-Z	tCHZ	-	20	ns
RE or CE High to Output hold	tOH	15	-	ns
RE High Hold Time	tREH	15	-	ns
Output Hi-Z to RE Low	tIR	0	-	ns
Last RE High to Busy(at sequential read)	tRB	-	100	ns
CE High to Ready(in case of interception by CE at read)	tCRY	-	50 +tr(R/B) ⁽¹⁾	ns
CE High Hold Time(at the last serial read) ⁽²⁾	tCEH	100	-	ns
CE Access Time	tCEA	-	45	ns
WE High to RE Low	tWHR	60	-	ns
Device Resetting Time(Read/Program/Erase)	tRST	-	5/10/500 ⁽³⁾	μs

NOTE:

1. The time to Ready depends on the value of the pull-up resistor tied R/B pin.
2. To break the sequential read cycle, CE must be held high for longer time than tCEH.
3. If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

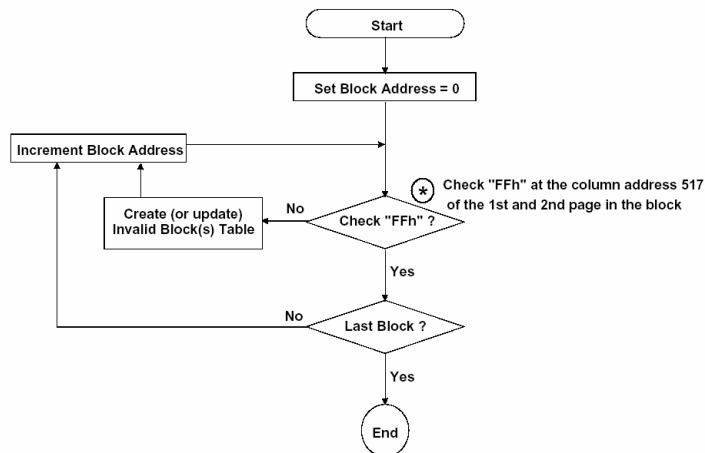
Identifying Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level or as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. **The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction.**

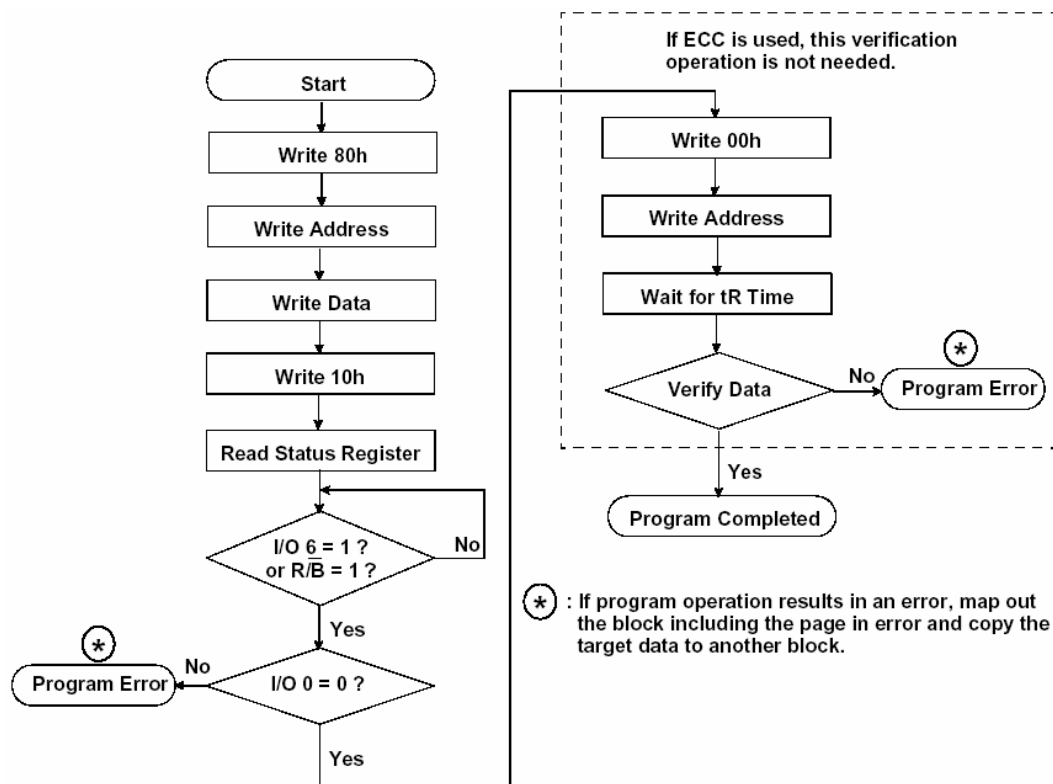
Invalid Block(s)

All device locations are erased (FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte in the spare area. Elisra makes sure that either the 1st or 2nd page of every invalid block has non-FFh data at the column address of 517. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart (Figure 4). Any intentional Erasure of the original invalid block information is prohibited.

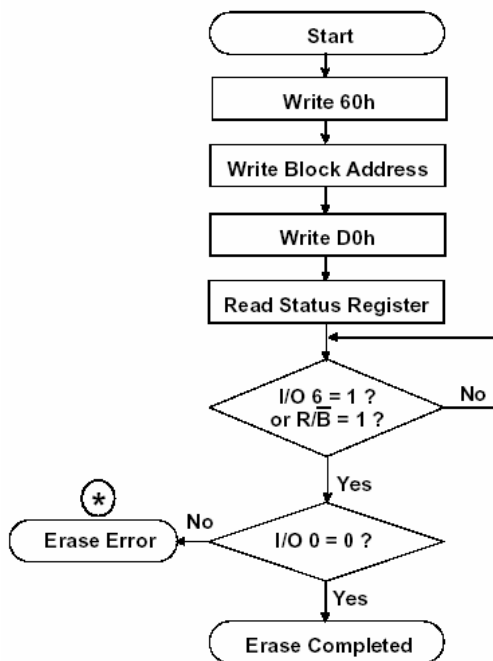
Flow Chart to Create Invalid Block



Program Flow Chart

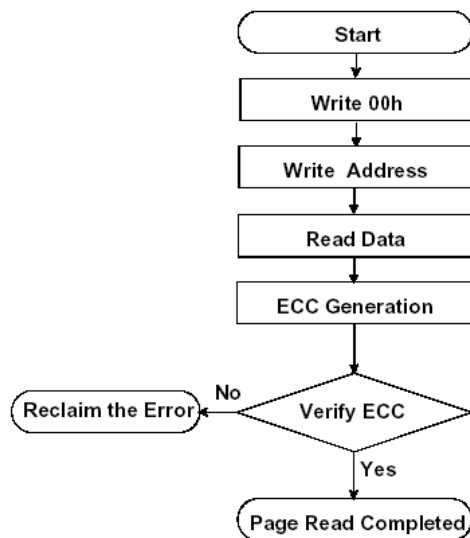


Erase Flow Chart

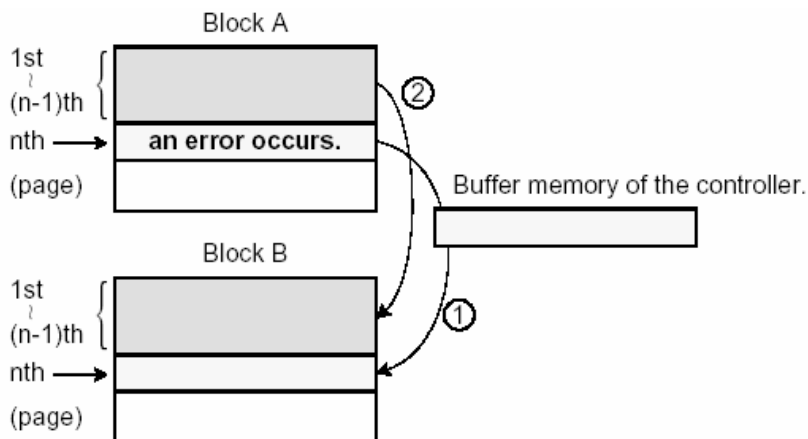


(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Read Flow Chart



Block Replacement



*** Step1**

When an error happens in the nth page of the Block 'A' during erase or program operation.

*** Step2**

Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')

*** Step3**

Then, copy the data in the 1st ~ (n-1)th page to the same location of the Block 'B'.

*** Step4**

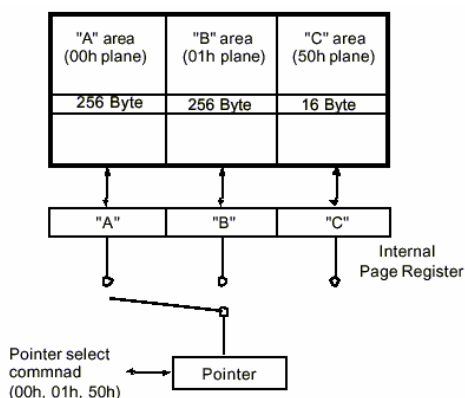
Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

Pointer Operation of MEF64M16ND

The NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area (0~255byte), '01h' command sets the pointer to 'B' area (256~511byte), and '50h' command sets the pointer to 'C' area (512~527byte). With these commands, the starting column address can be set to any of a whole page (0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

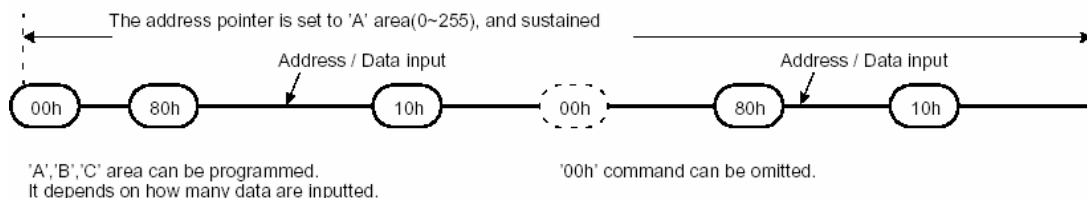
Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

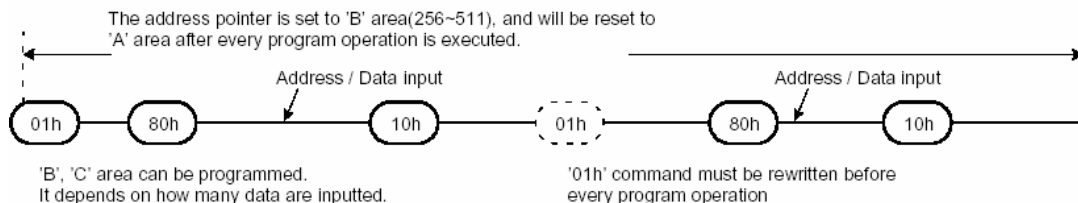


Block Diagram of Pointer Operation

(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



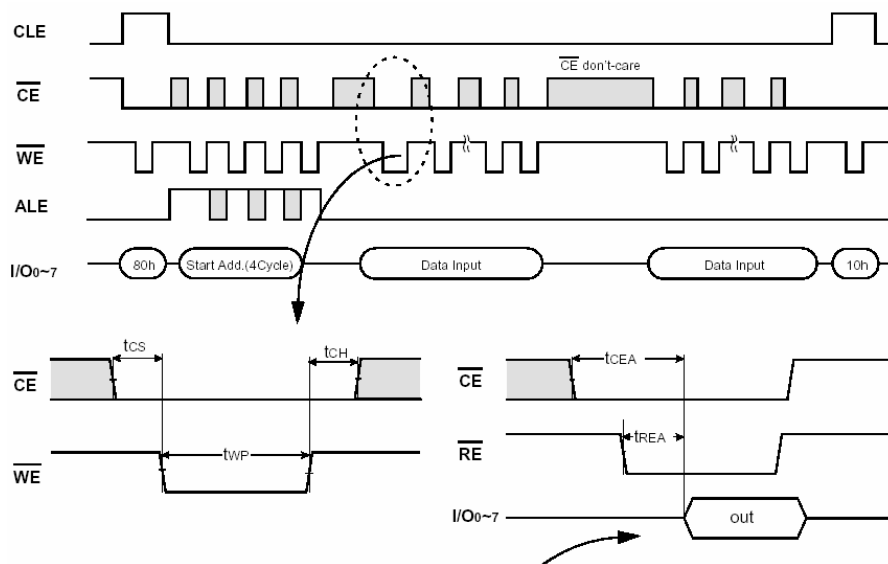
(3) Command input sequence for programming 'C' area



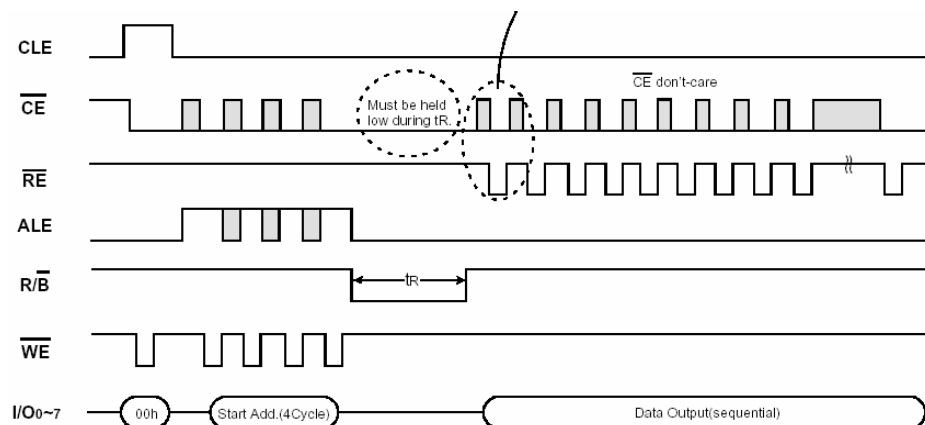
System Interface Using CE don't-care.

For an easier system interface, CE may be inactive during the data-loading or sequential data reading as shown below. The internal 2X528byte page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating CE during the data-loading and reading would provide significant savings in power consumption.

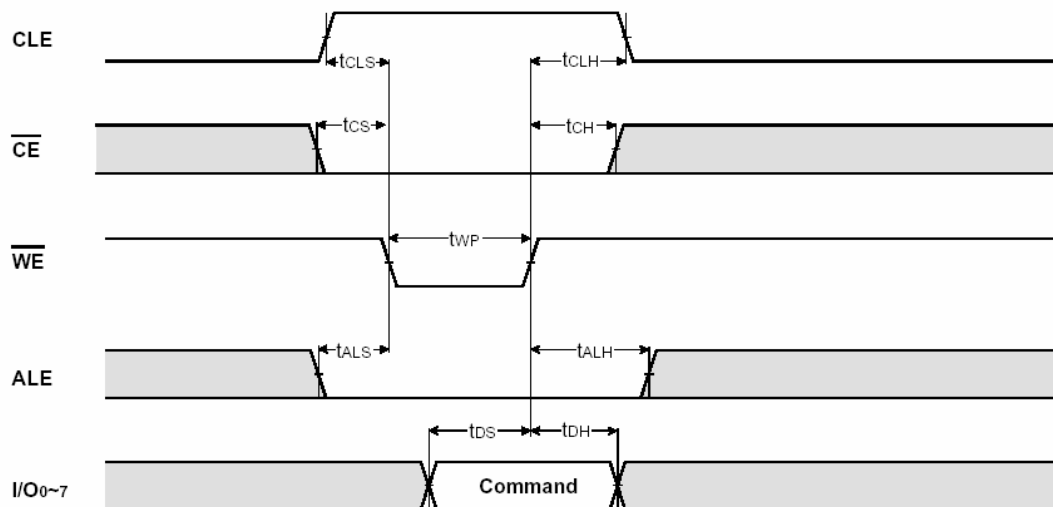
Program Operation with CE don't-care.



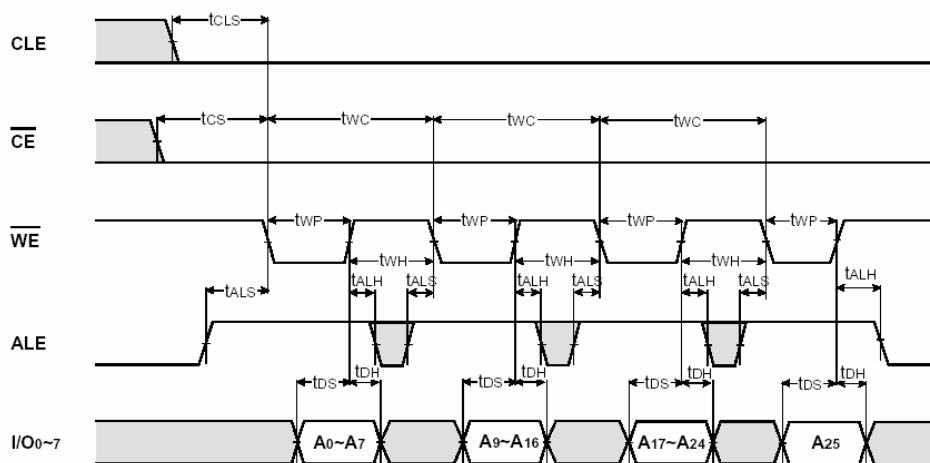
Read Operation with CE don't-care.



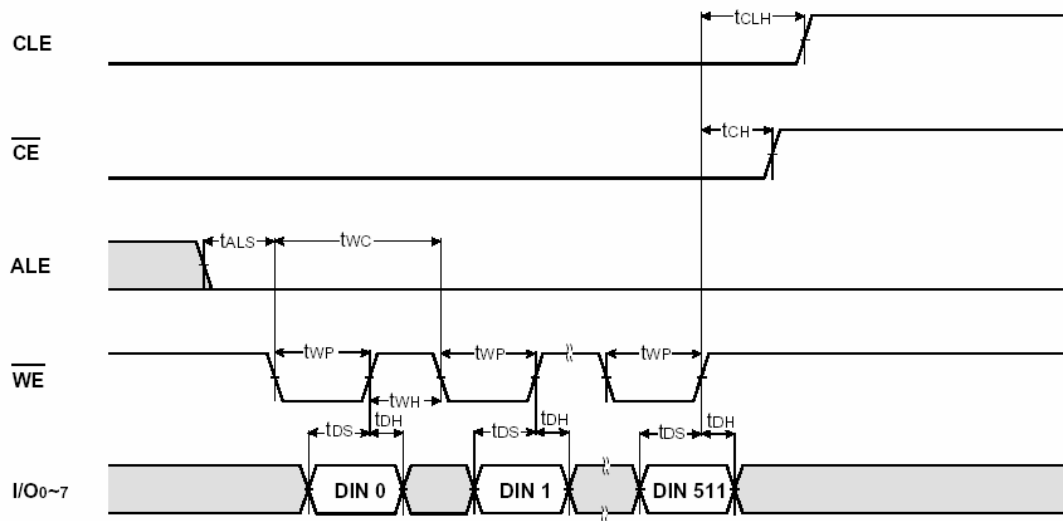
Command Latch Cycle



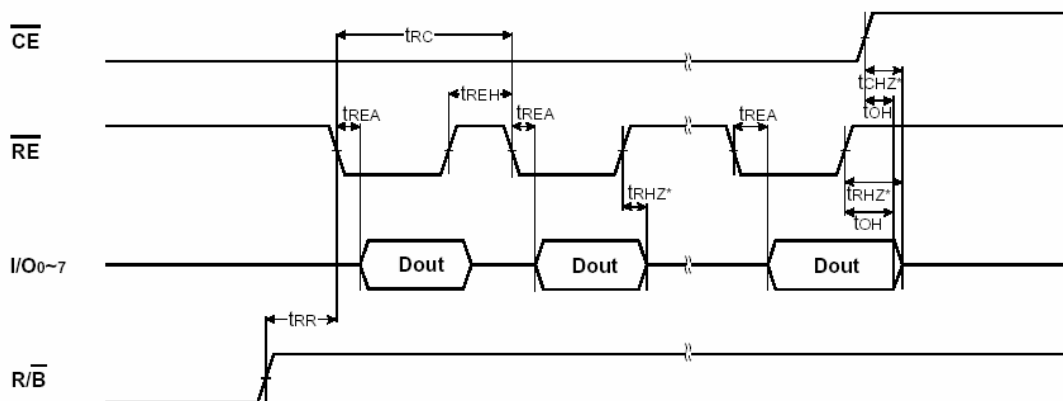
Address Latch Cycle



Input Data Latch Cycle

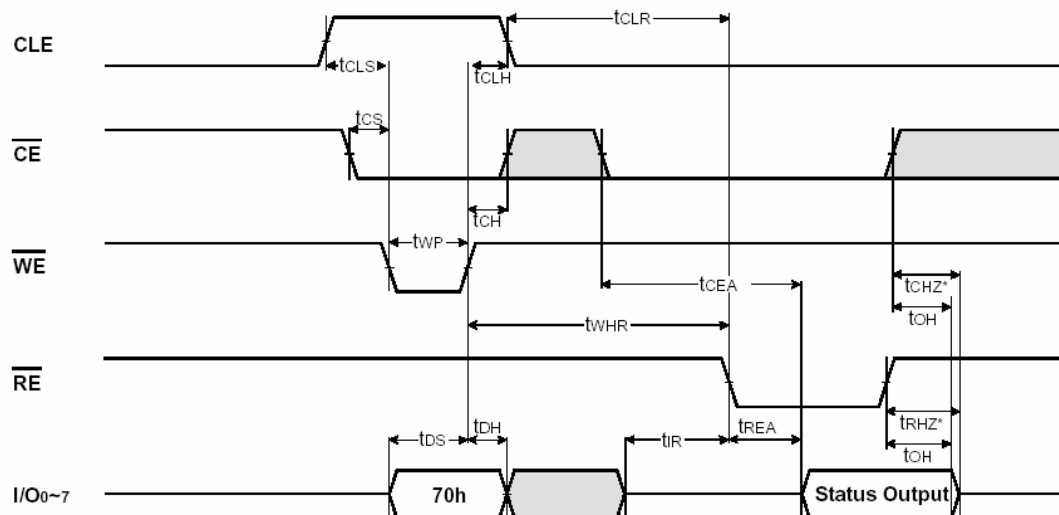


Serial access Out Cycle after Read (CLE=L, WE=H, ALE=L)

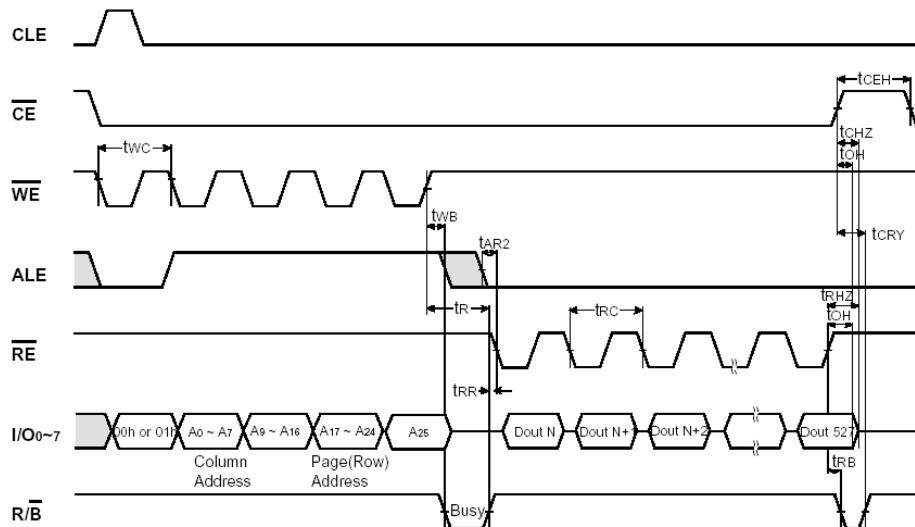


NOTES: Transition is measured $\pm 200\text{mV}$ from steady state voltage with load.
This parameter is sampled and not 100% tested.

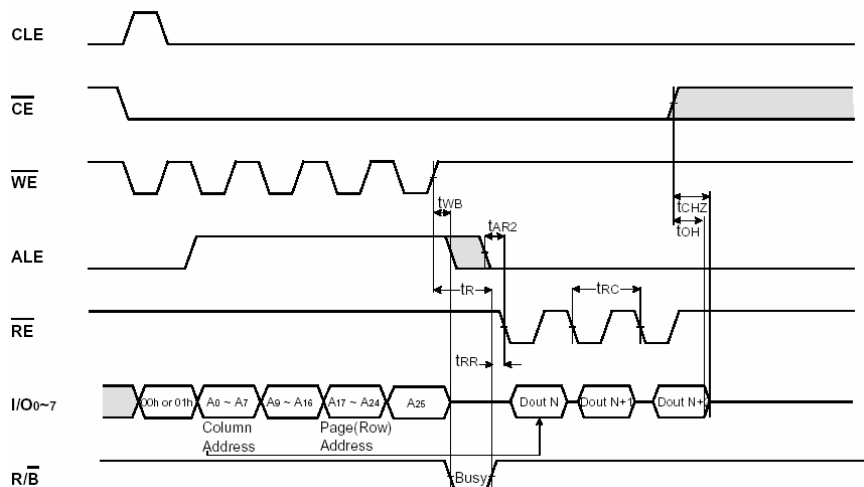
Status Read Cycle



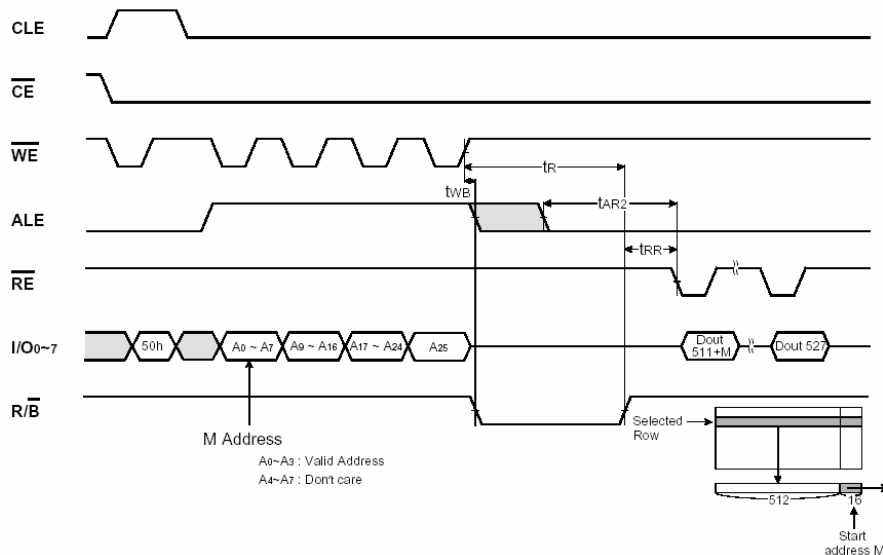
Read1 Operation (Read One Page)



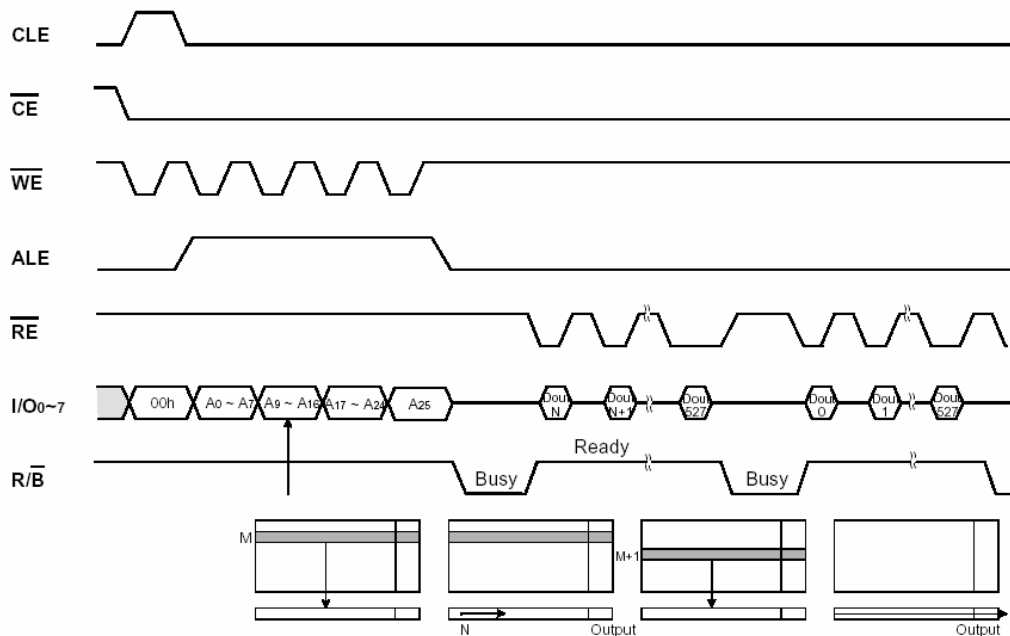
Read1 Operation (Intercepted by CE)



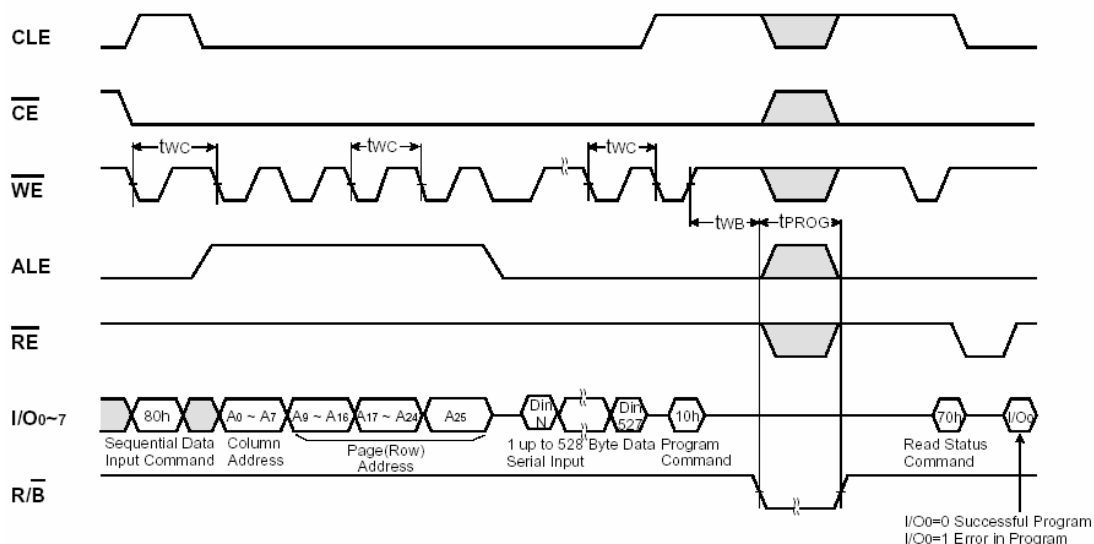
Read2 Operation (Read One Page)



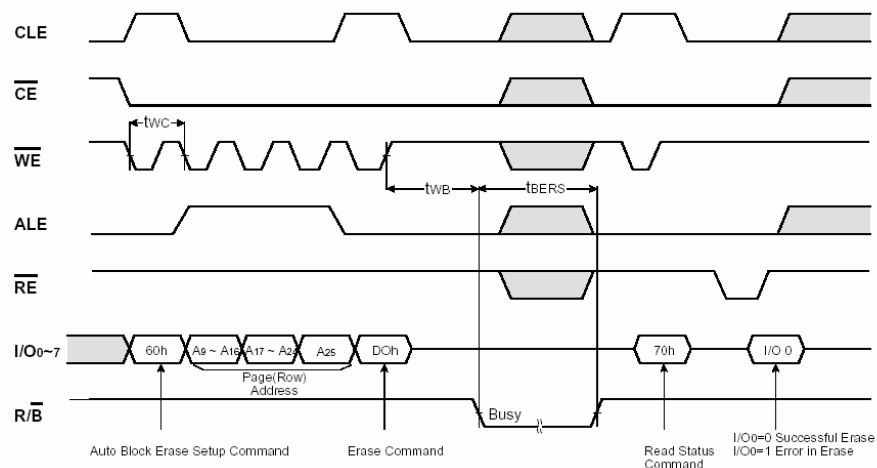
Sequential Row Read Operation (Within a Block)



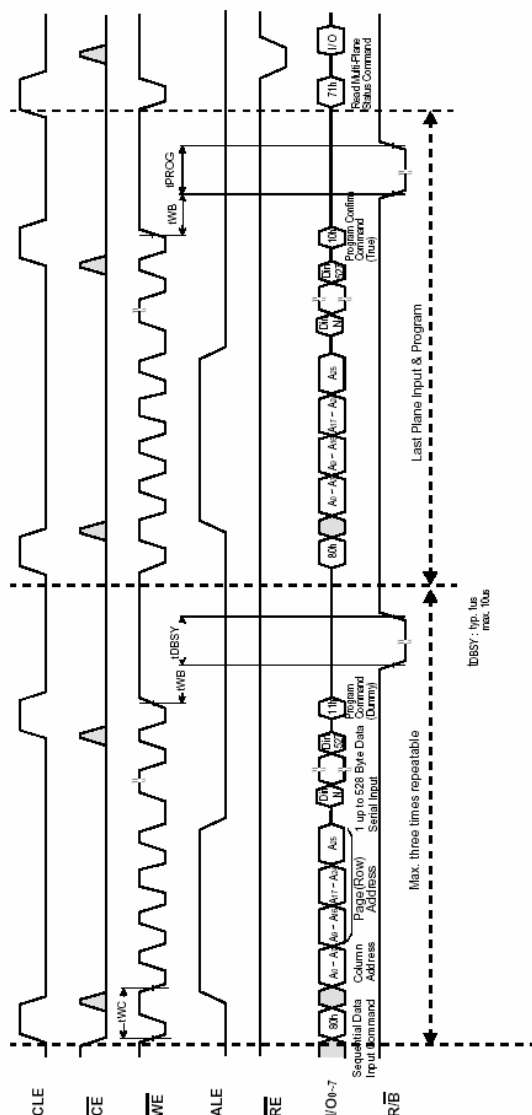
Page Program Operation



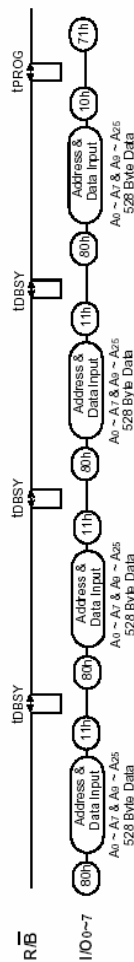
Block Erase Operation (ERASE ONE BLOCK)



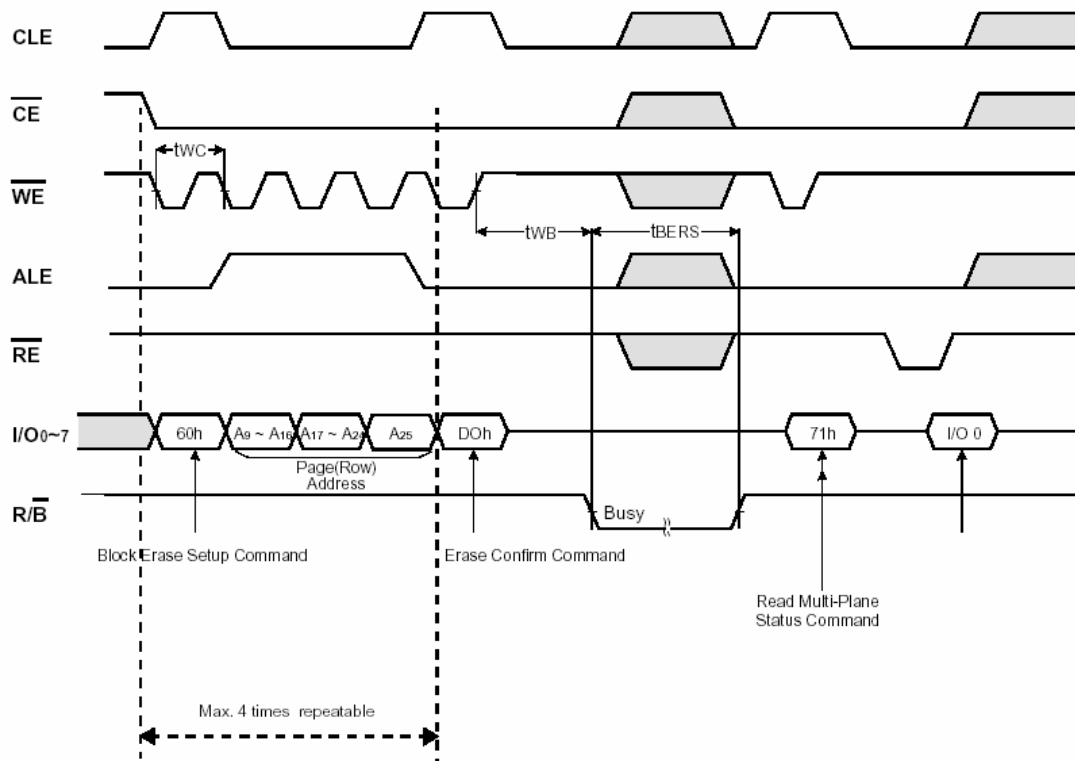
Multi-Plane Page Program Operation



Ex.) Four-Plane Page Program

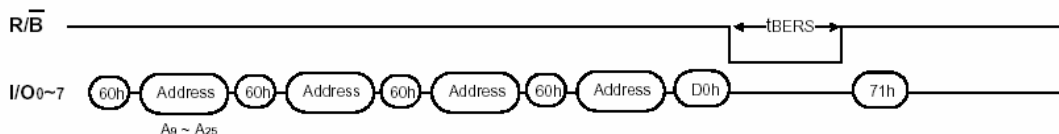


Multi-Plane Block Erase Operation

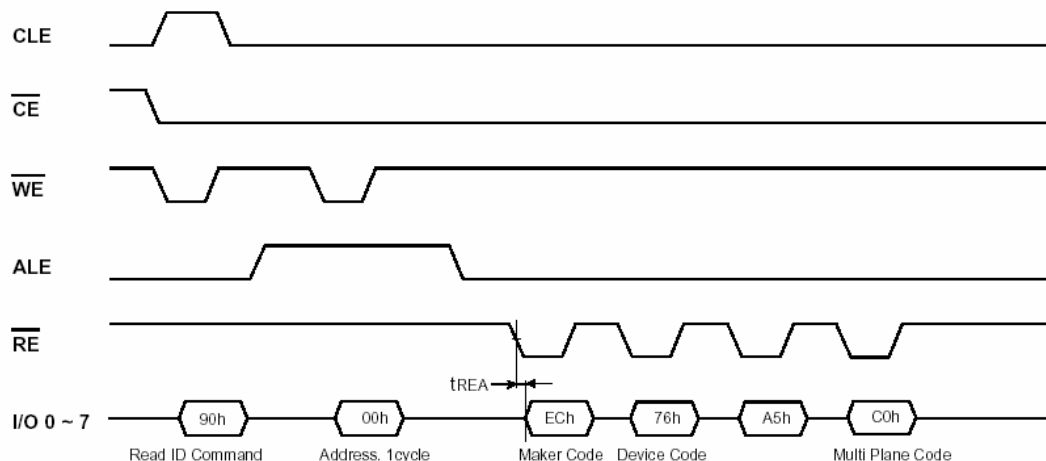


* For Multi-Plane Erase operation, Block address to be erased should be repeated before "D0H" command.

Ex.) Four-Plane Block Erase Operation



Read ID Operation

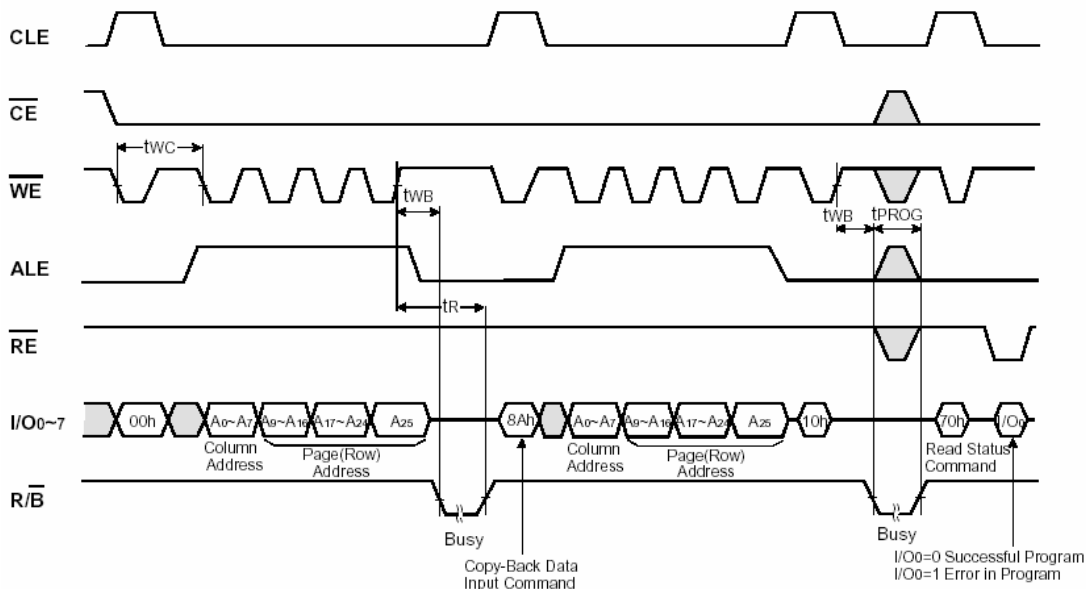


ID Definition Table

90 ID : Access command = 90H

	Value	Description
1 st Byte	ECh	Maker Code
2 nd Byte	79h	Device Code
3 rd Byte	A5h	Must be don't -cared
4 th Byte	C0h	Supports Multi Plane Operation

Copy-Back Program Operation

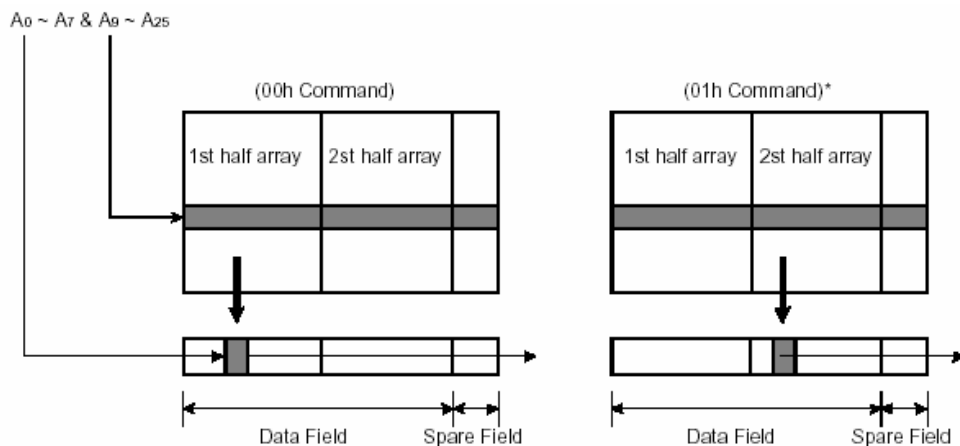
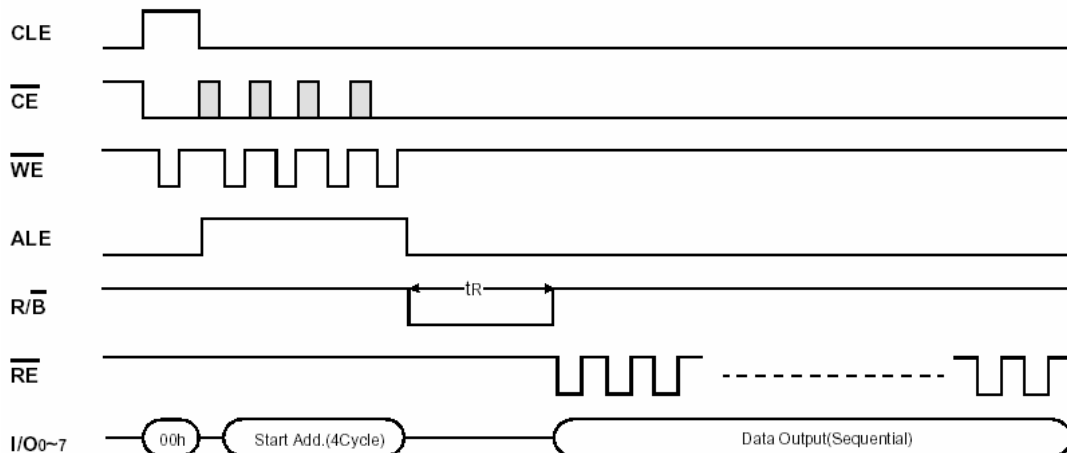


Device Operation

PAGE READ

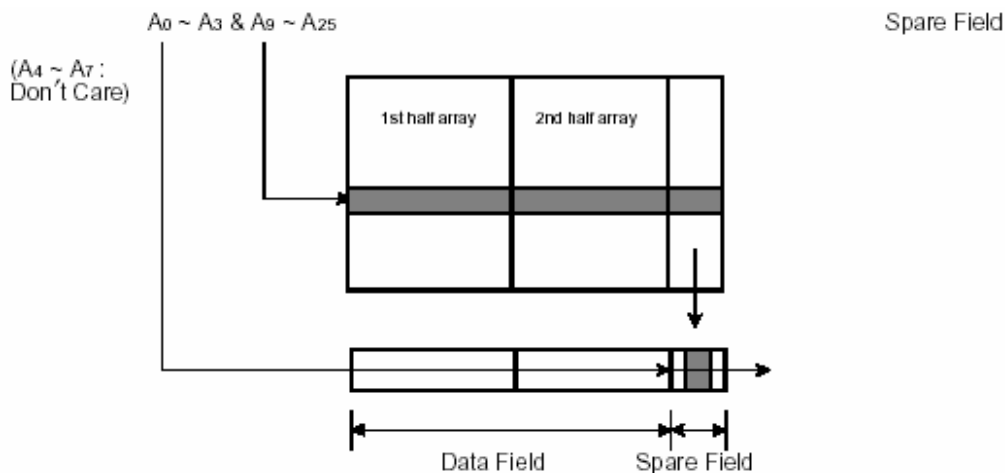
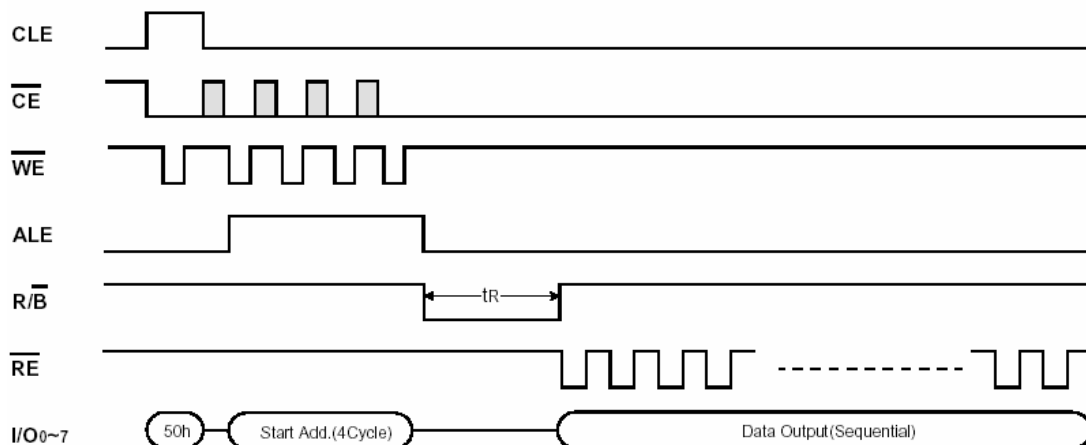
Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available: random read, serial page read and sequential row read. The random read mode is enabled when the page address is changed. The 2X528 bytes of data within the selected page are transferred to the data registers in less than 12 μ s (t_R). The system controller can detect the completion of this data transfer (t_R) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE. High to low transitions of the RE clock output the data stating from the selected column address up to the last column address. After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 12 μ s again allows reading the selected page. The sequential row read operation is terminated by bringing CE high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command (00h/01h) is needed to move the pointer back to the main area. Figures 8 to 11 show typical sequence and timings for each read operation.

Read1 Operation

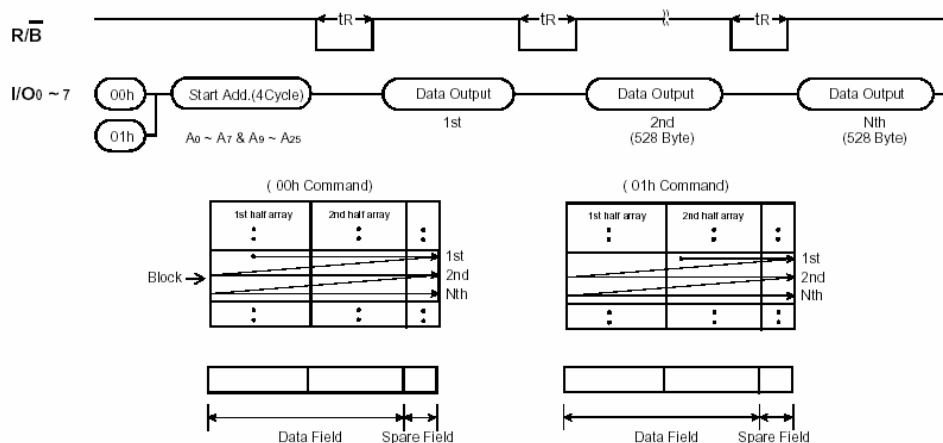


* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Read2 Operation

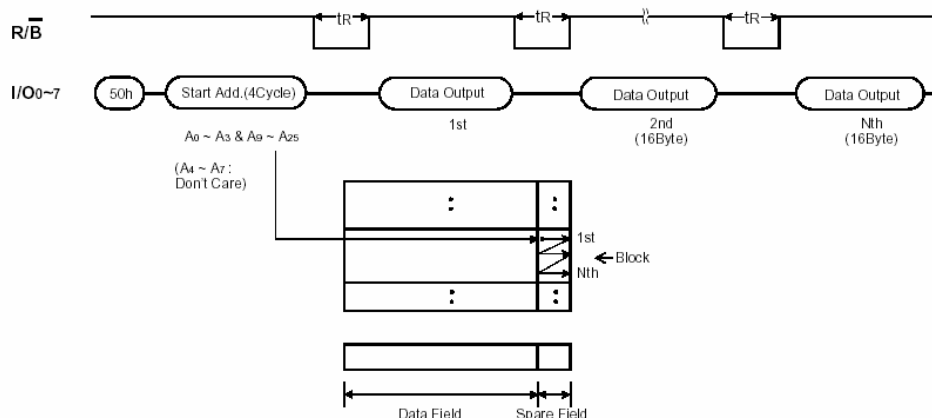


Sequential Row Read1 Operation



The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is read-out, the sequential read operation must be terminated by bringing CE high. When the page address moves onto the next block, read command and address must be given.

Sequential Row Read2 Operation



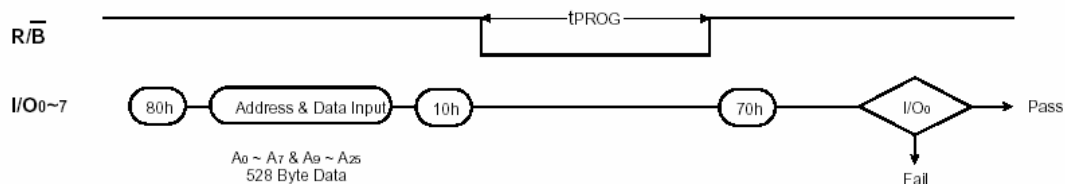
Page Program

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 2X528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 2X528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes. The serial data-loading period begins by inputting the Serial Data Input command (80h), followed by the four-cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded. The Page Program confirm command (10h) initiates the programming process.

Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with RE and CE low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked (Figure 12).

The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

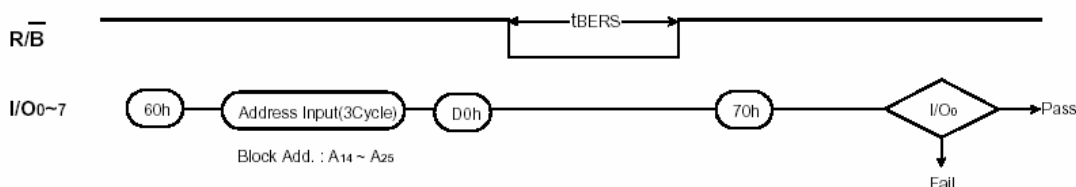
Program & Read Status Operation



Block Erase

The Erase operation is done on a block (16K Byte) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only address A₁₄ to A₂₅ is valid while A₉ to A₁₃ is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure 13 details the sequence.

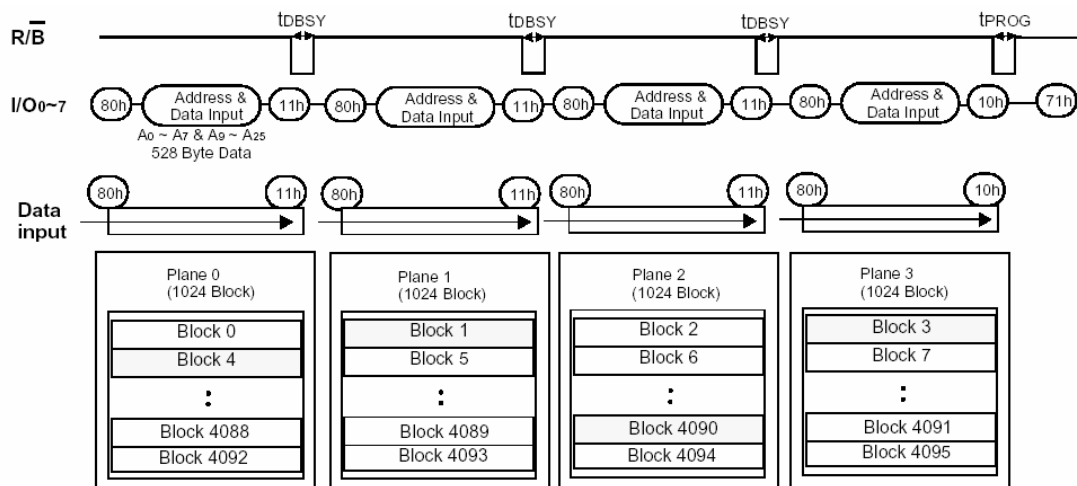
Block Erase Operation



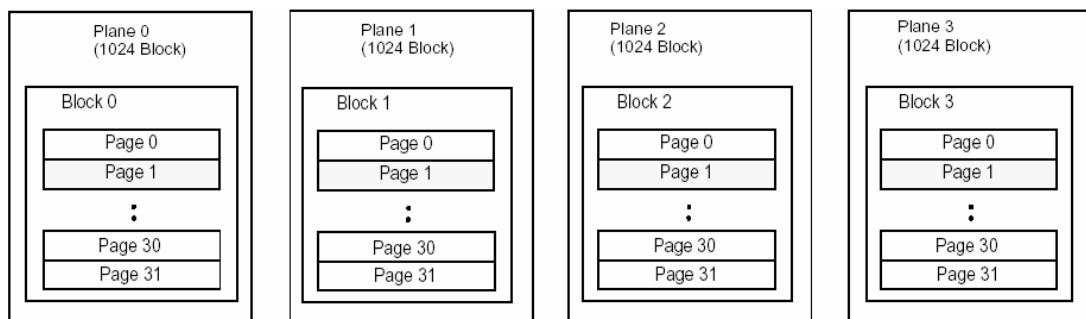
Multi-Plane Page Program

Multi-Plane Page Program is an extension of Page Program, which is executed for a single plane with 2X528 byte page registers. Since the device is equipped with four memory planes, activating the four sets of 2X528 byte page registers enables a simultaneous programming of four pages. Partial activation of four planes is also permitted. After writing the first set of data up to 2X528 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program (10h) is inputted to finish data-loading of the current plane and move to the next plane. Since no programming process is involved, R/B remains in Busy state for a short period of time (t_{DBSY}). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit (I/O 6). Then the next set of data for one of the other planes is inputted with the same command and address sequences. After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Since maximum four pages are programmed simultaneously, pass/fail status is available for each page when the program operation completes. The extended status bits (I/O1 through I/O 4) are checked by inputting the Read Multi-Plane Status Register. Status bit of I/O 0 is set to "1" when any of the pages fails. Multi-Plane page Program with "01h" pointer is not supported thus prohibited.

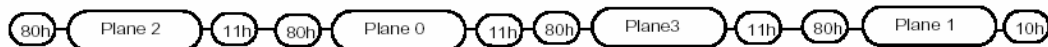
Four-Plane Page Program



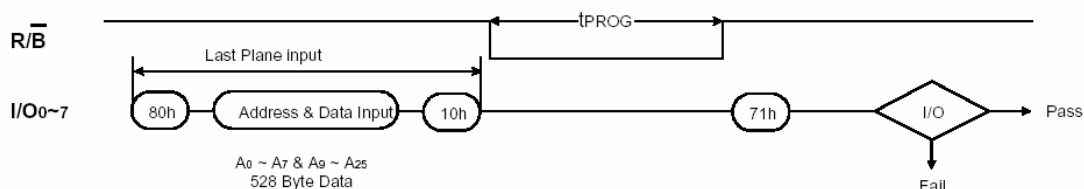
Multi-Plane Program & Read Status Operation



Addressing Multiple Planes



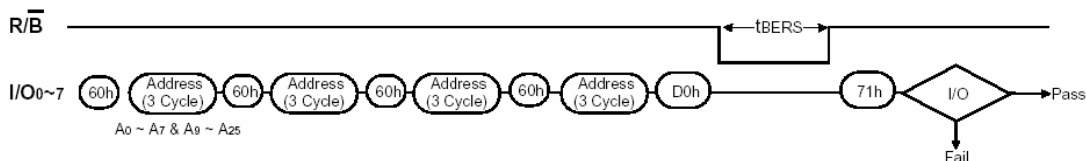
Multi-Plane Page Program & Read Status Operation



Multi-Plane Block Erase

Basic concept of Multi-Plane Block Erase operation is identical to that of Multi-Plane Page Program. Up to four blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command followed by three address cycles) may be repeated up to four times for erasing up to four blocks. Only one block should be selected from each plane. The Erase Confirm command initiates the actual erasing process. The completion is detected by analyzing R/B pin or Ready/Busy status (I/O 6). Upon the erase completion, pass/fail status of each block is examined by reading extended pass/fail status (I/O 1 through I/O 4).

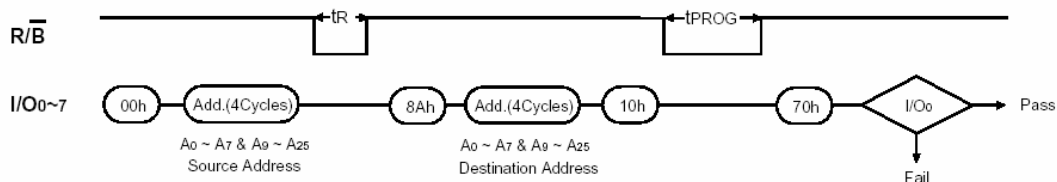
Four Block Erase Operation



Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without utilizing an external memory. Since the time-consuming sequentially-reading and its re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 2X528byte data into the internal page registers. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. A14 and A15 must be the same between source and target page. Figure19 shows the command sequence for single plane operation. **"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."**

One Page Copy-Back program Operation



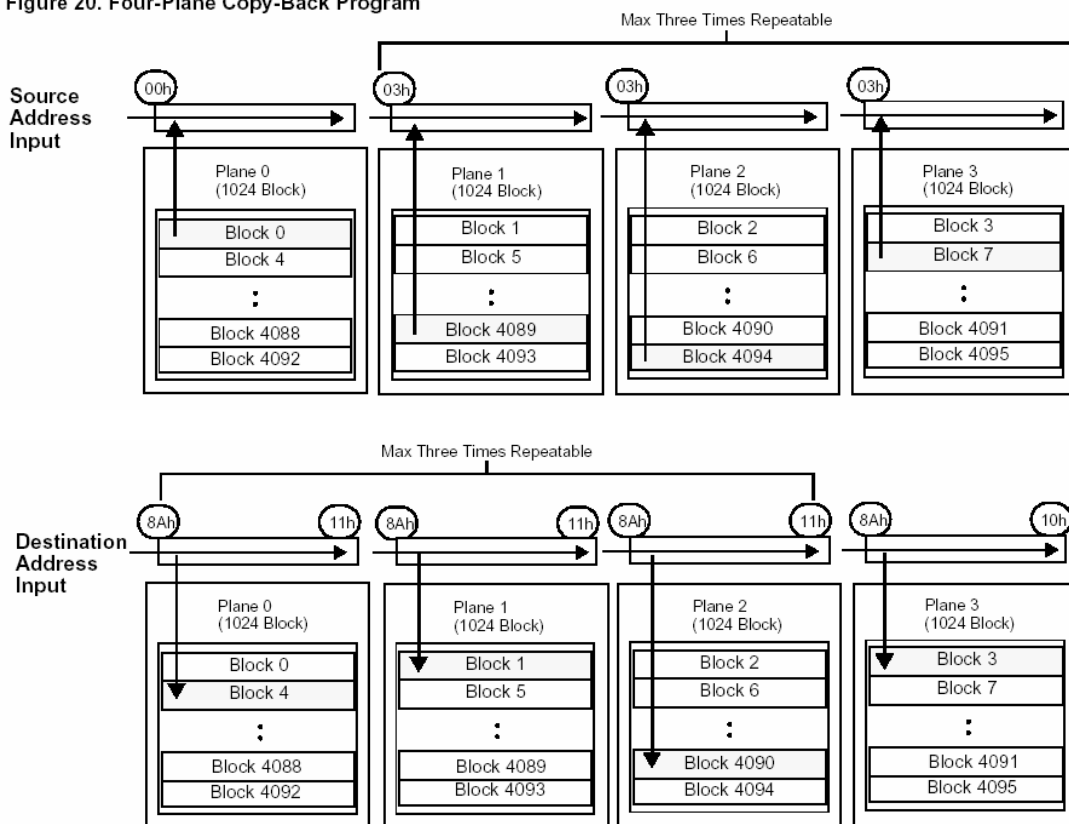
Multi-Plane Copy-Back Program

Multi-Plane Copy-Back Program is an extension of one page Copy-Back Program into four plane operation. Since the device is equipped with four memory planes, activating the four sets of 2X528 byte page registers enables a simultaneous Multi-Plane Copy-Back programming of four pages. Partial activation of four planes is also permitted. First, normal read operation with the "00h" command and address of the source page moves the whole 2X528 byte data into internal page buffers. Any further read operation for transferring the addressed pages to the corresponding page register must be executed with "03h" command instead of "00h" command. Any plane may be selected without regard to "00h" or "03h". Up to four planes may be addressed. Data moved into the internal page registers are loaded into the destination plane addresses. After the input of command sequences for reading the source pages, the same procedure as Multi-Plane Page programming except for a replacement address command with "8Ah" is executed. Since no programming process is involved during data loading at the destination plane address, R/B remains in Busy state for a short period of time (tDBSY). Read Status command (standard 70h or alternate 71h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit (I/O 6). After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Since maximum four pages are programmed simultaneously, pass/fail status is available for each page when the program operation completes.

No pointer operation is supported with Multi-Plane Copy-Back Program. **Once the Multi-Plane Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase once the Multi-Plane Copy-Back Program is finished.**

Four-Plane Copy-Back Program

Figure 20. Four-Plane Copy-Back Program



Read Status

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read Cycle, a read command (00h or 50h) should be given before sequential page read cycle. For Read Status of Multi Plane Program/Erase, the Read Multi-Plane Status command (71h) should be used to find out whether Multi-plane program or erase operation is completed, and whether the program or erase operation is completed successfully. The pass/fail status data must be checked only in the Ready condition after the completion of Multi-Plane program or erase operation.

Read Status Register Definition (8 Bit Mode)

I/O No.	Status	Definition by 70h Command		Definition by 71h Command	
I/O 0	Total Pass/Fail	Pass : "0"	Fail : "1"	Pass : "0" ⁽¹⁾	Fail : "1"
I/O 1	Plane 0 Pass/Fail	Must be don't -cared		Pass : "0" ⁽²⁾	Fail : "1"
I/O 2	Plane 1 Pass/Fail	Must be don't -cared		Pass : "0" ⁽²⁾	Fail : "1"
I/O 3	Plane 2 Pass/Fail	Must be don't -cared		Pass : "0" ⁽²⁾	Fail : "1"
I/O 4	Plane 3 Pass/Fail	Must be don't -cared		Pass : "0" ⁽²⁾	Fail : "1"
I/O 5	Reserved	Must be don't -cared		Must be don't-cared	
I/O 6	Device Operation	Busy : "0"	Ready : "1"	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Protected : "0"	Not Protected : "1"	Protected : "0"	Not Protected : "1"

NOTE: 1. I/O 0 describes combined Pass/Fail condition for all planes. If any of the selected multiple pages/blocks fails in Program/

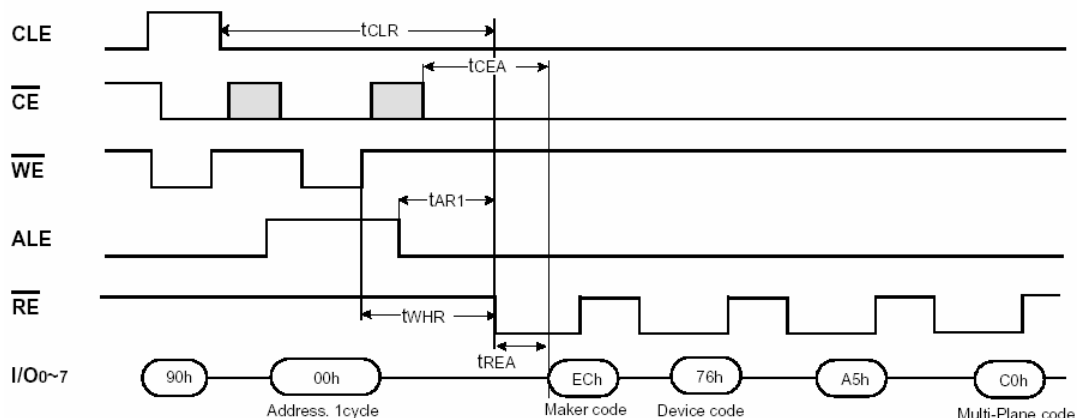
Erase operation, it sets "Fail" flag.

2. The pass/fail status applies only to the corresponding plane.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacture code (ECh), and the device code (76h), Reserved (A5h), Multi plane operation code (C0h) respectively. A5h must be don't-cared. C0h means that device supports Multi Plane operation. The command register remains in Read ID mode until further commands are issued to it.

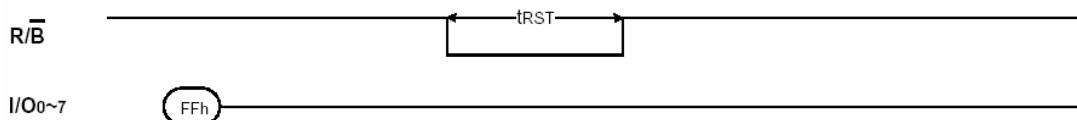
Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 4 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to Figure 23 below.

RESET Operation



Device Status

	After Power-up	After Reset
Operation Mode	Read	Waiting for next command

Ready/Busy

The device has a R/B output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to $t_r(R/B)$ and current drain during busy(i_{busy}), an appropriate value can be obtained with the following reference chart(Fig 24). Its value can be determined by the following guidance.

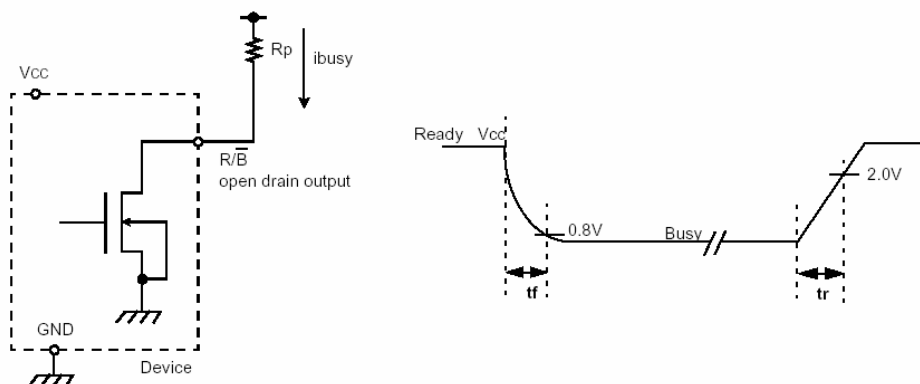
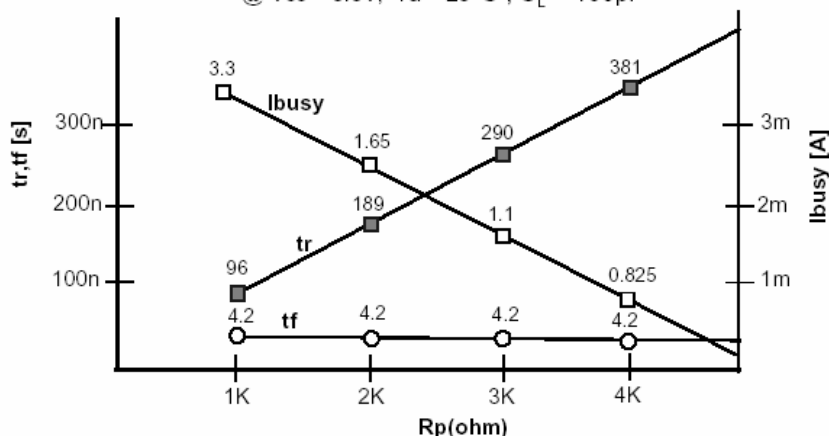


Fig 24 R_p vs t_r, t_f & R_p vs i_{busy}

@ $V_{cc} = 3.3V$, $T_a = 25^\circ C$, $C_L = 100pF$



Rp value guidance

$$R_{p(\min)} = \frac{V_{CC(\text{Max.})} - V_{OL(\text{Max.})}}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

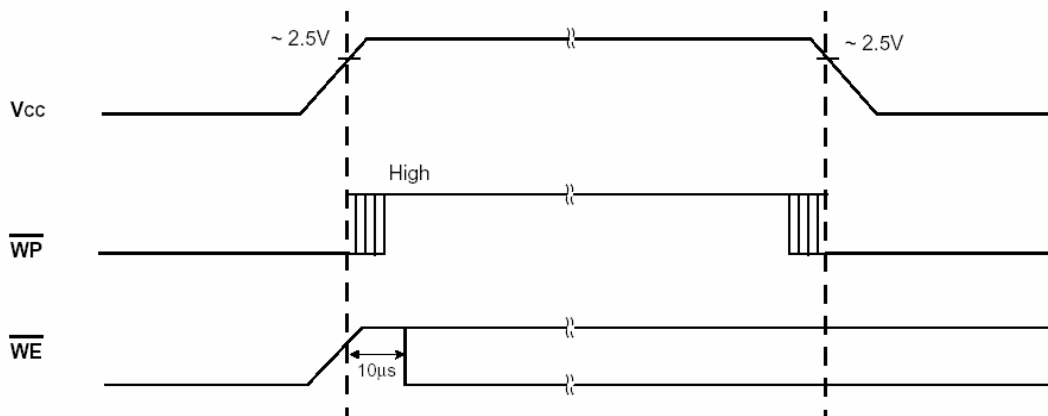
where I_L is the sum of the input currents of all devices tied to the $\overline{R/B}$ pin.

$R_{p(\max)}$ is determined by maximum permissible limit of t_r

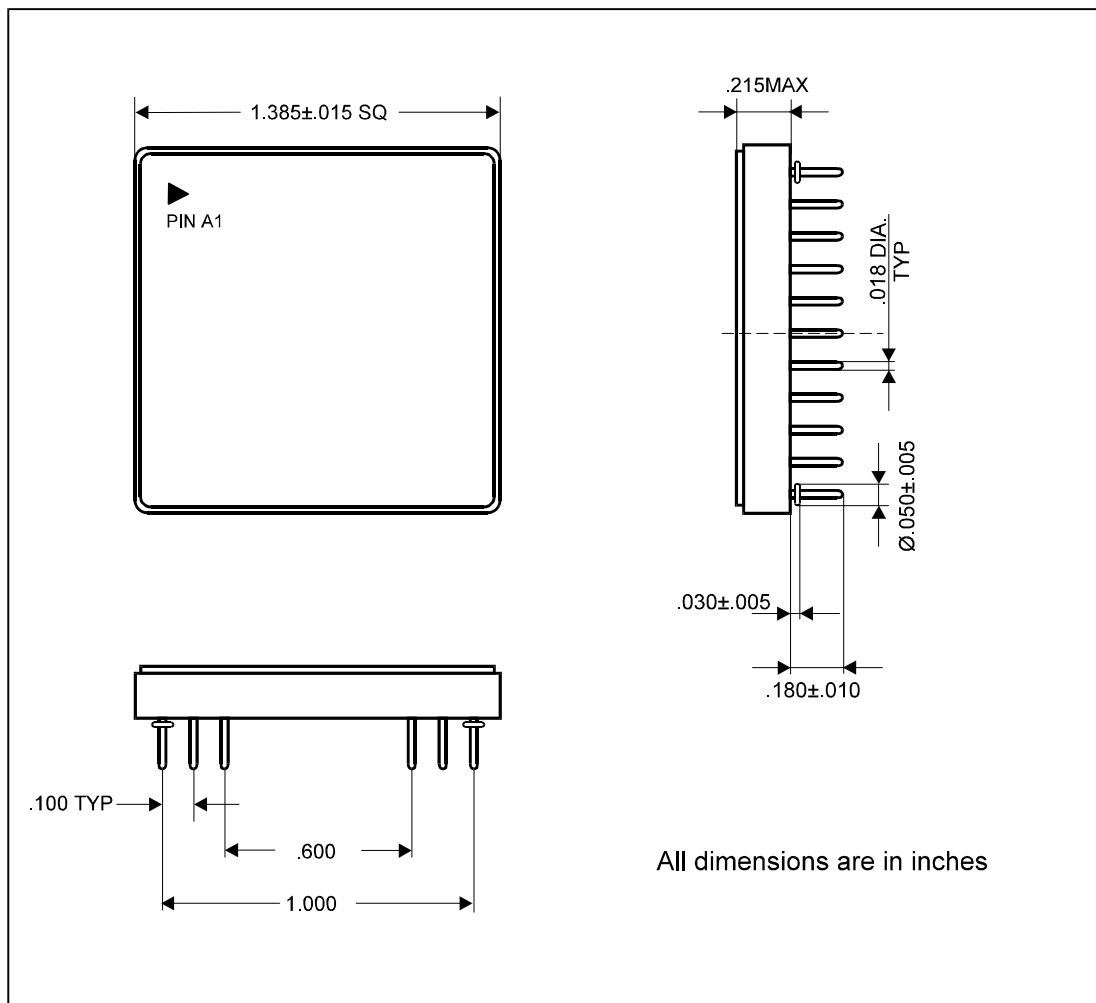
Data Protection & Power-up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2V. \overline{WP} pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum $10\mu s$ is required before internal circuit gets ready for any command sequences as shown in Figure 25. The two step command sequence for program/erase provides additional software protection.

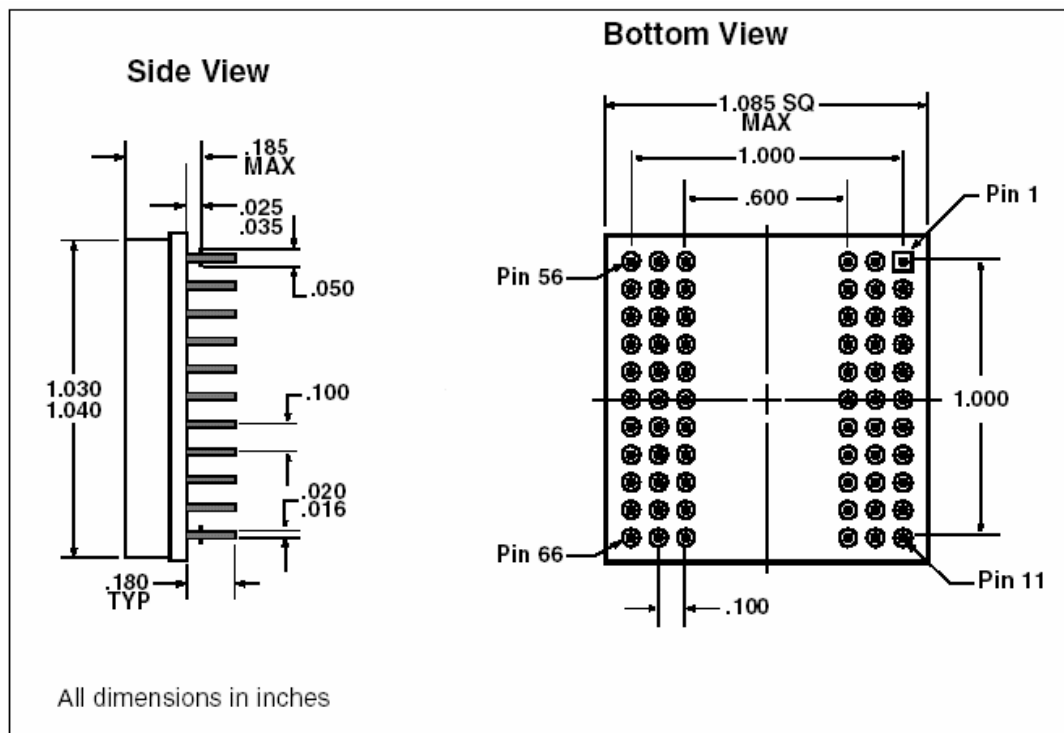
AC Waveforms for Power Transition



Outline Drawing for 66-Pin Ceramic PGA (G1)



Outline Drawing for 66-Pin Ceramic PGA (G7)



Ordering Information (Military & Industrial Screened Products*)

<i>Model Number</i>	<i>Speed</i>	<i>Package</i>
MEF64M16G150M3ND	50ns	CPGA
MEF64M16G150I3ND	50ns	CPGA
MEF64M16G750M3ND	50ns	CPGA
MEF64M16G750I3ND	50ns	CPGA

(*) - Contact Elisra for additional designs

Part Number Breakdown

