P-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME8117A-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 5.2m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 10.5m\Omega @ V_{GS}=-4V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

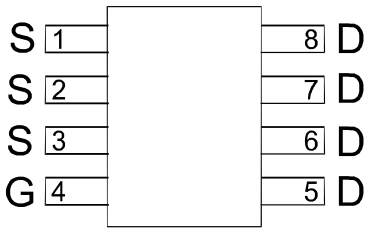
APPLICATIONS

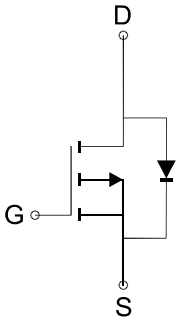
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOP-8)

Top View





P-Channel MOSFET

Ordering Information: ME8117A /ME8117A-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	-35	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Tj=150℃)	T_A=25℃	I_D	-17.3	A
	T_A=70℃		-14	
Pulsed Drain Current		I_{DM}	69	A
Maximum Power Dissipation*	T_A=25℃	P_D	2.5	W
	T_A=70℃		1.6	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	50	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{BR(DSS)}$	Drain-source breakdown voltage	I_D=-10mA, V_{GS}=0V	-35			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}= V_{DS}, I_D=-250 μA	-1		-3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-35V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -9A		4.3	5.2	mΩ
		V_{GS}=-4V, I_D= -9A		8	10.5	
V_{SD}	Diode Forward Voltage	I_{DR}=-18A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=-24V, V_{GS}=-10V, I_D=-18A		142		nC
Qg	Total Gate Charge	V_{DD}=-24V, V_{GS}=-4.5V, I_D=-18A		74		
Qgs	Gate-Source Charge			26		
Qgd	Gate-Drain Charge			41		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		6362		pF
Coss	Output Capacitance			773		
Crss	Reverse Transfer Capacitance			694		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L =15Ω V_{GS}=-10V,R_G=4.7Ω		74		nC
t_r	Turn-On Rise Time			31		
$t_{d(off)}$	Turn-Off Delay Time			270		
t_f	Turn-Off Fall Time			76		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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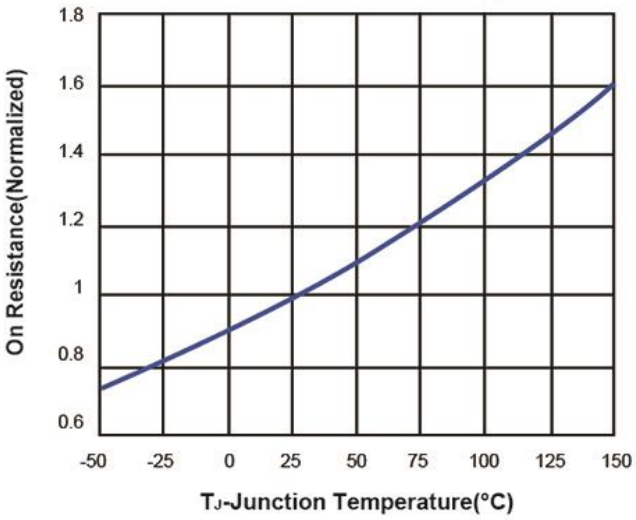
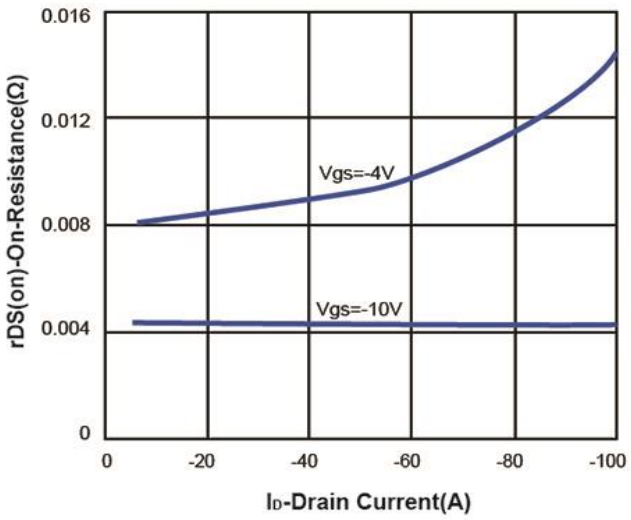
Typical Characteristics (T_J =25℃ Noted)

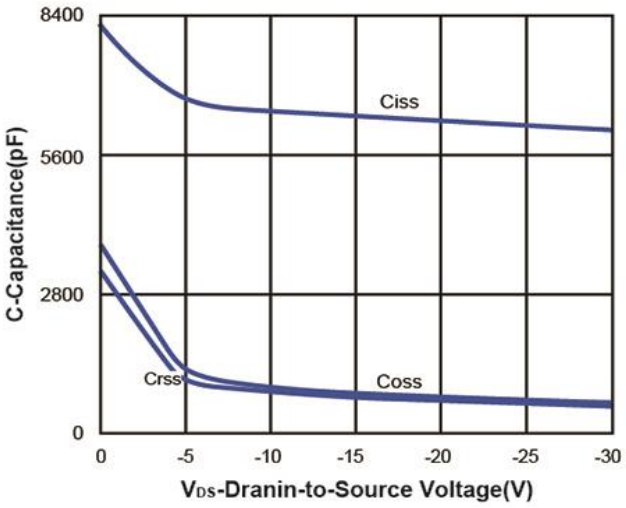
On Resistance vs. Junction Temperature



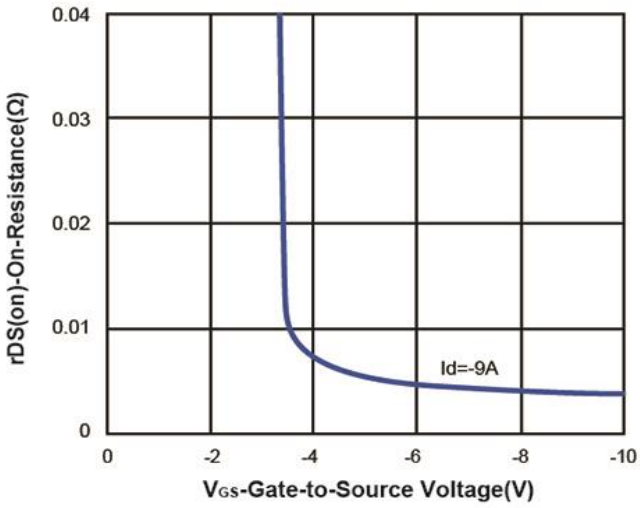
On Resistance vs. Drain Current



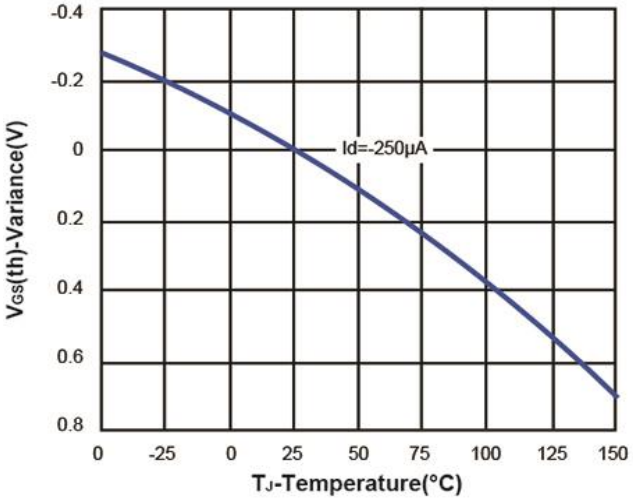
Capacitance



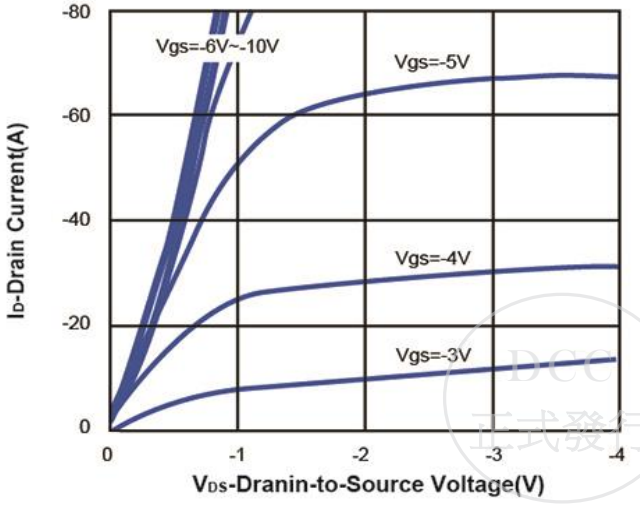
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



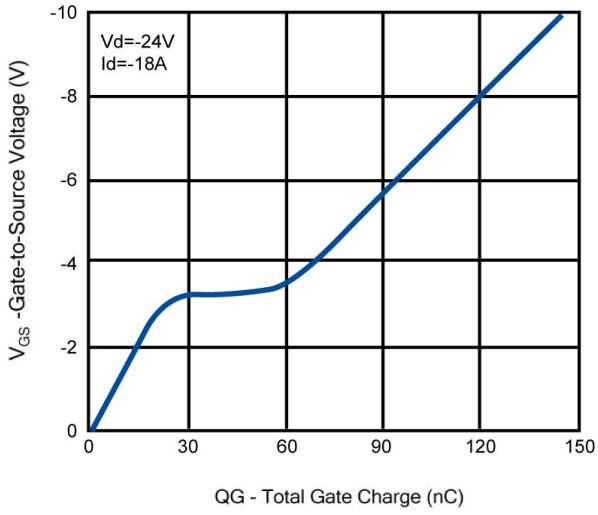
On-Region Characteristics



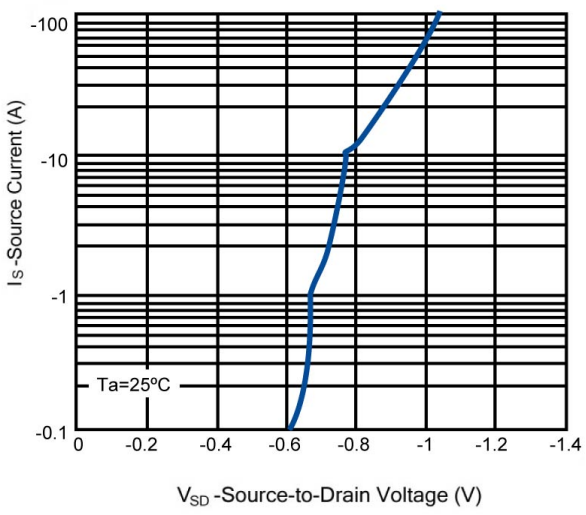
P-Channel Enhancement Mode MOSFET

Typical Characteristics (T_J =25℃ Noted)

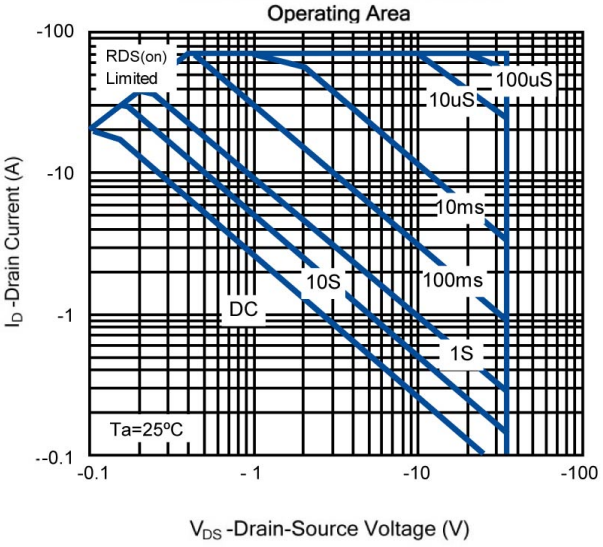
Gate Charge



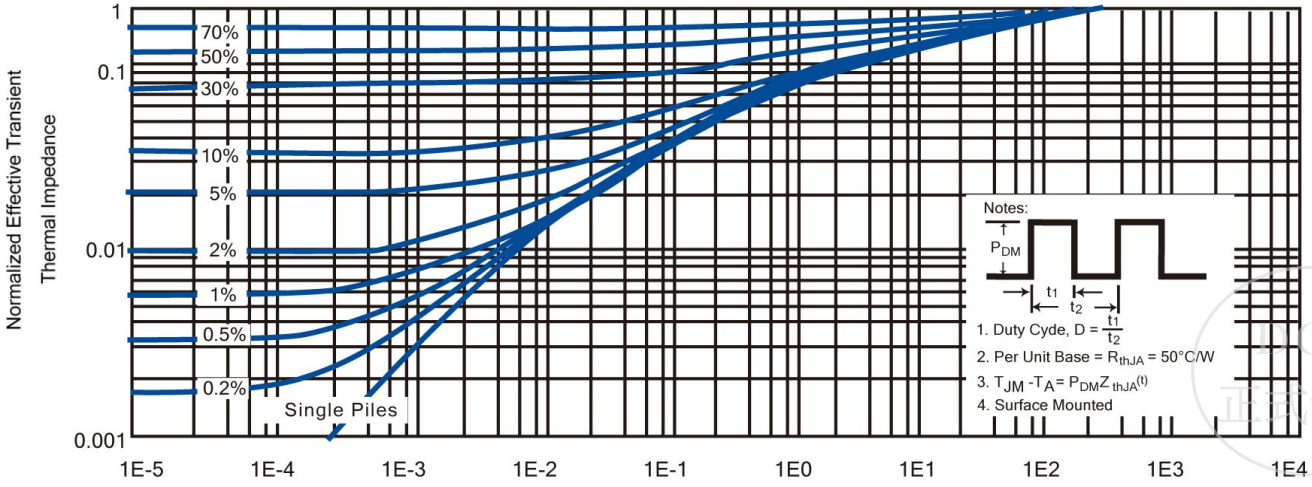
Source to Drain Diode Forward Voltage



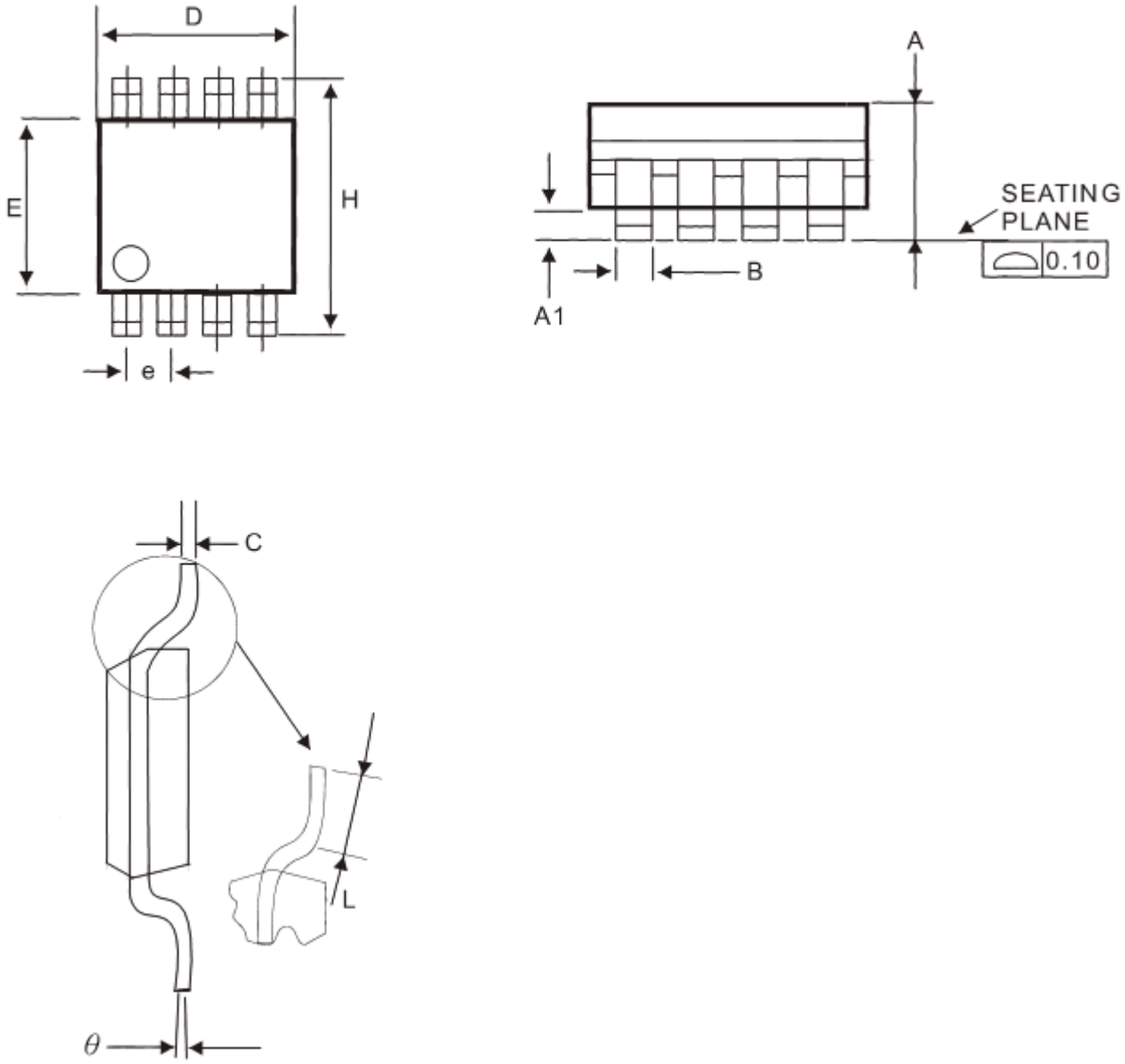
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline



Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.