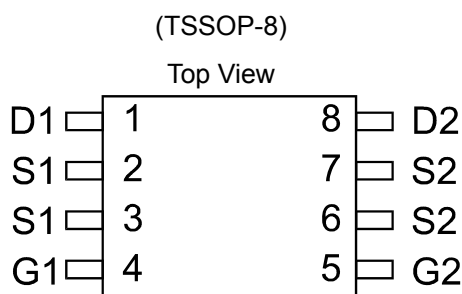


Dual N-Channel 20-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME6970D Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

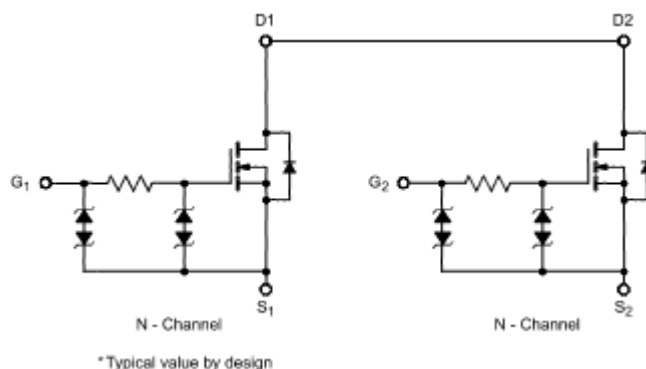


FEATURES

- $R_{DS(ON)} \leq 22m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 23m\Omega @ V_{GS}=4.0V$
- $R_{DS(ON)} \leq 26m\Omega @ V_{GS}=3.0V$
- $R_{DS(ON)} \leq 29m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC



Ordering Information: ME6970D (Pb-free)

ME6970D-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	± 12	V
Continuous Drain Current ($T_J=150^\circ\text{C}$)	$T_A=25^\circ\text{C}$	I_D	6.3	A
	$T_A=70^\circ\text{C}$		5.0	
Pulsed Drain Current		I_{DM}	25	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.3	W
	$T_A=70^\circ\text{C}$		0.8	
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	$^\circ\text{C/W}$

* The device mounted on 1in² FR4 board with 2 oz copper

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Dual N-Channel 20-V (D-S) MOSFET

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	0.5		1.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = $\pm$ 8V			$\pm$ 10	μ A
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =4.5V, I _D = 7A		15.5	22	m Ω
		V _{GS} =4V, I _D = 6.8A		16	23	
		V _{GS} =3V, I _D = 6.3A		18	26	
		V _{GS} =2.5V, I _D = 6.0A		20	29	
V _{SD}	Diode Forward Voltage	I _S =7A, V _{GS} =0V			1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =10V, I _D =6.5A		24		nC
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =4.5V, I _D =6.5A		12		
Q _{gs}	Gate-Source Charge			1.9		
Q _{gd}	Gate-Drain Charge			3.7		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		360		pF
C _{oss}	Output Capacitance			100		
C _{rss}	Reverse Transfer Capacitance			31		
t _{d(on)}	Turn-On Delay Time	V _{DD} =10V, R _L =10 Ω I _D =1A, V _{GEN} =4.5V R _G =6 Ω		311		ns
t _r	Turn-On Rise Time			441		
t _{d(off)}	Turn-Off Delay Time			4130		
t _f	Turn-Off Fall Time			1440		

Notes: a. pulse test: pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

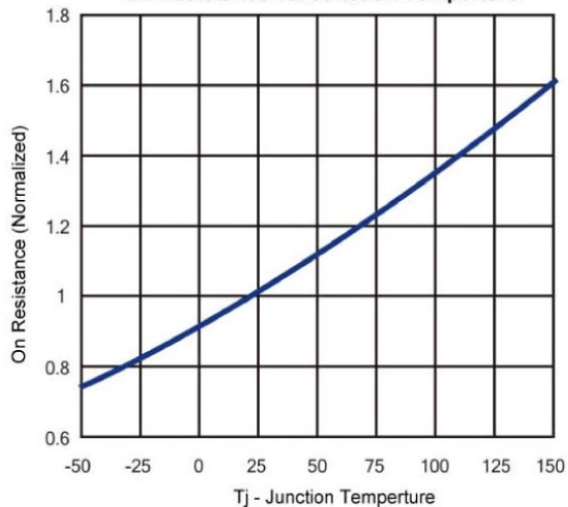
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



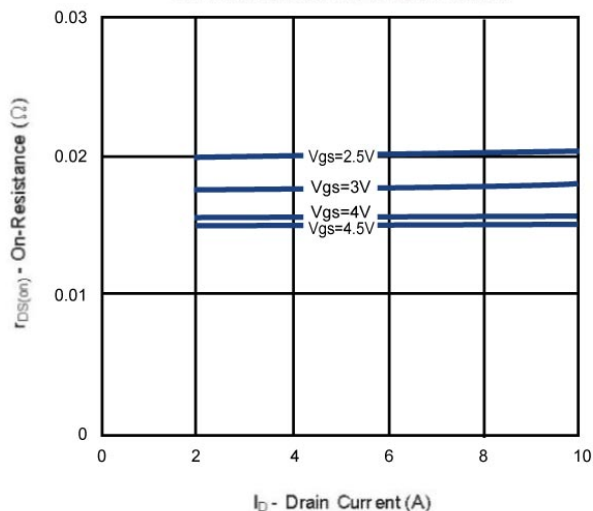
Dual N-Channel 20-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

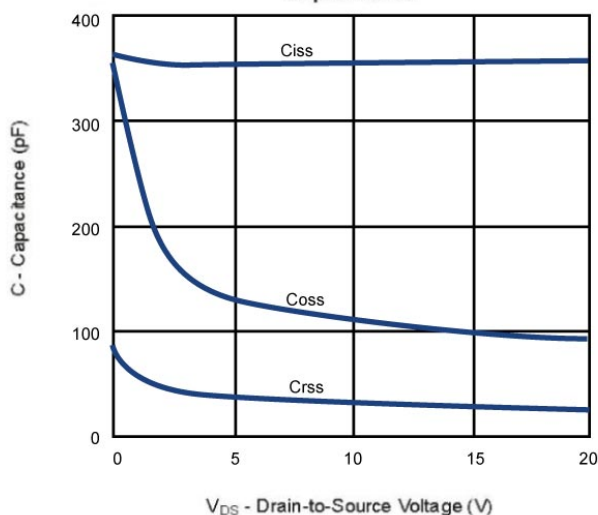
On Resistance vs. Junction Temperature



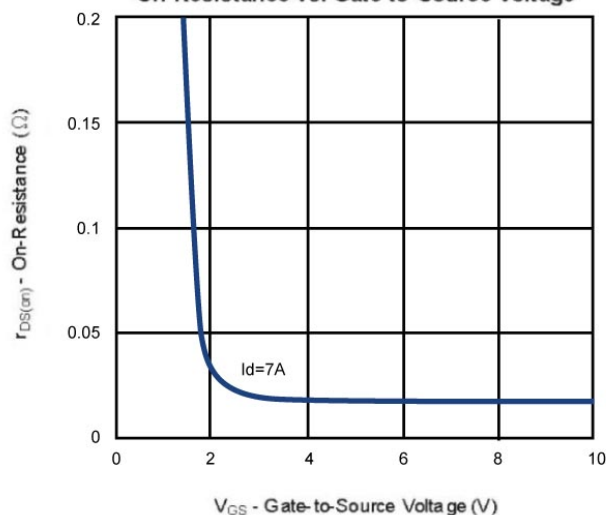
On-Resistance vs. Drain Current



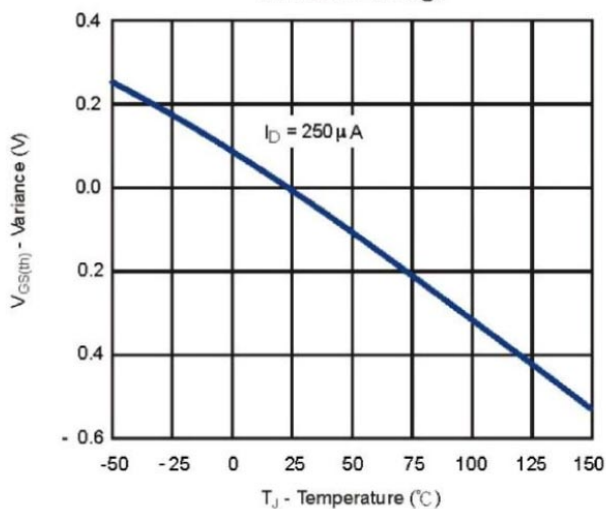
Capacitance



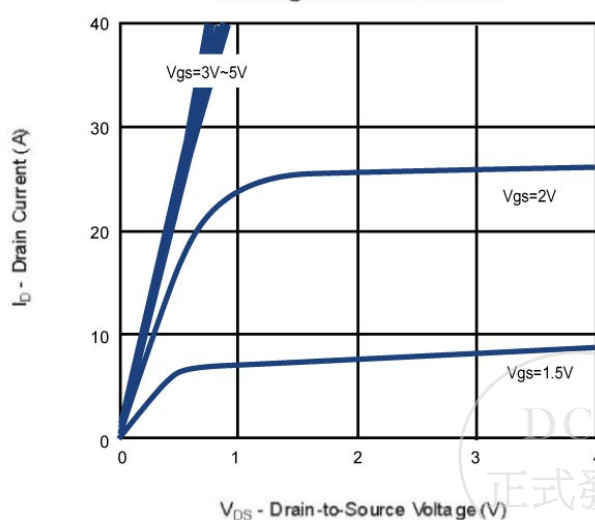
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

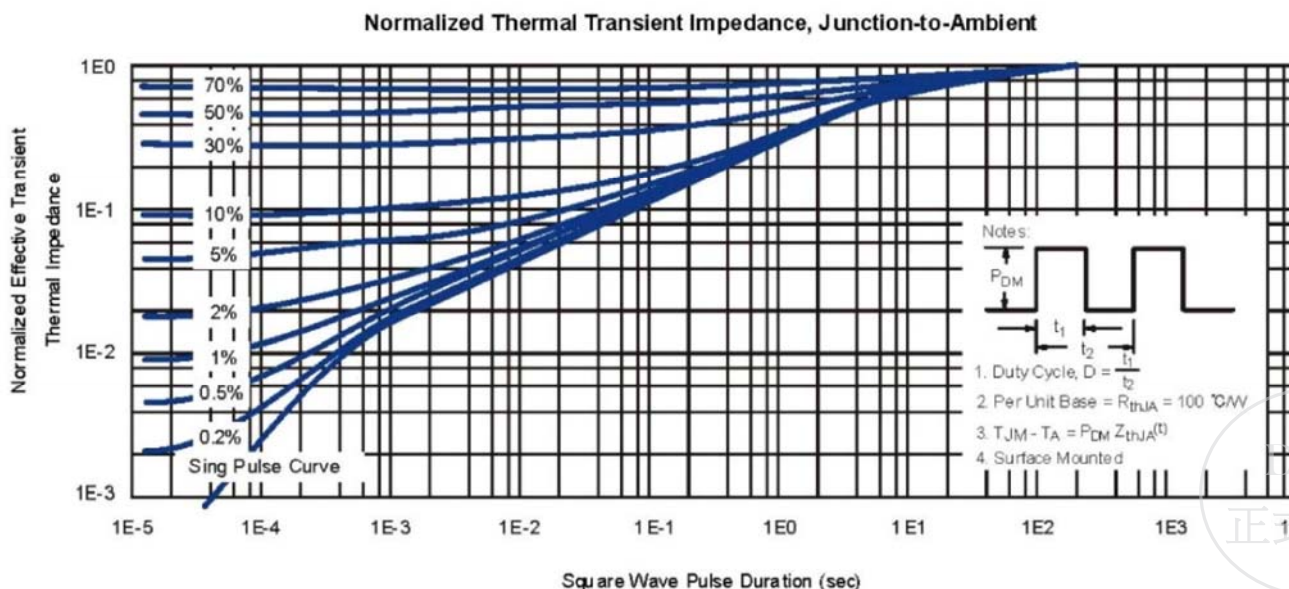
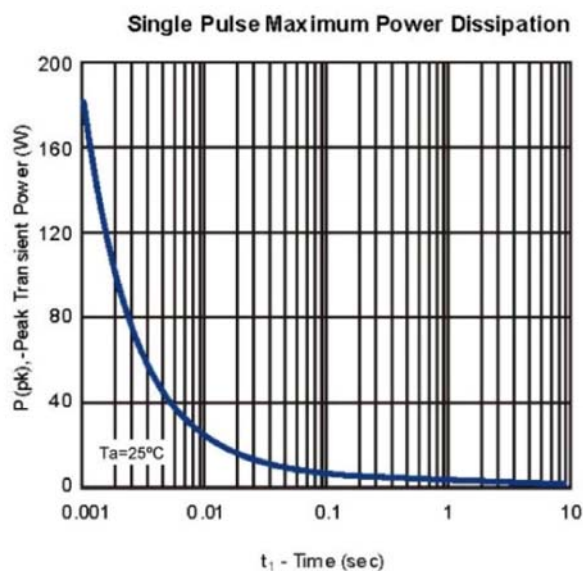
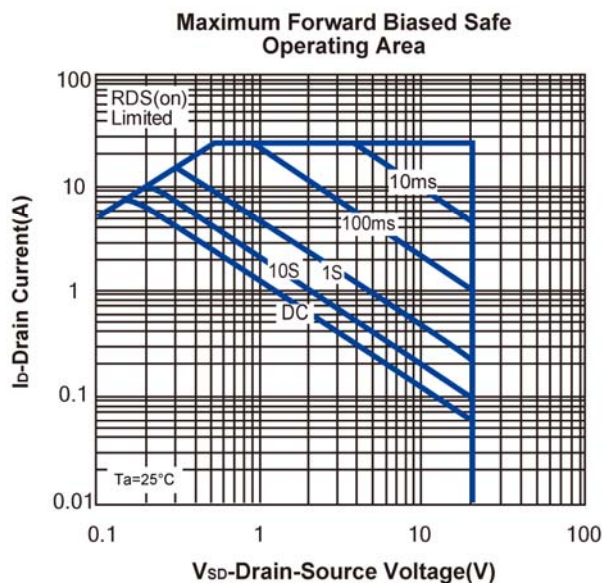
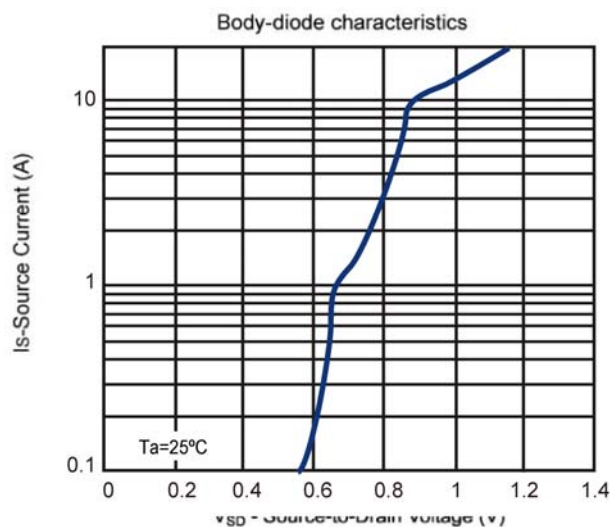
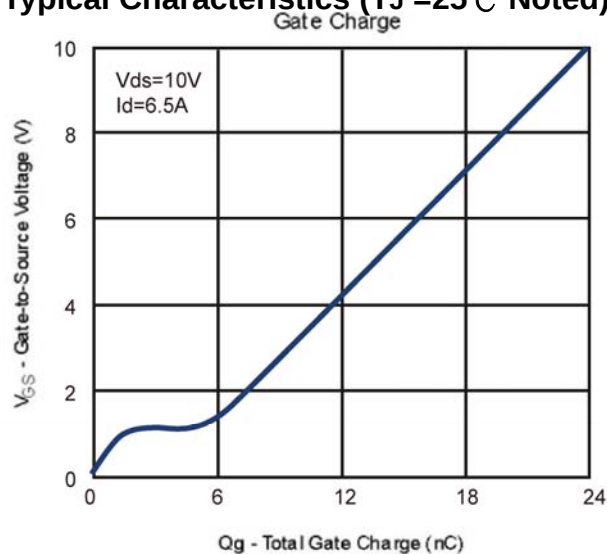


On-Region Characteristics

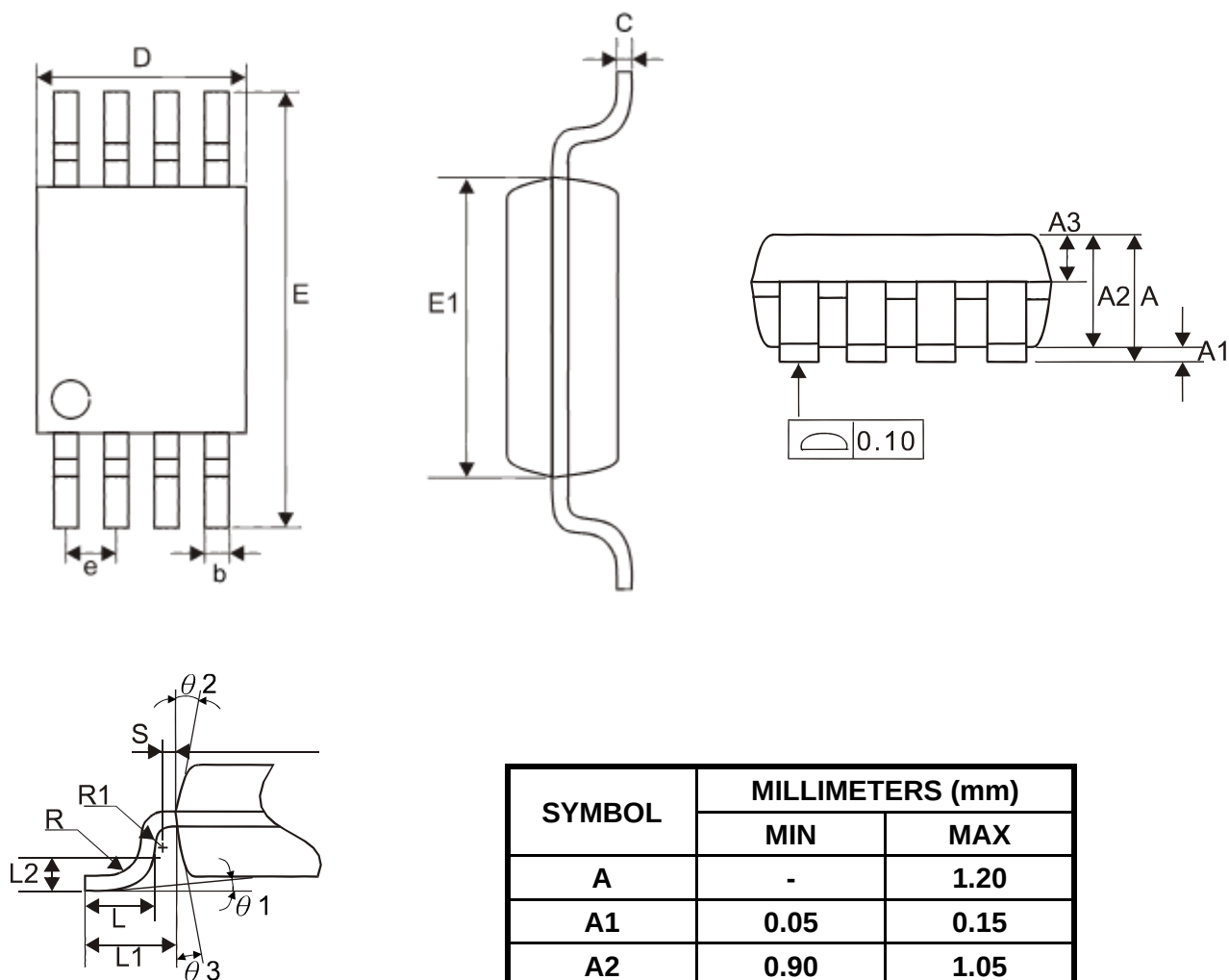


Dual N-Channel 20-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)



TSSOP-8 Package



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.34	0.54
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L1	1.00REF	
L2	0.25BSC	
R	0.09	-

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