N- Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME50N10 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 17m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

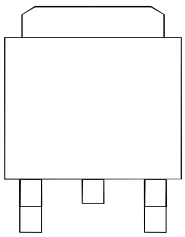
APPLICATIONS

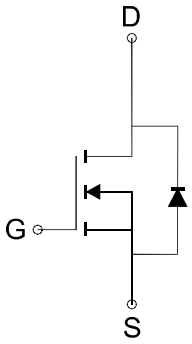
- Power Management
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME50N10 (Pb-free)

ME50N10-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	50.5	A
	T_C=70℃		40.4	
Pulsed Drain Current		I_{DM}	202	A
Maximum Power Dissipation	T_C=25℃	P_D	69.4	W
	T_C=70℃		44.4	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	1.8	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper.

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Electrical Characteristics (T_C=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=25A		14	17	mΩ
V_{SD}	Diode Forward Voltage *	I_S=45A, V_{GS}=0V		0.9	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=80V, V_{GS}=10V, I_D=28A		121		nC
Qg	Total Gate Charge	V_{DD}=80V, V_{GS}=4.5V, I_D=28A		28		
Qgs	Gate-Source Charge			28.6		
Qgd	Gate-Drain Charge			34.4		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.8		Ω
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		6170		pF
Coss	Output Capacitance			427		
Crss	Reverse Transfer Capacitance			307		
$t_{d(on)}$	Turn-On Delay Time	V_{GS} =10V, R_L=1.8Ω V_{DD}=50V, R_G=2.5Ω, I_D=28A		42.4		ns
t_r	Turn-On Rise Time			85.7		
$t_{d(off)}$	Turn-Off Delay Time			154		
t_f	Turn-Off Fall Time			25		

Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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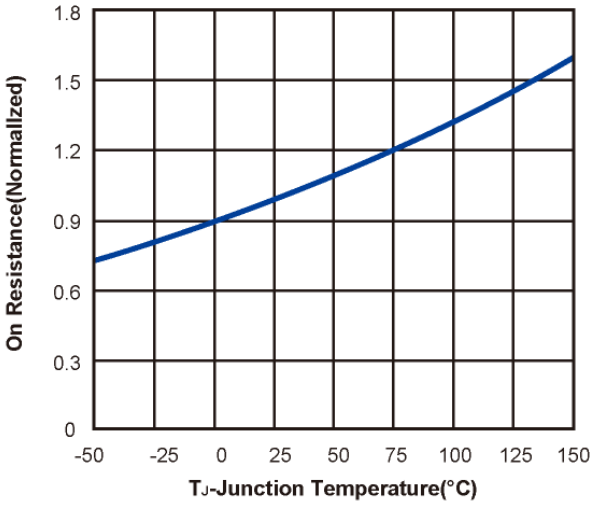
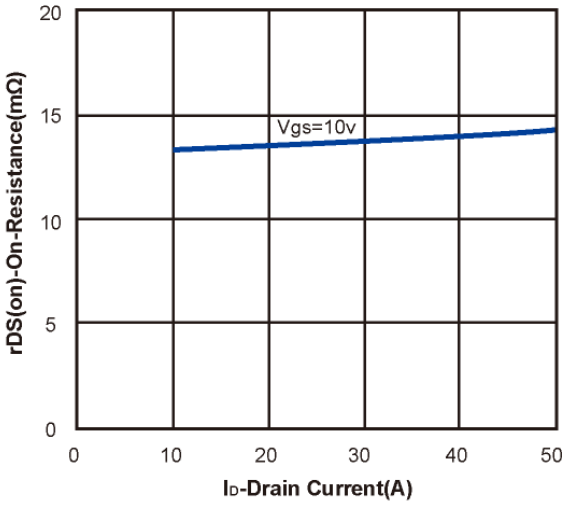
Typical Characteristics (T_J =25℃ Noted)

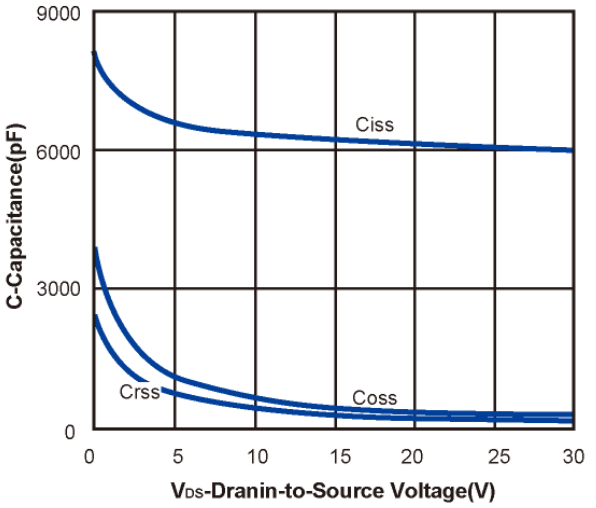
On Resistance vs. Junction Temperature



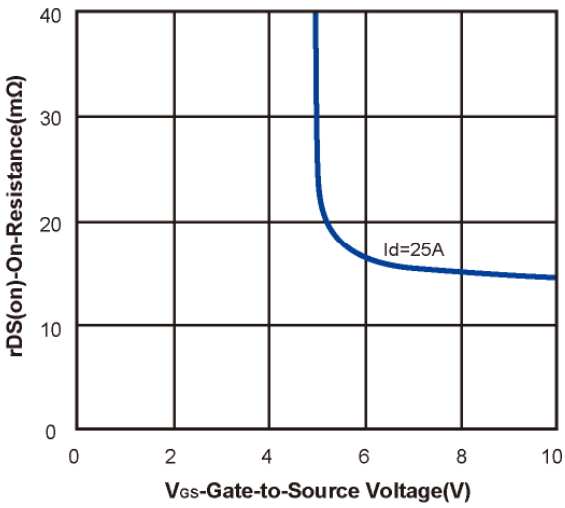
On Resistance vs. Drain Current



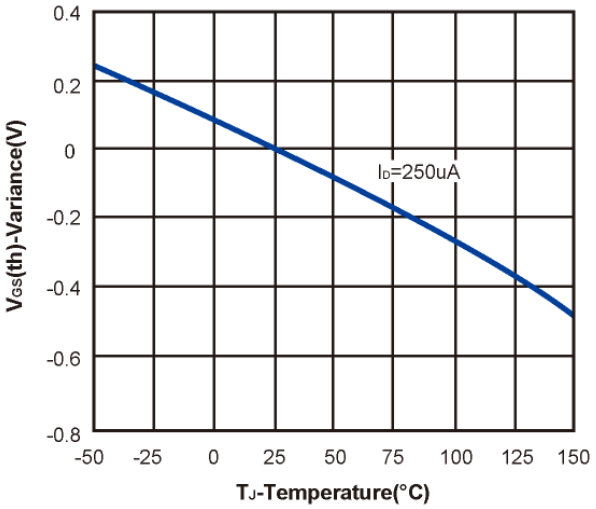
Capacitance



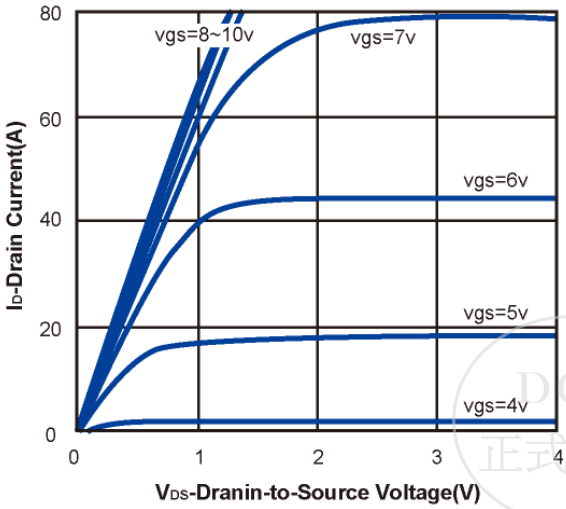
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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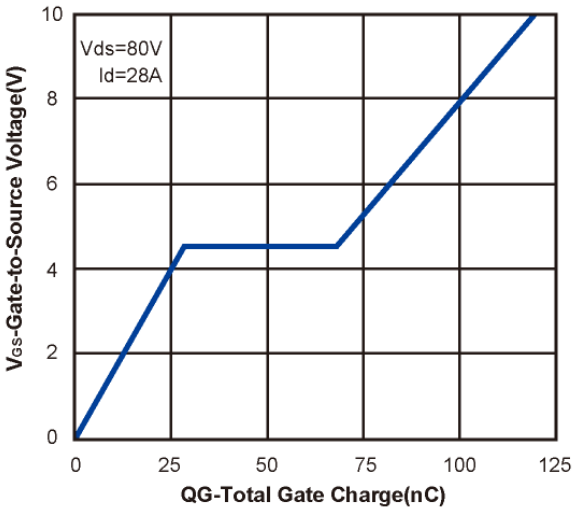
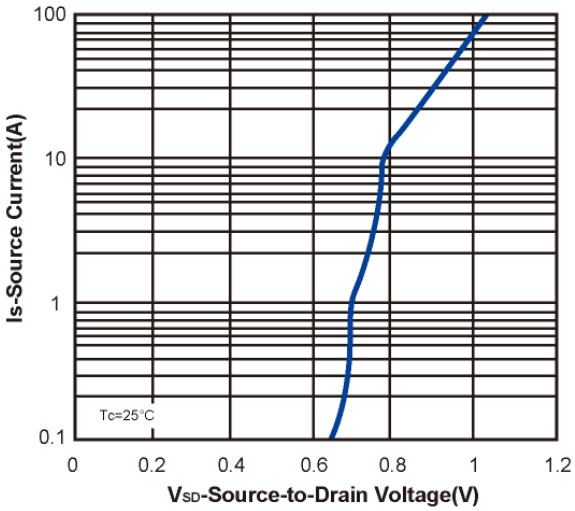
Typical Characteristics (T_J =25℃ Noted)

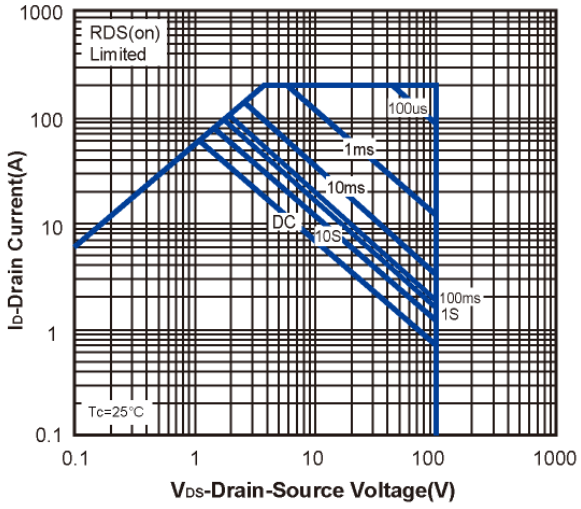
Gate Charge

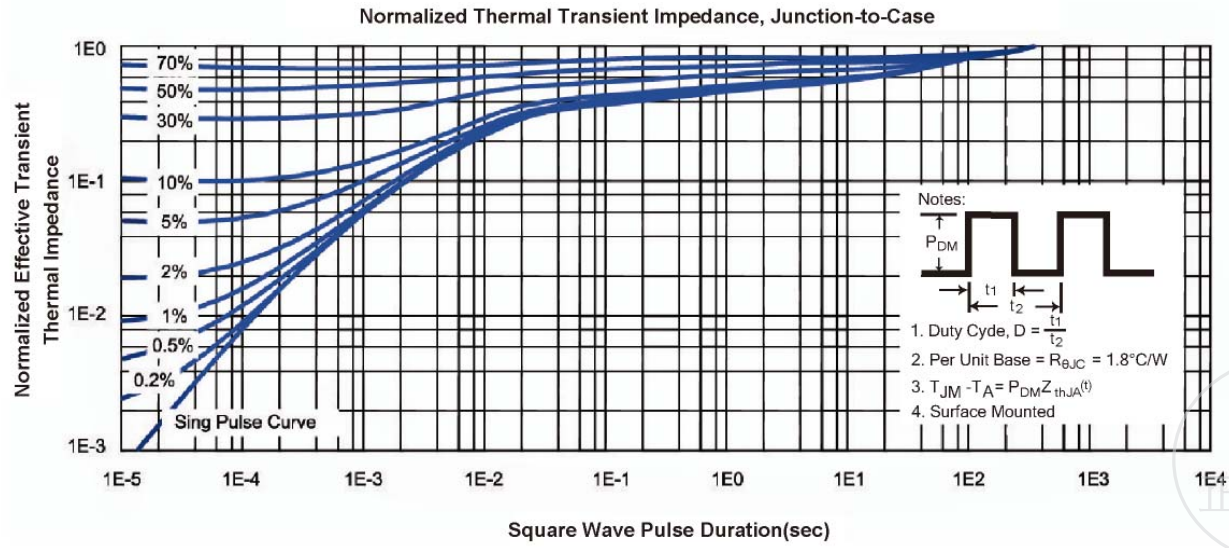


Body-diode characteristics

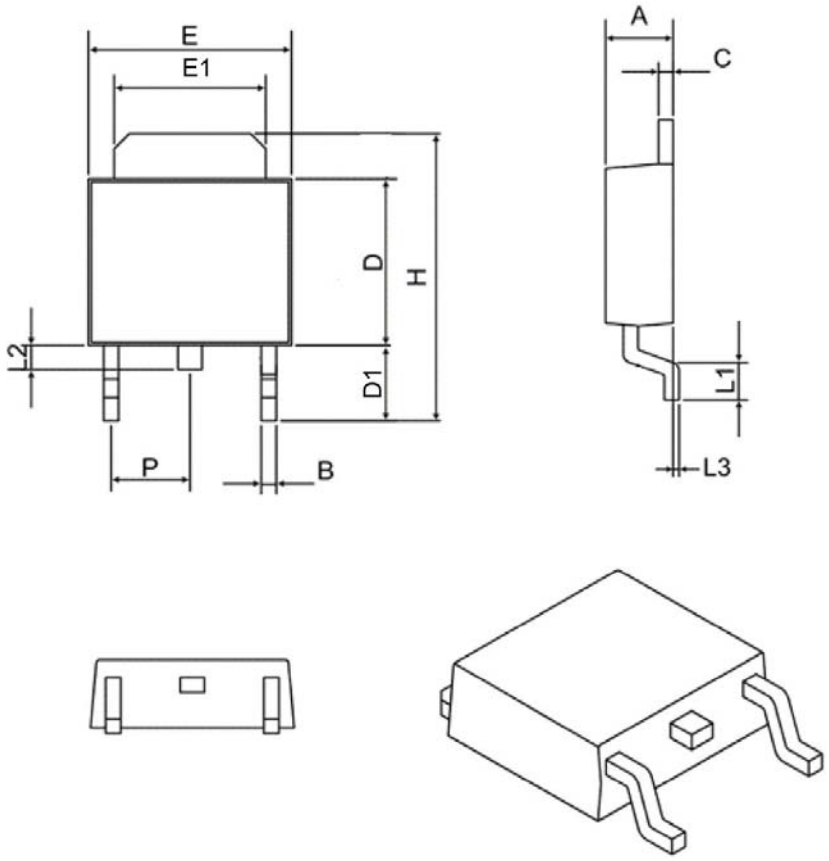


Maximum Forward Biased Safe Operating Area





TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

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