

30V N-Channel Enhancement Mode

GENERAL DESCRIPTION

The ME45N03T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leq 14m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 21m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

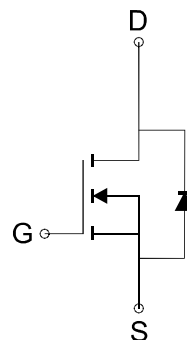
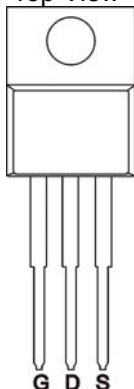
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-220)

Top View



N-Channel MOSFET

Ordering Information: ME45N03T (Pb-free)

ME45N03T-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current (Tj=150°C)	I_D	Tc=25°C	58
		Tc=70°C	48
Pulsed Drain Current	I_{DM}	232	A
Maximum Power Dissipation	P_D	Tc=25°C	75
		Tc=70°C	53
Operating Junction Temperature	T_J	-55 to 175	°C
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	2	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper



30V N-Channel Enhancement Mode

Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

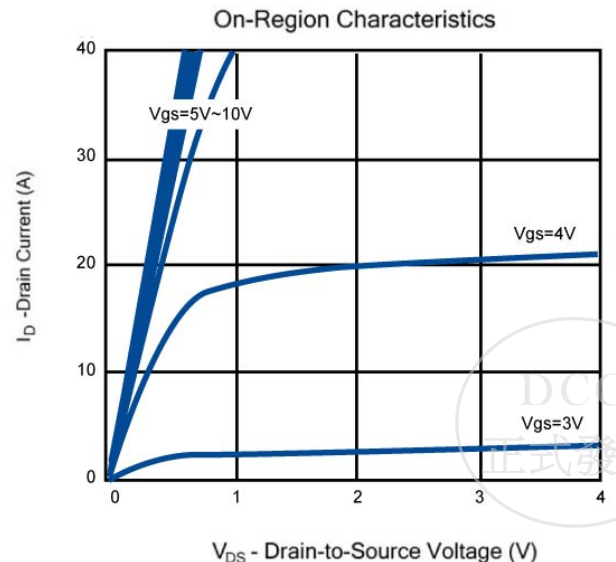
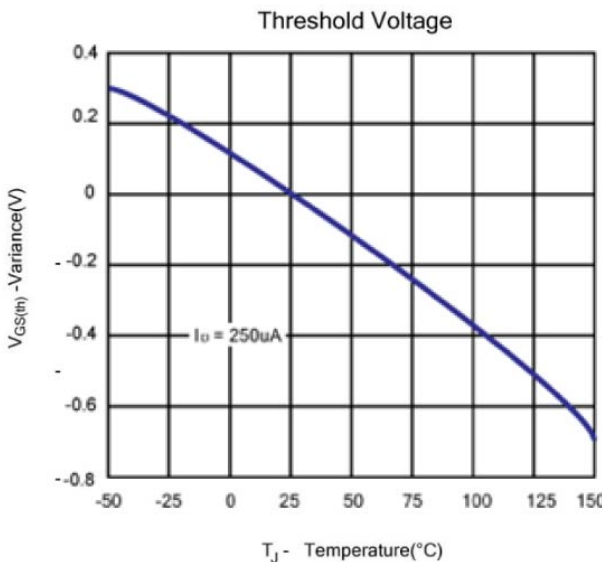
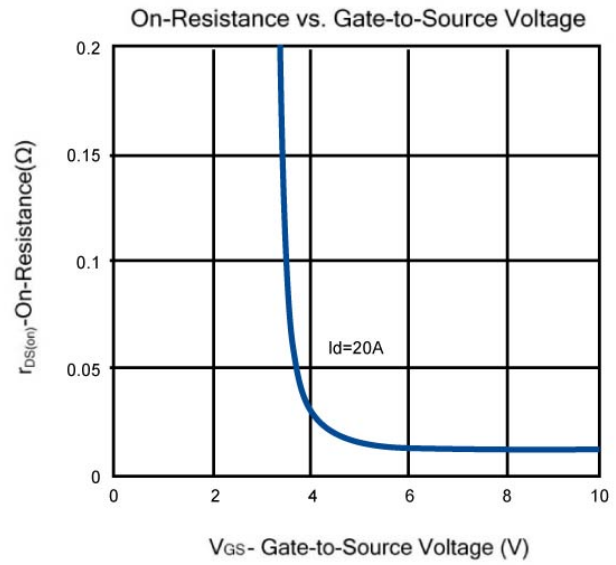
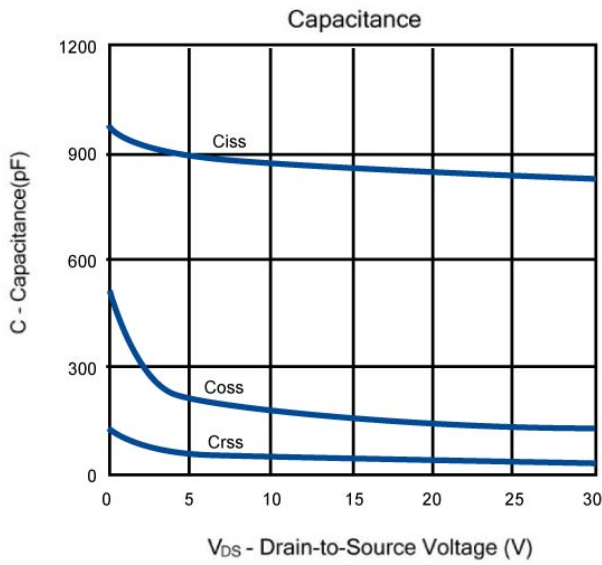
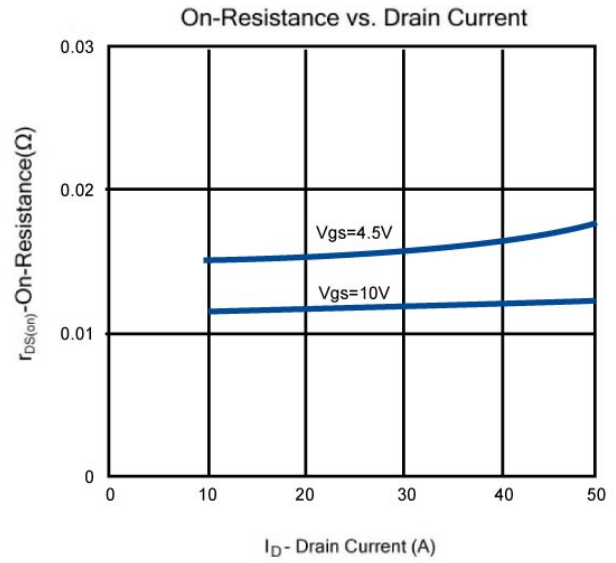
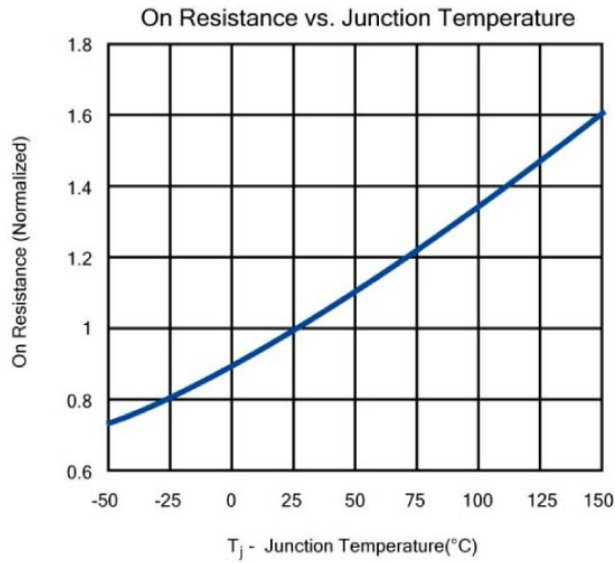
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =20A		11.5	14	mΩ
		V _{GS} =4.5V, I _D =20A		15	21	
V _{SD}	Diode Forward Voltage *	I _{SD} =20A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DD} =24V, V _{GS} =10V, I _D =20A		20		nC
Q _g	Total Gate Charge			11.4		
Q _{gs}	Gate-Source Charge	V _{DD} =24V, V _{GS} =5V, I _D =20A		4.5		
Q _{gd}	Gate-Drain Charge			5.3		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		1.7		Ω
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		832		pF
C _{oss}	Output Capacitance			133		
C _{rss}	Reverse Transfer Capacitance			41		
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, I _D =10A, V _{GS} =5V, R _G =4.7Ω		22		ns
t _r	Turn-On Rise Time			31		
t _{d(off)}	Turn-Off Delay Time			29		
t _f	Turn-Off Fall Time			7		

Notes: a. pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

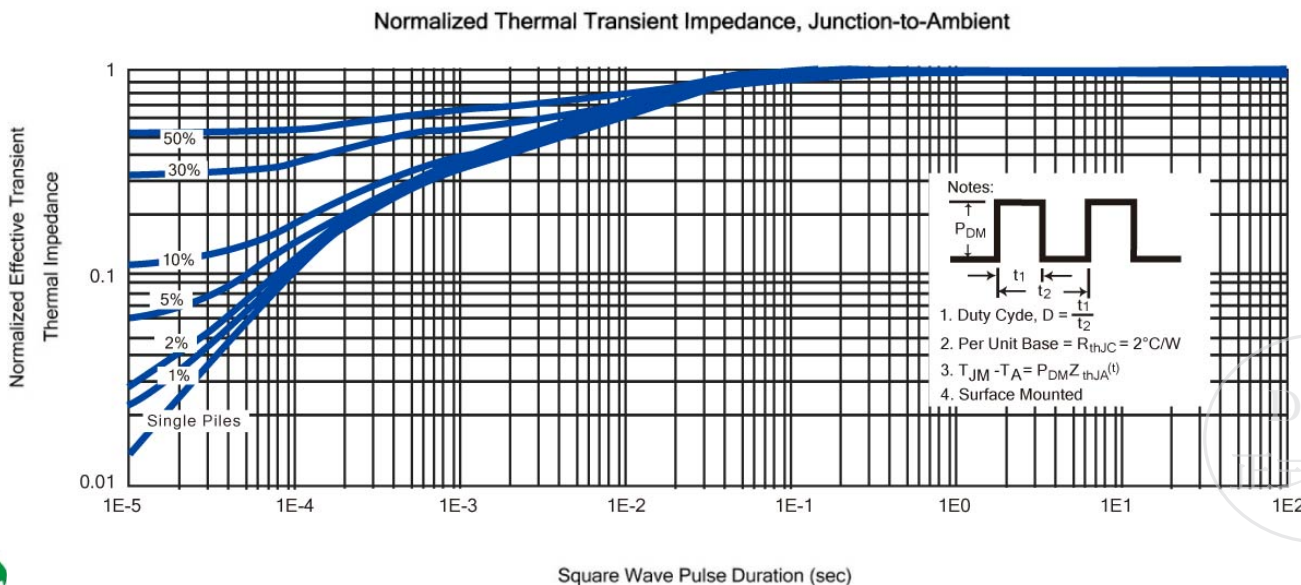
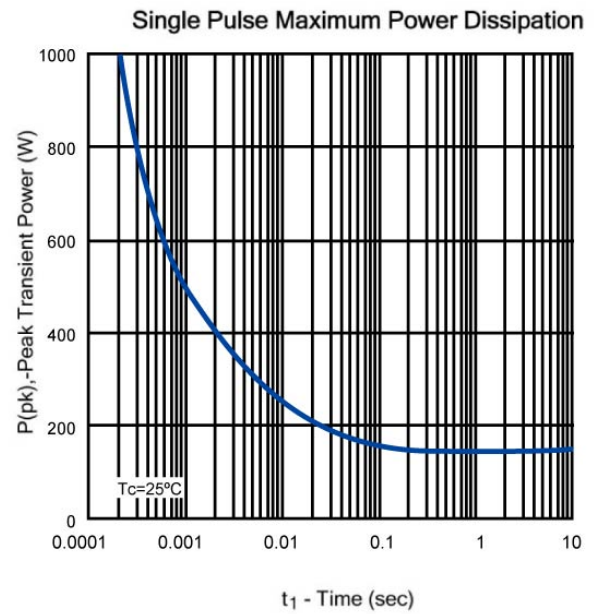
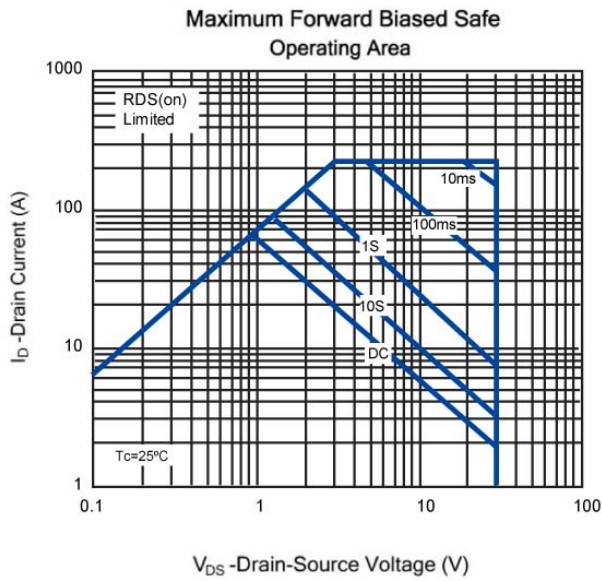
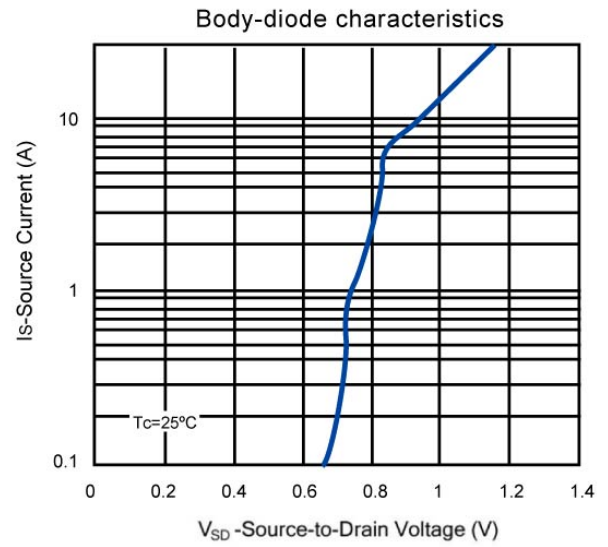
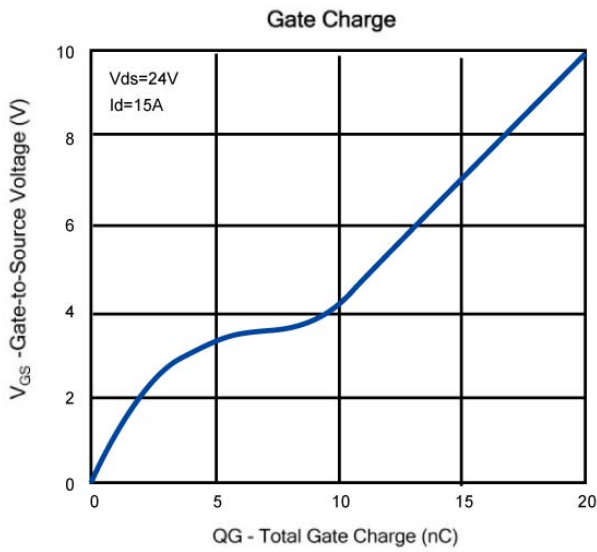
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



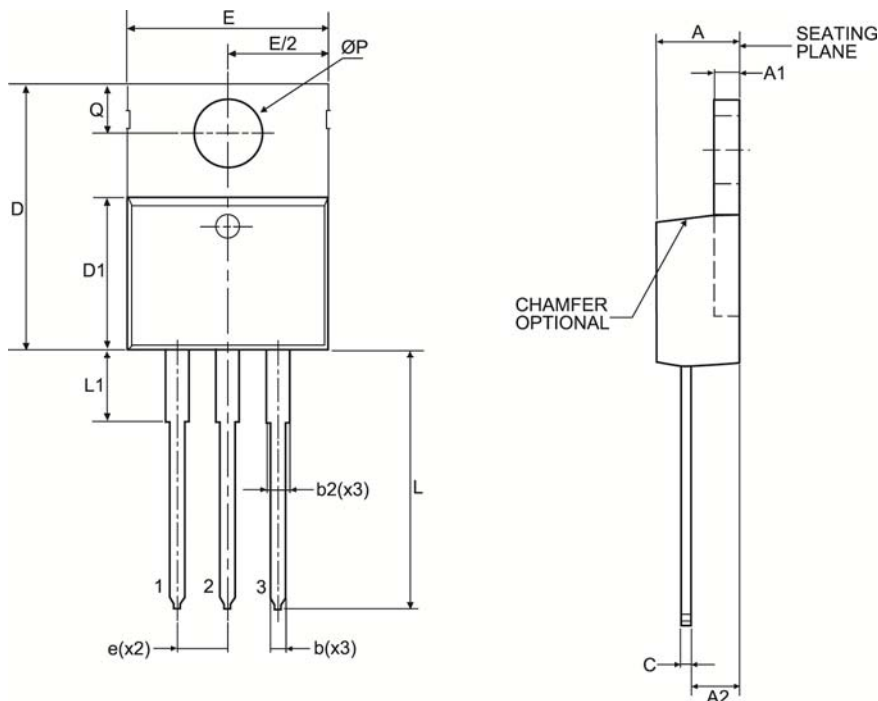
Typical Characteristics (T_J =25°C Noted)



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TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20

