N- and P-Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4566 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 34m\Omega @ V_{GS}=10V$ (N-Ch)
- $R_{DS(ON)} \leqq 42m\Omega @ V_{GS}=4.5V$ (N-Ch)
- $R_{DS(ON)} \leqq 66m\Omega @ V_{GS}=-10V$ (P-Ch)
- $R_{DS(ON)} \leqq 86m\Omega @ V_{GS}=-4.5V$ (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

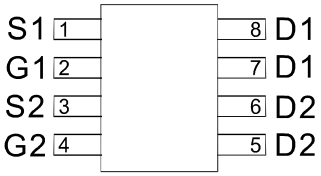
APPLICATIONS

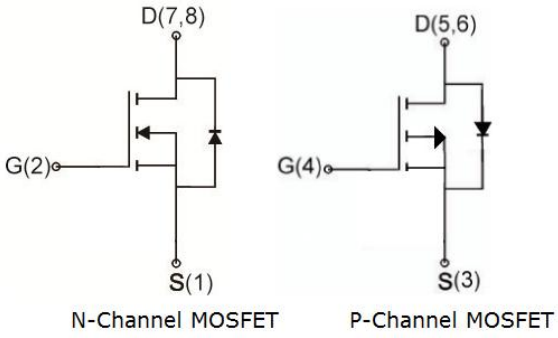
- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

PIN CONFIGURATION

(SOP-8)

Top View





N-Channel MOSFET P-Channel MOSFET

Ordering Information: ME4566 (Pb-free)

ME4566-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A=25℃	I_D	6.1	-4.4	A
	T_A=70℃		4.9	-3.5	
Pulsed Drain Current		I_{DM}	24	-17	
Maximum Power Dissipation	T_A=25℃	P_D	2	2	W
	T_A=70℃		1.3	1.3	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150		℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	62.5	62.5	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (T_j=25℃ Unless Otherwise Specified)

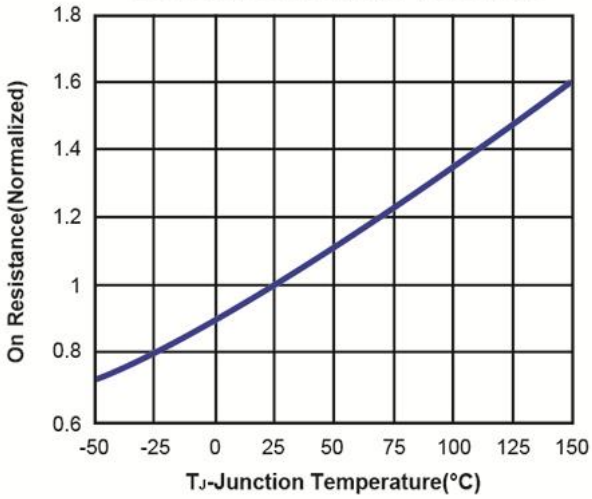
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA V_{GS}=0V, I_D=-250μA	N-Ch P-Ch	60 -60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA V_{DS}=V_{GS}, I_D=-250μA	N-Ch P-Ch	1 -1		2.5 -2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V V_{DS}=0V, V_{GS}=±20V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V V_{DS}=-60V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 4A V_{GS}=-10V, I_D= -2A	N-Ch P-Ch		28 55	34 66	mΩ
		V_{GS}=4.5V, I_D= 2A V_{GS}=-4.5V, I_D= -1A	N-Ch P-Ch		32 66	42 86	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V I_S=-1.7A, V_{GS}=0V	N-Ch P-Ch		0.74 -0.78	1.1 -1.1	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=30V, V_{GS}=10V, I_D=4A P-Channel V_{DS}=-30V, V_{GS}=-10V, I_D=-2A	N-Ch P-Ch		21.4 23.2		nC
Qg	Total Gate Charge	N-Channell V_{DS}=30V, V_{GS}= 5V, I_D=4A P-Channel V_{DS}=-30V, V_{GS}=-4.5V,I_D=-2A	N-Ch P-Ch		13.2 11.3		
Qgs	Gate-Source Charge		N-Ch P-Ch		3.1 4.7		
Qgd	Gate-Drain Charge		N-Ch P-Ch		4.9 4.5		
Ciss	Input Capacitance	N-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz P-Channel V_{DS}=-15V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		636 725		pF
Coss	Output Capacitance		N-Ch P-Ch		90 73		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		54 54		
$t_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD}=30V, R_L =30Ω I_D=1A, V_{GS}=10V, R_G=1Ω P-Channel V_{DD}=-30V, R_L =30Ω I_D=-1A, V_{GS}=-10V,R_G=3Ω	N-Ch P-Ch		11.2 30.2		ns
tr	Turn-On Rise Time		N-Ch P-Ch		11 8.6		
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		24.9 56.2		
tf	Turn-Off Fall Time		N-Ch P-Ch		3.2 6.6		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

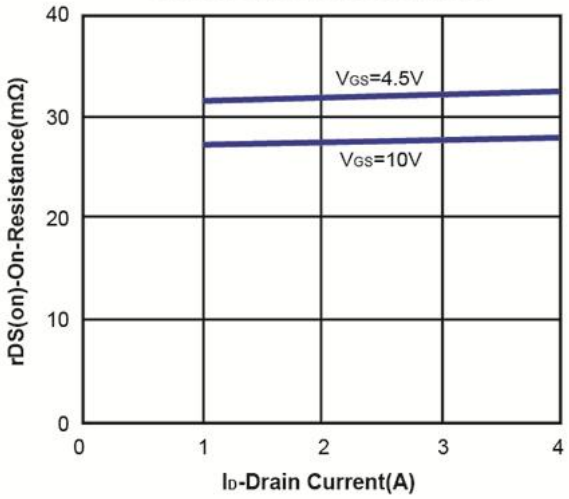
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

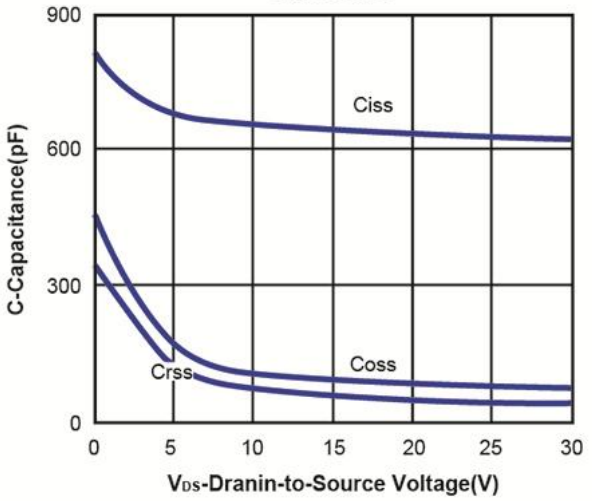
On Resistance vs. Junction Temperature



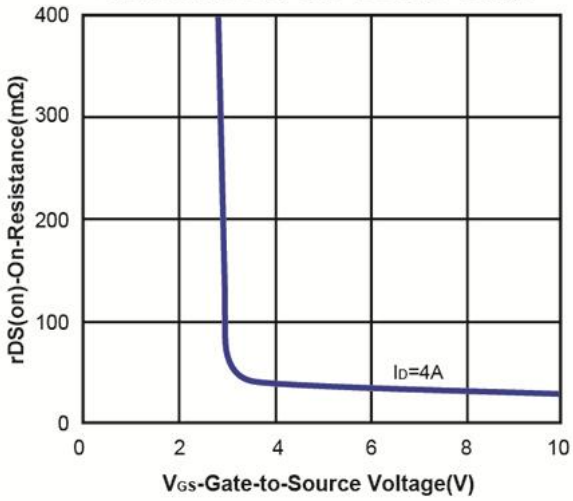
On Resistance vs. Drain Current



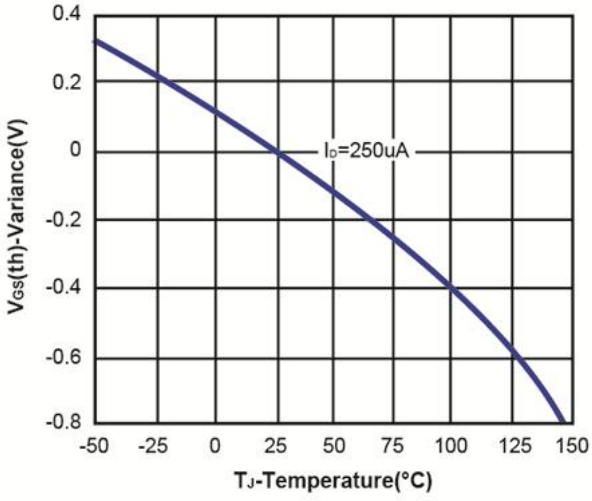
Capacitance



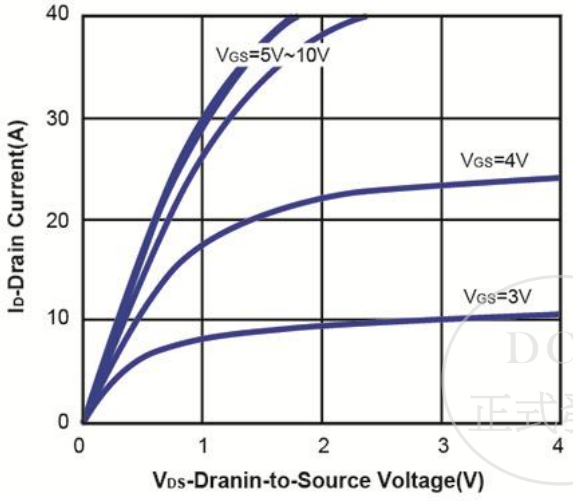
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



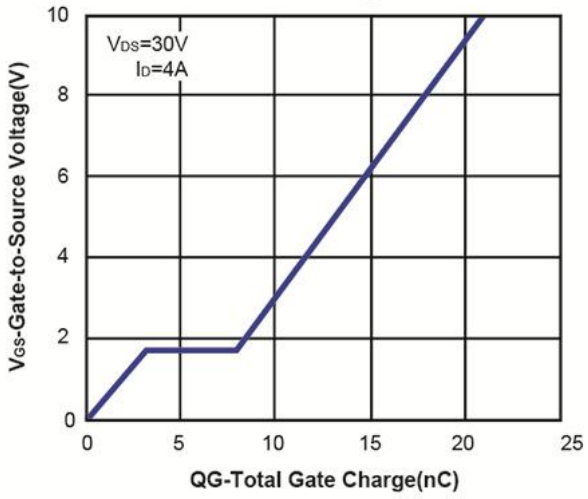
On-Region Characteristics



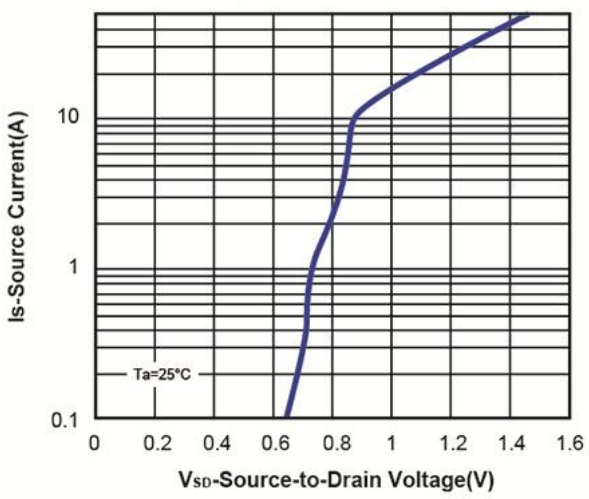
N- and P-Channel 60-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

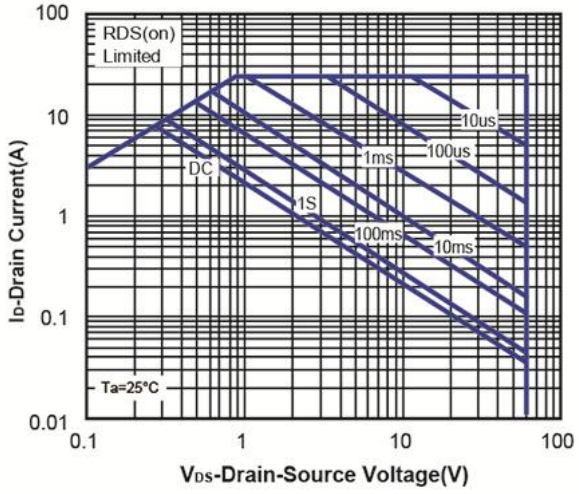
Gate Charge



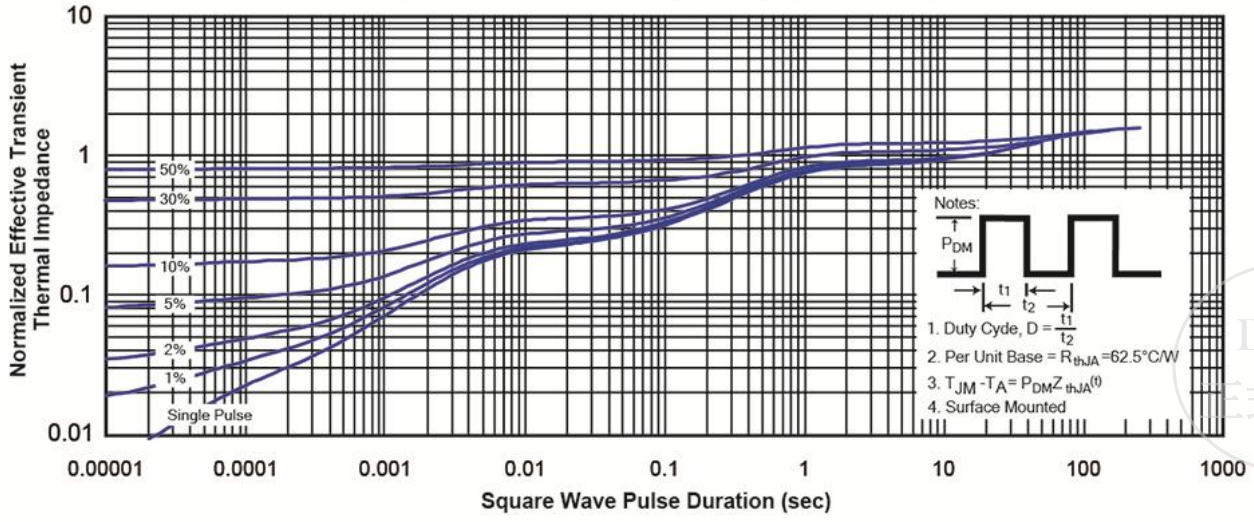
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



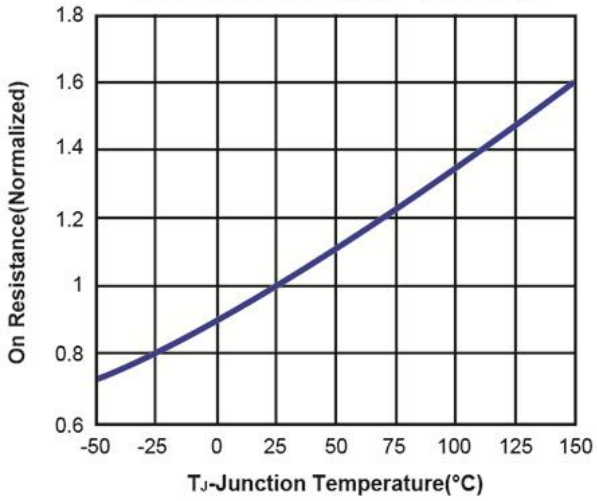
Normalized Thermal Transient Impedance, Junction-to-Ambient



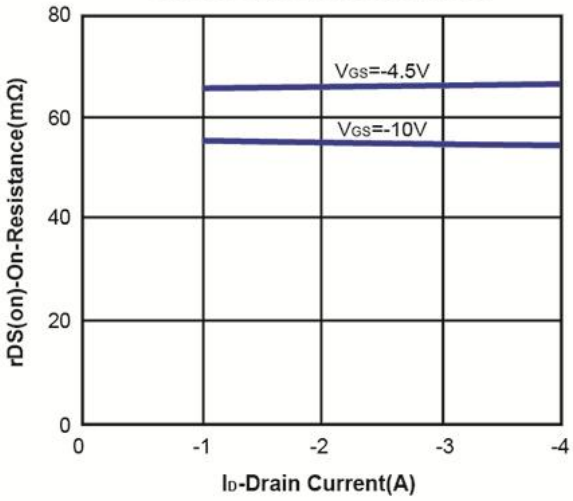
N- and P-Channel 60-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

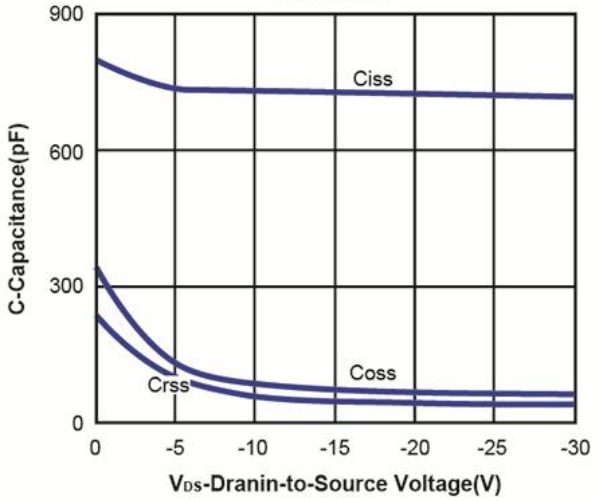
On Resistance vs. Junction Temperature



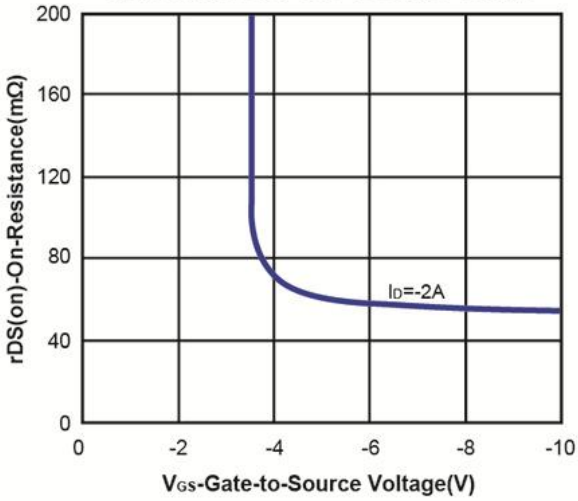
On Resistance vs. Drain Current



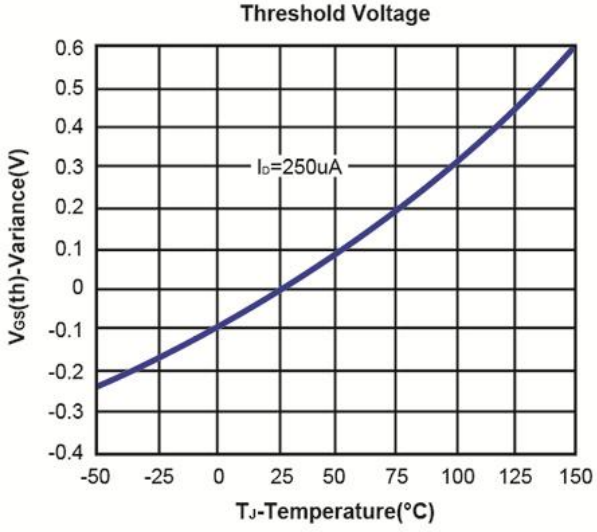
Capacitance



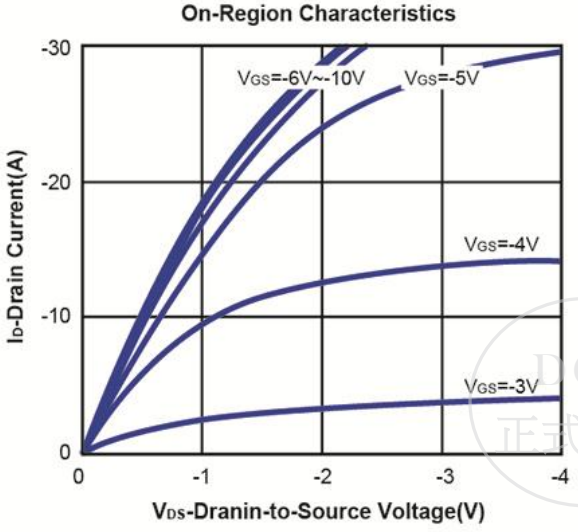
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



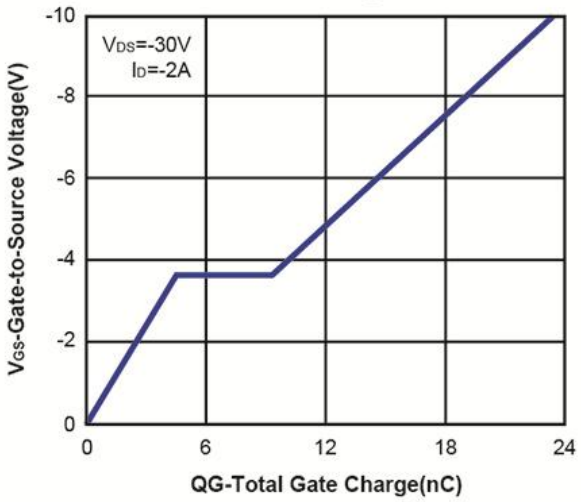
On-Region Characteristics



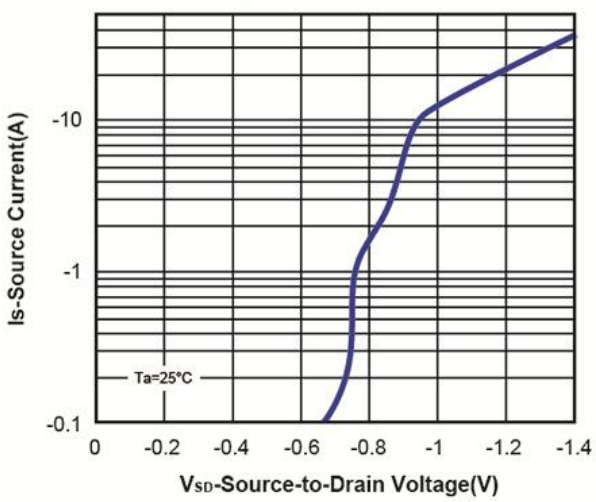
N- and P-Channel 60-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

Gate Charge



Body-diode characteristics



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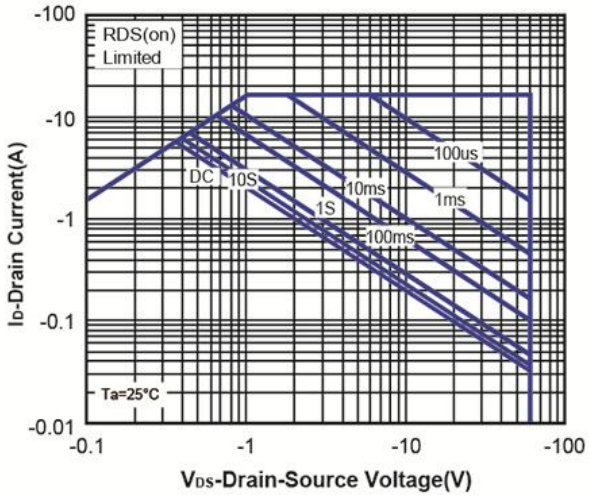
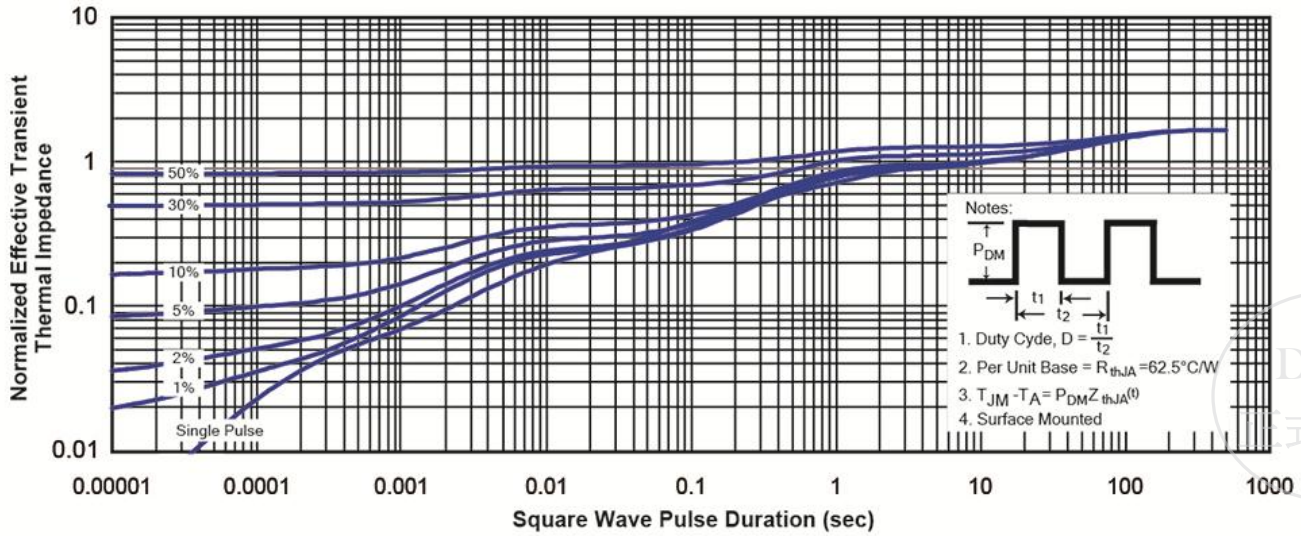
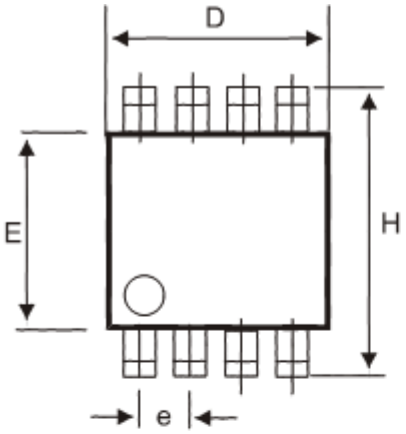
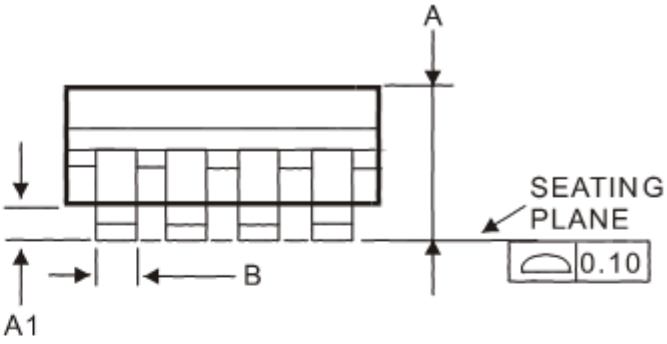


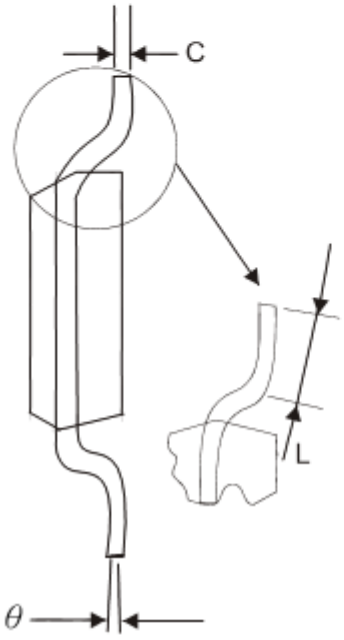
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°