ME25N10F/ME25N10F-G

N- Channel 100V (D-S) MOSFET

GENERAL DESCRIPTION

The ME25N10F is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leqq 85m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 105m\Omega @ V_{GS}=5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

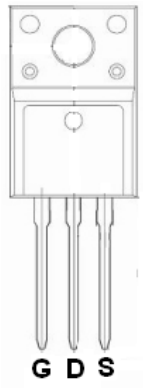
APPLICATIONS

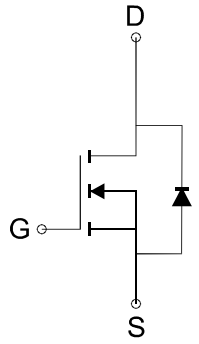
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-220F)

Top View





N-Channel MOSFET

Ordering Information: ME25N10F (Pb-free)

ME25N10F-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	Tc=25℃	I_D	11.7	A
	Tc=70℃		9.8	
Pulsed Drain Current		I_{DM}	46.9	A
Maximum Power Dissipation	Tc=25℃	P_D	23.4	W
	Tc=70℃		16.4	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 175	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	6.4	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

N- Channel 100V (D-S) MOSFET

Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 12A		70	85	mΩ
		V_{GS}=5V, I_D= 12A		80	105	
V_{SD}	Diode Forward Voltage	I_S=12A, V_{GS}=0V			1.3	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=80V, V_{GS}=10V, I_D=25A		28.6		nC
Qg	Total Gate Charge	V_{DS}=80V, V_{GS}=5V, I_D=25A		17		
Qgs	Gate-Source Charge			7.1		
Qgd	Gate-Drain Charge			10.1		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, F=1MHz		699		pF
Coss	Output Capacitance			108		
Crss	Reverse Transfer Capacitance			68		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.5		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=50V, R_L =50Ω V_{GEN}=5V, R_G=4.7Ω		19.2		ns
t_r	Turn-On Rise Time			13.6		
$t_{d(off)}$	Turn-Off Delay Time			35		
t_f	Turn-Off Fall Time			9.2		

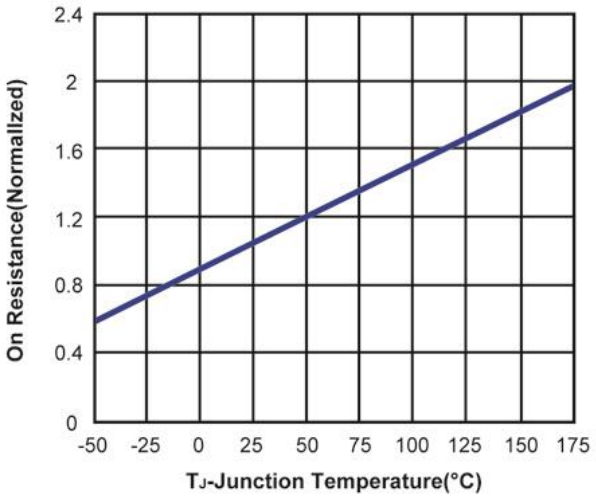
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

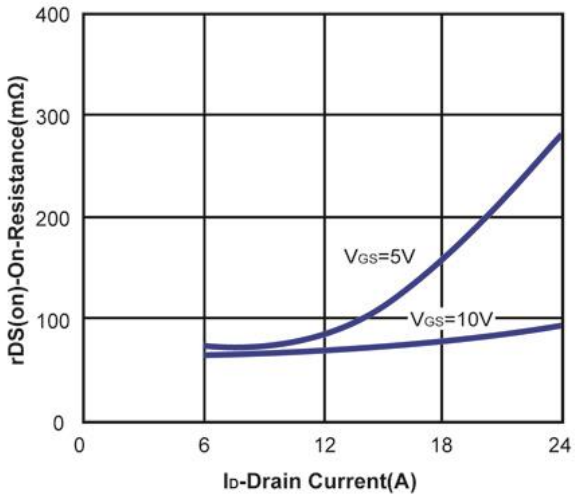
N- Channel 100V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

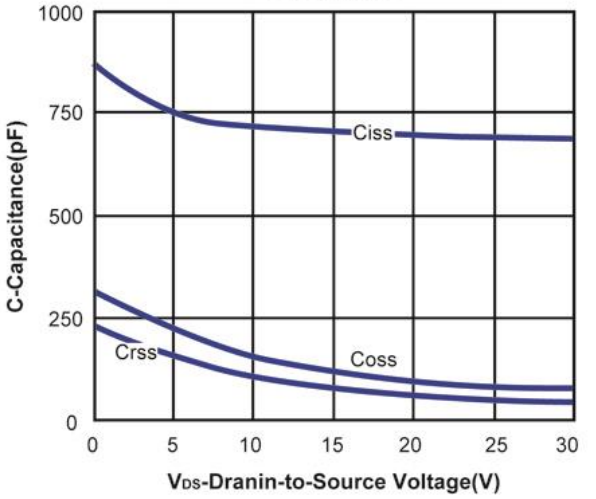
On Resistance vs. Junction Temperature



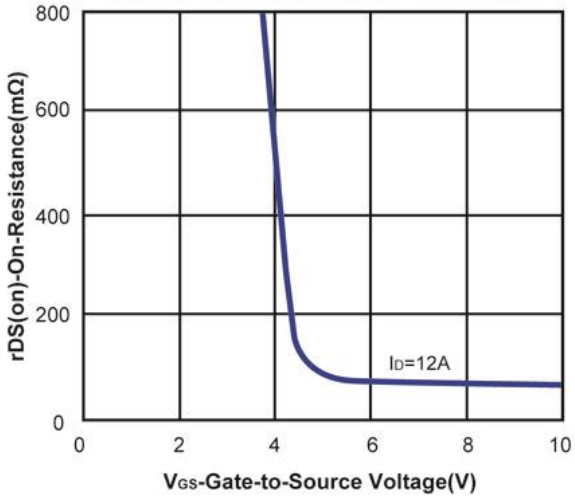
On Resistance vs. Drain Current



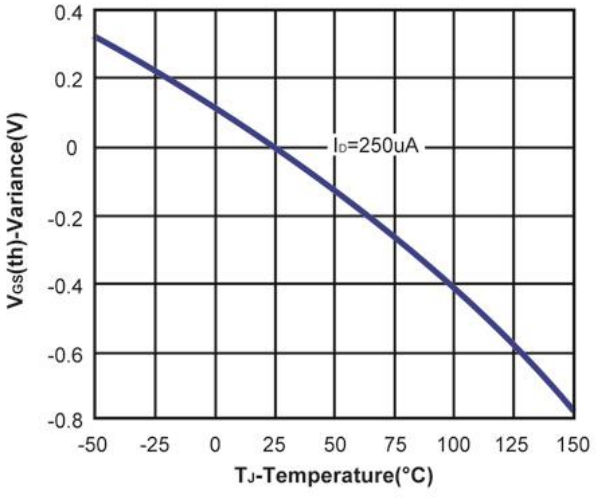
Capacitance



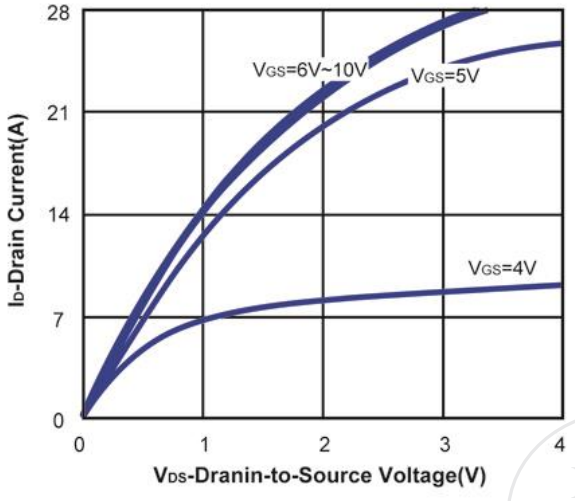
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



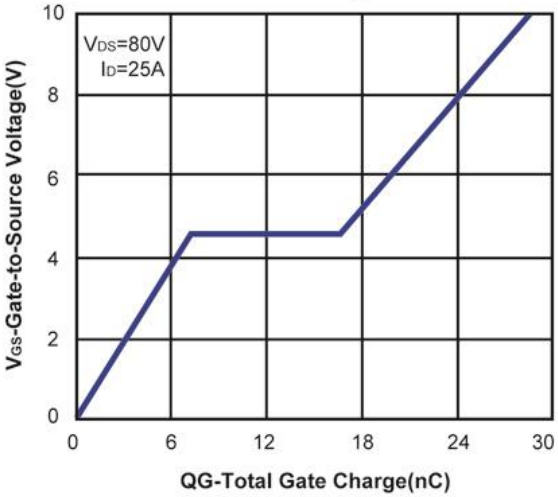
On-Region Characteristics



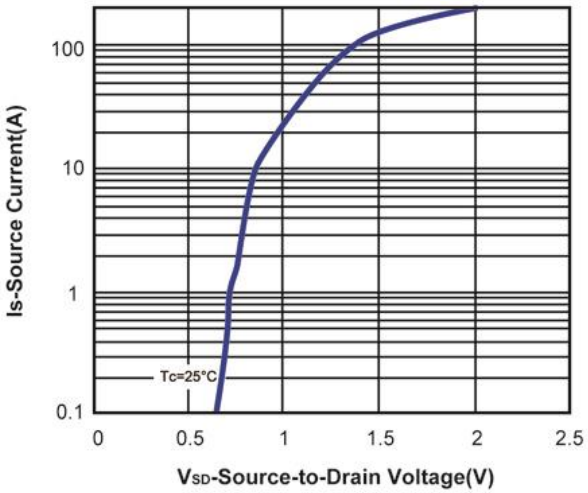
N- Channel 100V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

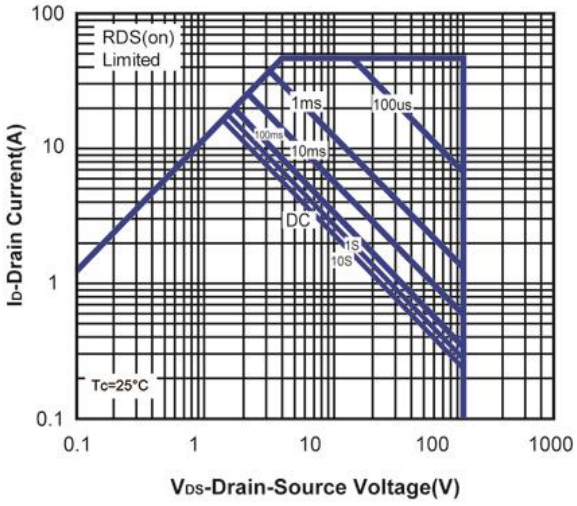
Gate Charge



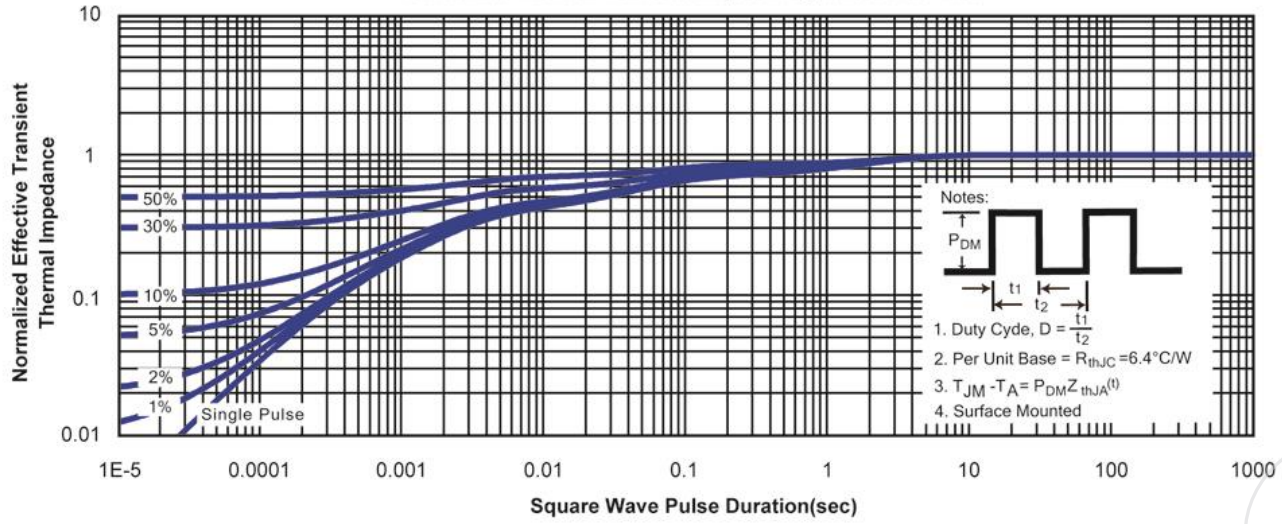
Body-diode characteristics



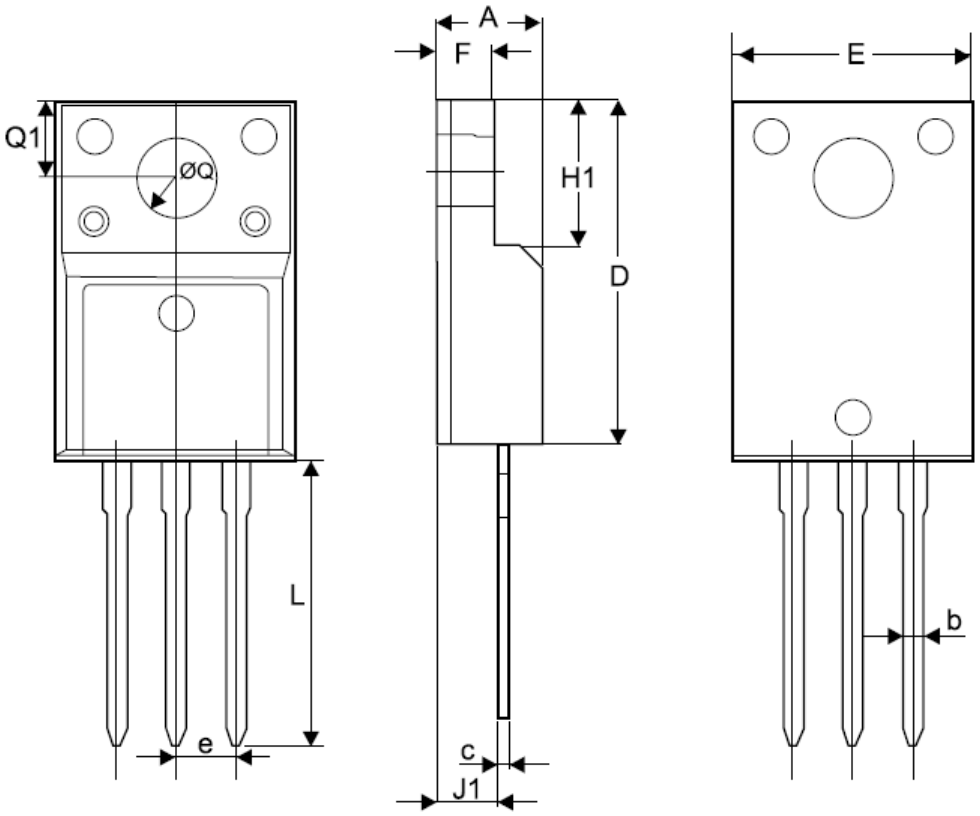
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-220F Package Outline



Symbol	MILLIMETERS(mm)	
	MIN	MAX
A	4.40	5.00
b	0.60	1.00
C	0.30	0.70
D	15.40	16.40
E	6.96	10.46
F	2.30	2.80
e	2.54 TYP	
H1	6.40	7.00
J1	2.45	3.05
L	12.28	13.68
Ø Q	2.92	3.38
Q1	3.05	3.55