

N-Channel 100V (D-S) MOSFET
GENERAL DESCRIPTION

The ME2514 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 166\text{m}\Omega @ V_{GS}=10\text{V}$
- $R_{DS(ON)} \leq 213\text{m}\Omega @ V_{GS}=4.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

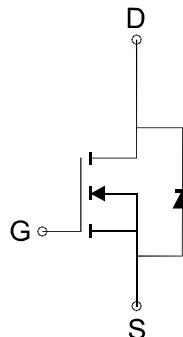
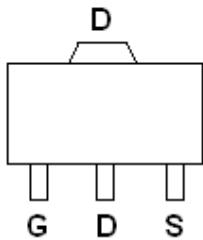
APPLICATIONS

- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(SOT-89)

Top View



N-Channel MOSFET

Ordering Information: ME2514 (Pb-free)

ME2514-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_D	2.2	A
	$T_A=70^\circ\text{C}$		1.7	
Pulsed Drain Current		I_{DM}	9	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.3	W
	$T_A=70^\circ\text{C}$		0.8	
Operating Junction Temperature		T_J	150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	100	$^\circ\text{C}/\text{W}$

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_c = 25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{BR(DSS)}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1.0		3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{dss}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V			1	μA
R _{Ds(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 3A		132	166	mΩ
		V _{GS} =4.5V, I _D =2.4A		148	213	
V _{SD}	Diode Forward Voltage	I _S =2.5A, V _{GS} =0V		0.8	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =10V, I _D =2.5A		19.2		nC
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =4.5V, I _D =2.5A		11.2		
Q _{gs}	Gate-Source Charge			3.4		
Q _{gd}	Gate-Drain Charge			6.1		
C _{iss}	Input capacitance	V _{DS} =15V, V _{GS} =0V, f=1.0MHz		531		pF
C _{oss}	Output Capacitance			71		
C _{rss}	Reverse Transfer Capacitance			42		
t _{d(on)}	Turn-On Delay Time	V _{DS} =50V, R _L =10Ω V _{GS} =10V, R _G =6Ω I _D =5A		12.5		ns
t _r	Turn-On Rise Time			6		
t _{d(off)}	Turn-Off Delay Time			32.4		
t _f	Turn-Off Fall Time			4.3		

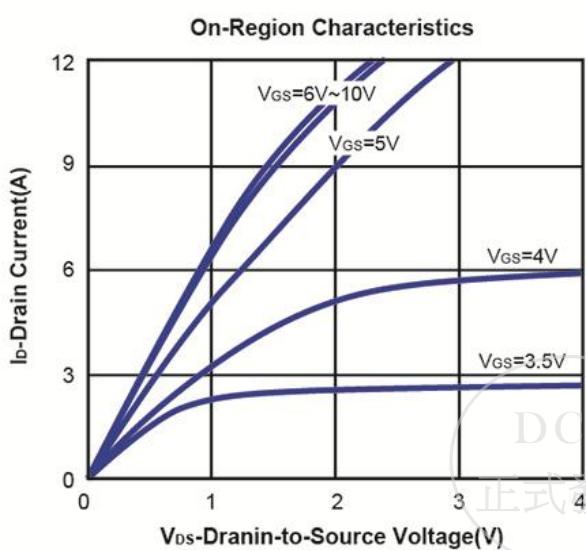
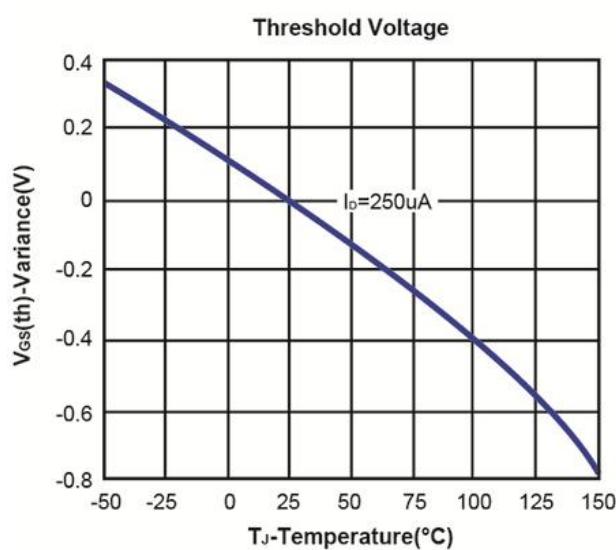
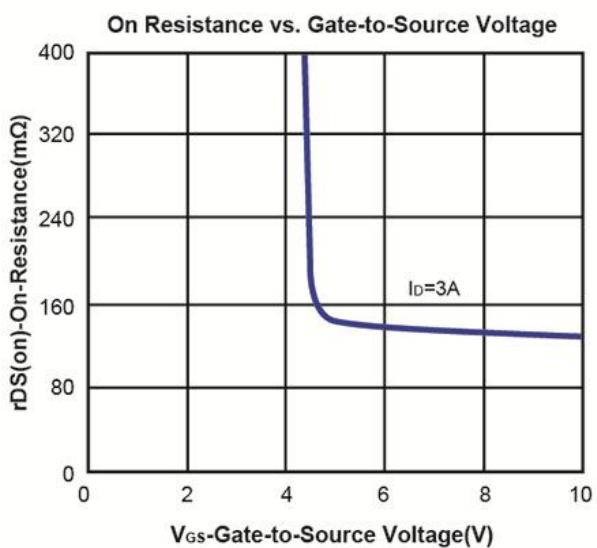
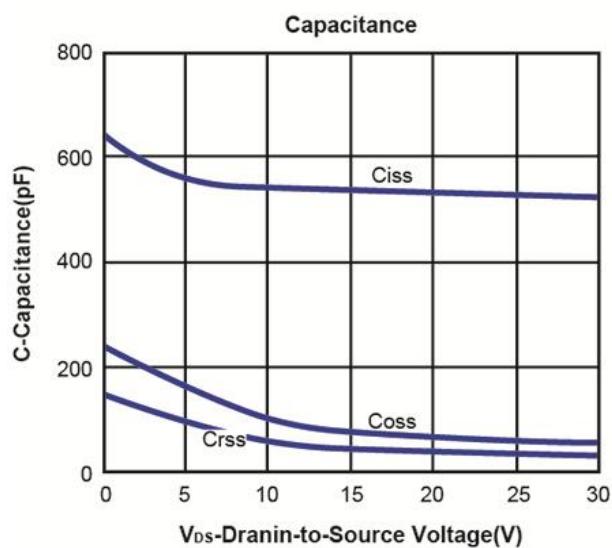
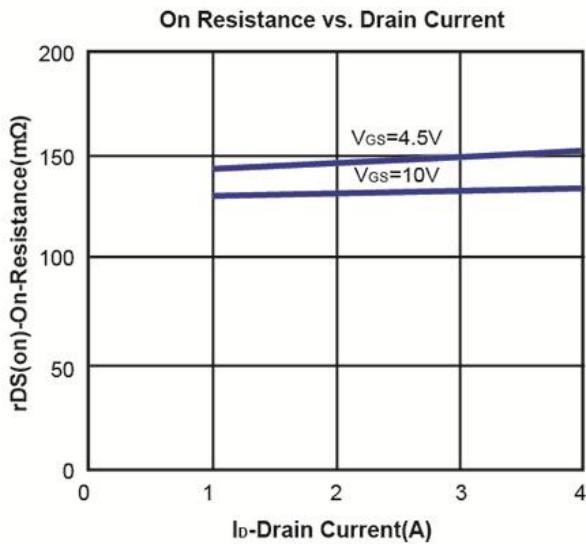
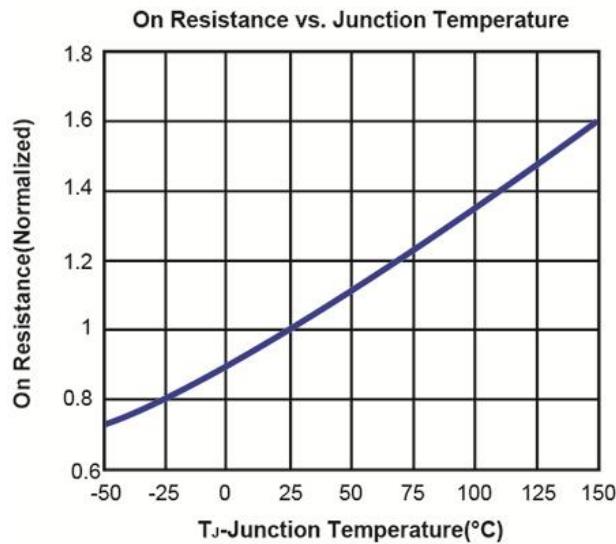
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



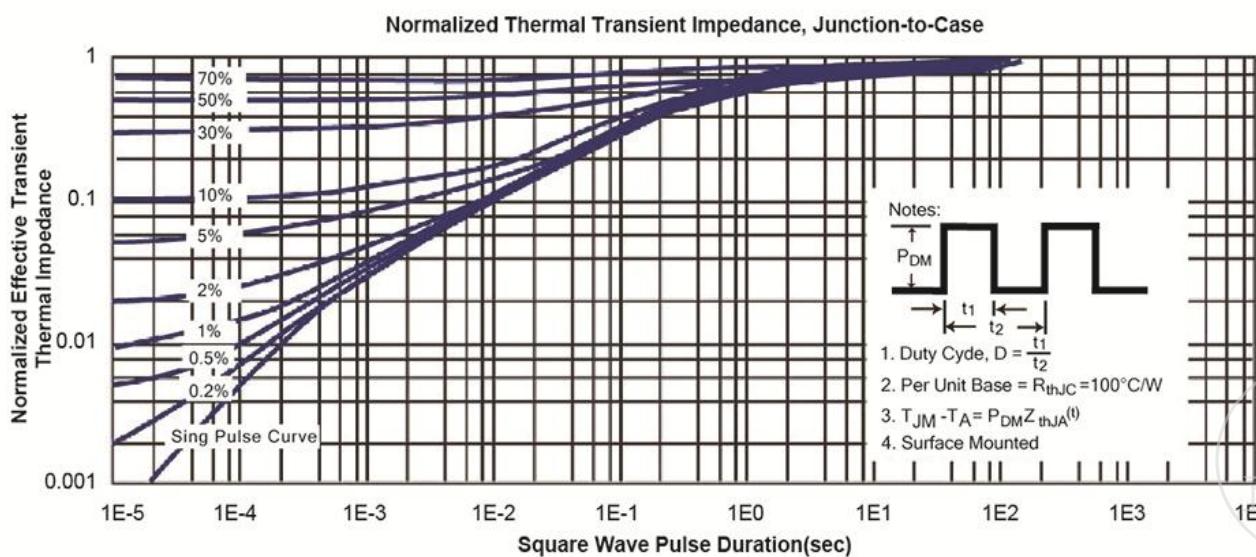
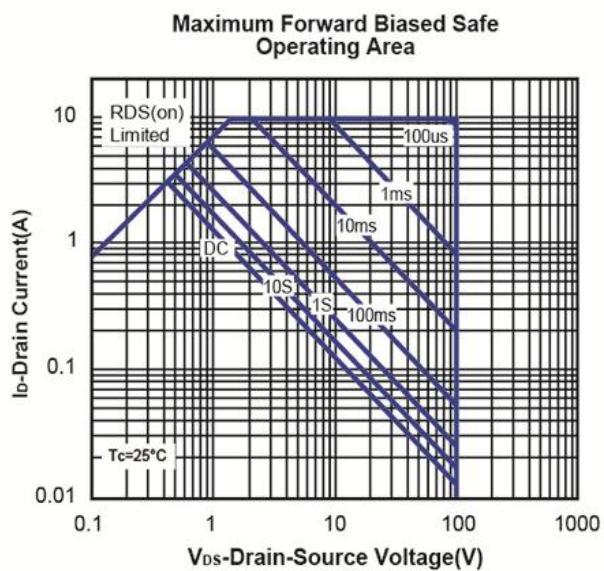
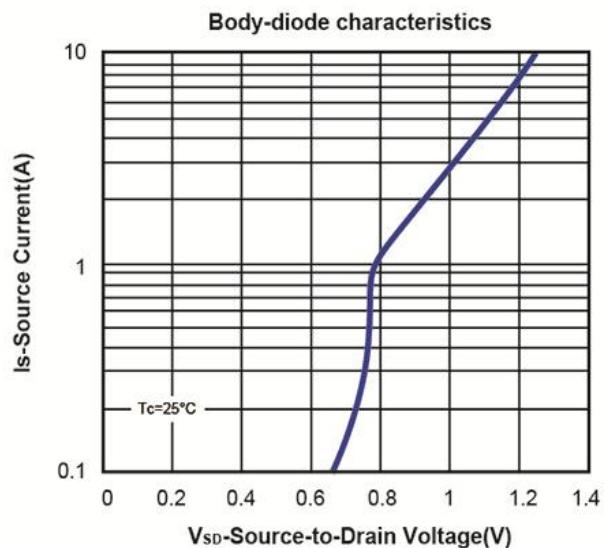
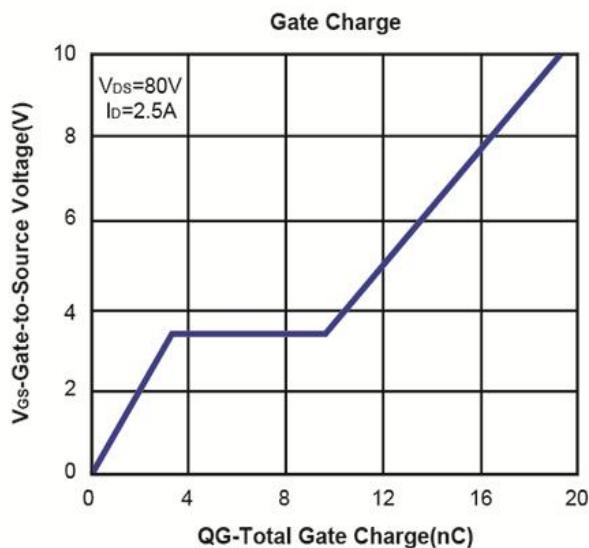
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Typical Characteristics (T_J =25°C Noted)

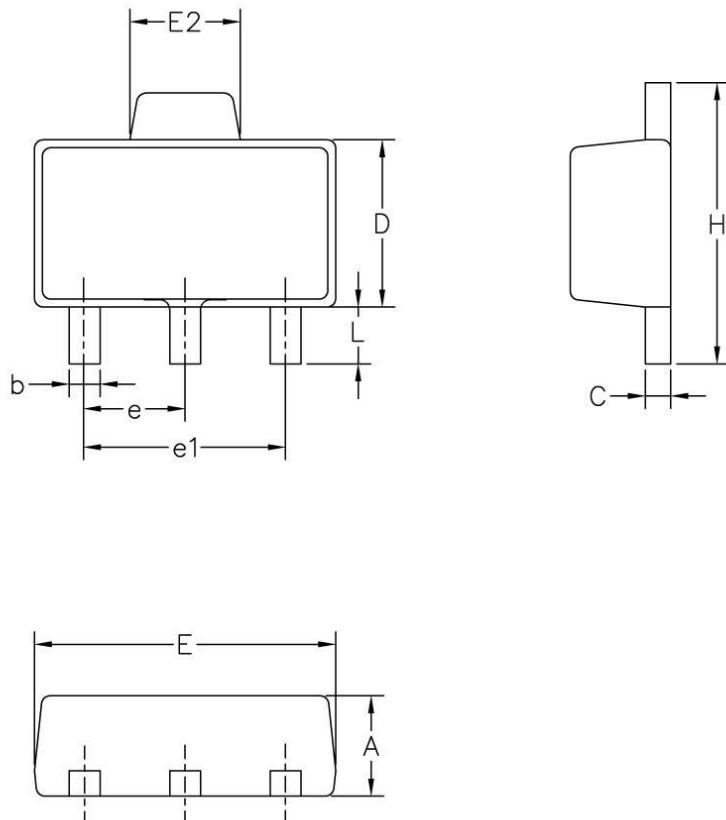


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Typical Characteristics (T_J = 25°C Noted)



SOT-89 Package Outline



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.41	1.59	0.056	0.063
B	0.43	0.50	0.017	0.020
C	0.37	0.39	0.0146	0.0154
E	4.41	4.59	0.174	0.181
E2	1.65	Ref	0.065	Ref
e	1.50 BSC		0.059 BSC	
e1	3.00	±0.03	0.118	±0.012
D	2.41	2.59	0.095	0.102
H	3.97	4.24	0.156	0.167
L	0.81	1.16	0.032	0.046

