ME2318S /ME2318S-G

N-Channel 40V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2318S-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦40mΩ@V_{GS}=10V
- $R_{DS(ON)}$ ≦65mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

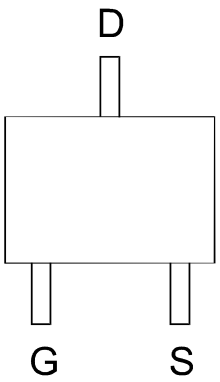
APPLICATIONS

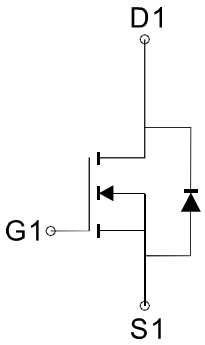
- Power Management in Note book
- Portable Equipment
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





N-Channel MOSFET

Ordering Information: ME2318S / ME2318S-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Tj=150℃)*	T_A=25℃	I_D	4	A
	T_A=70℃		3.2	
Pulsed Drain Current		I_{DM}	16	A
Maximum Power Dissipation*	T_A=25℃	P_D	1.04	W
	T_A=70℃		0.67	
Operating Junction & Storage Temperature Range		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	120	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V_{DS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0		3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D= 4.0A		32	40	mΩ
		V_{GS}=4.5V, I_D= 3.5A		50	65	
V_{SD}	Diode Forward Voltage	I_S=1A		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=10V, I_D=4A		16		nC
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=4.5V, I_D=4A		8.2		
Qgs	Gate-Source Charge			3.6		
Qgd	Gate-Drain Charge			3.9		
Ciss	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1.0MHz		547		pF
Coss	Output Capacitance			52		
Crss	Reverse Transfer Capacitance			43		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=20V, R_L =20Ω I_D=1A, V_{GS}=10V R_G=1Ω		12		ns
t_r	Turn-On Rise Time			12		
$t_{d(off)}$	Turn-Off Delay Time			37		
t_f	Turn-Off Fall Time			4		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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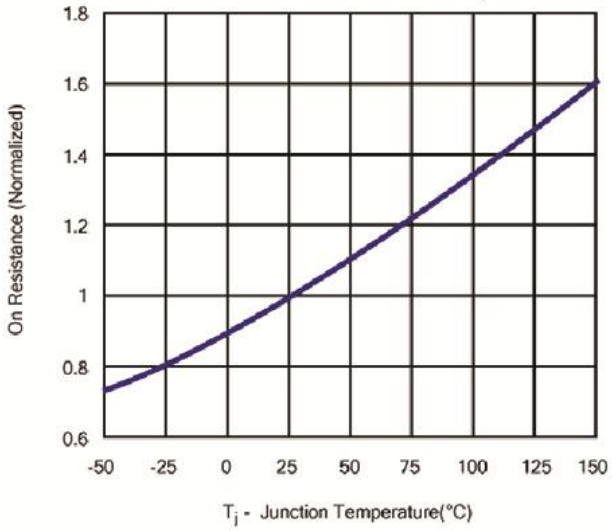
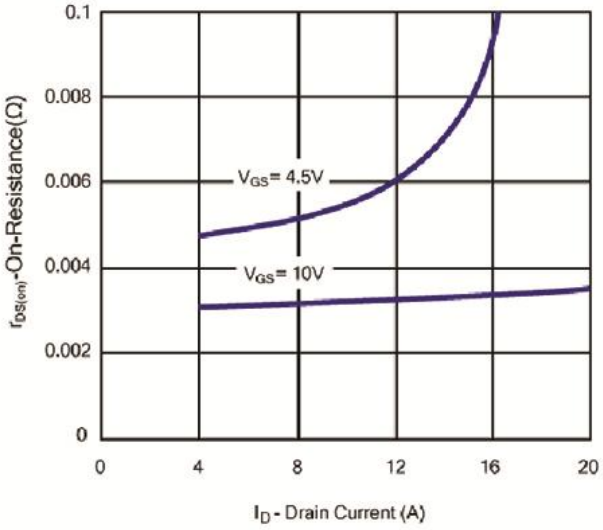
Typical Characteristics (T_J =25℃ Noted)

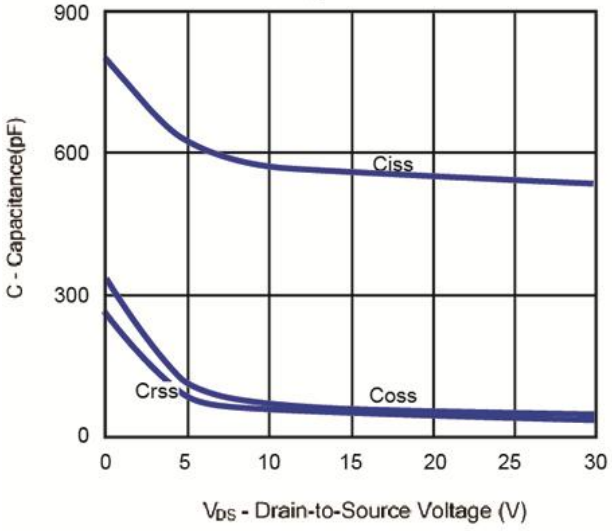
On Resistance vs. Junction Temperature



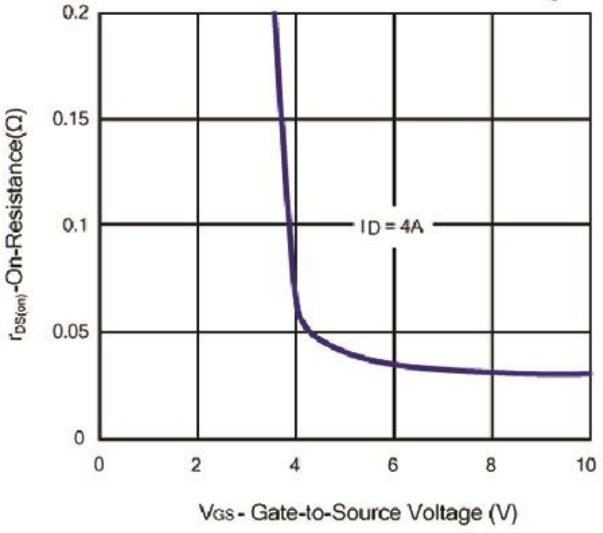
On-Resistance vs. Drain Current



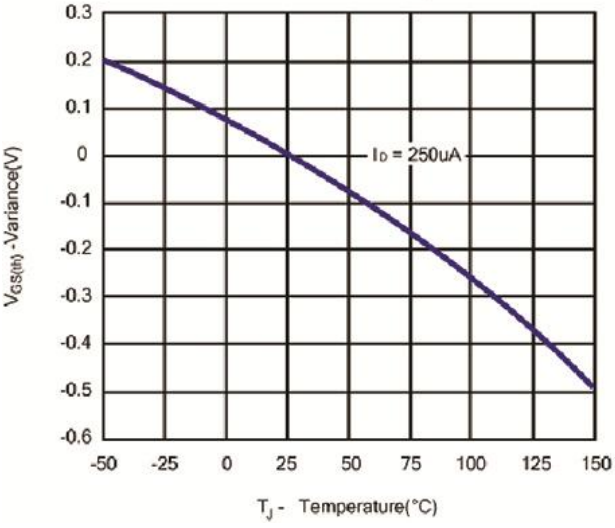
Capacitance



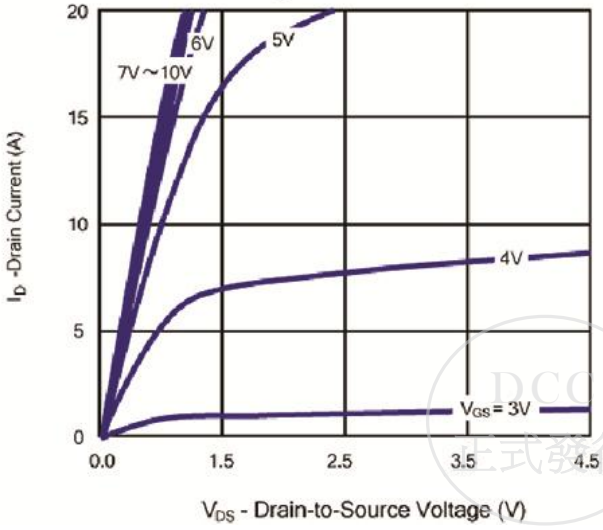
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



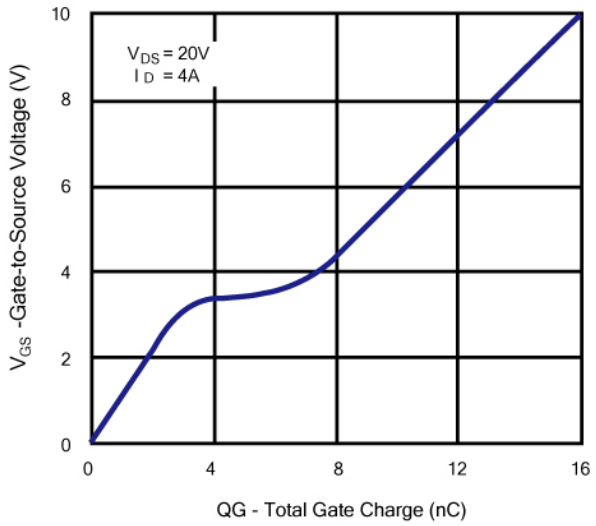
On-Region Characteristics



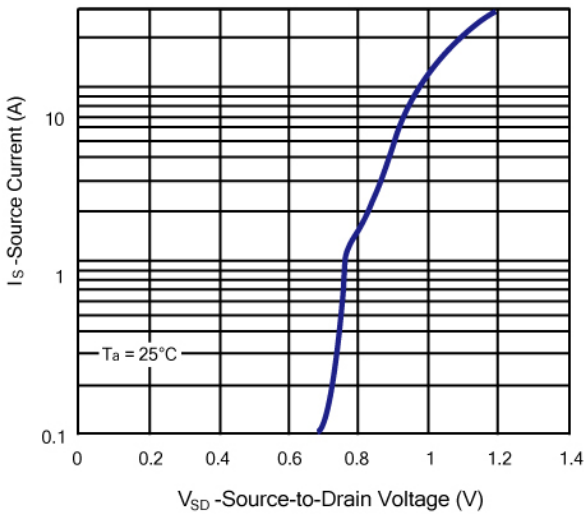
N-Channel 40V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

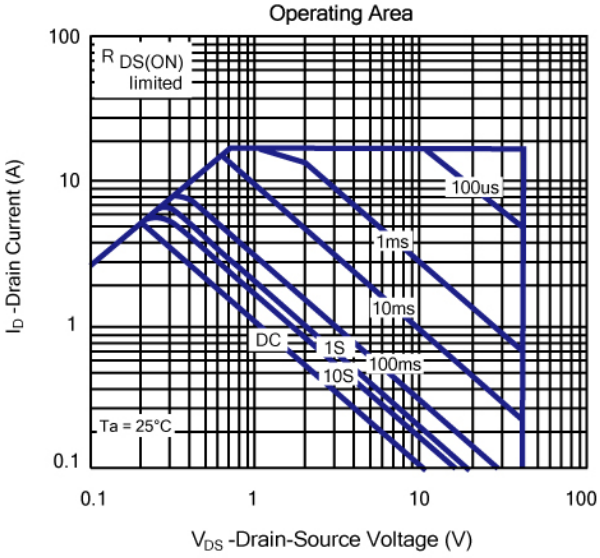
Gate Charge



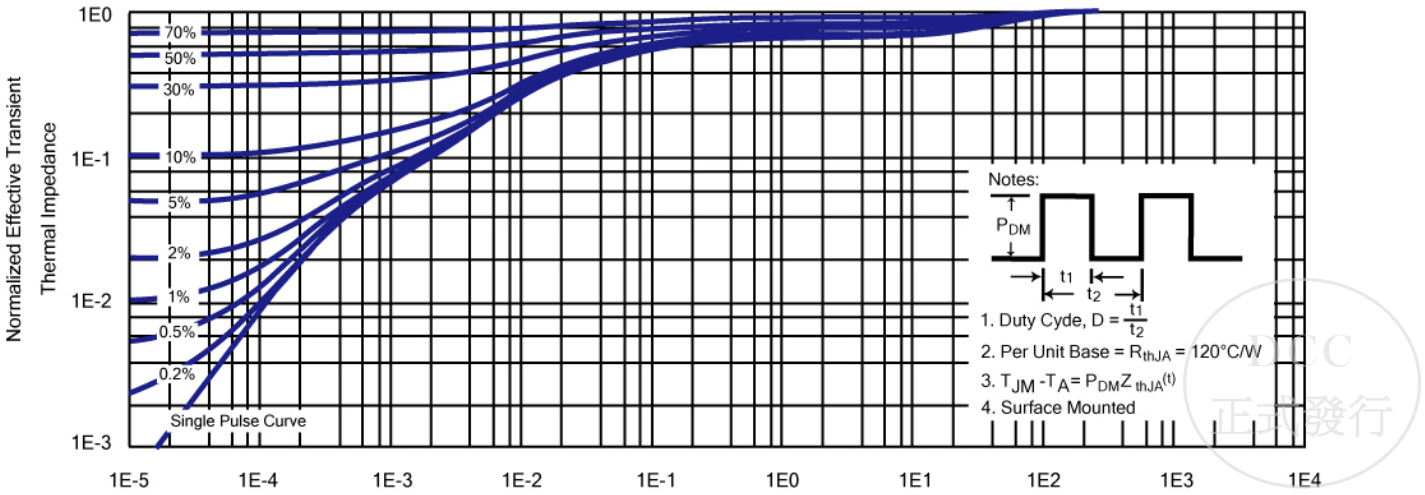
Source to Drain Diode Forward Voltage



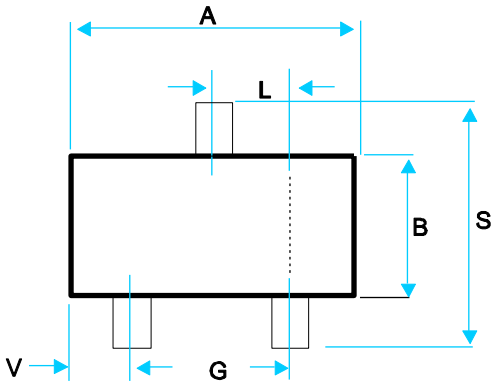
Maximum Forward Biased Safe Operating Area

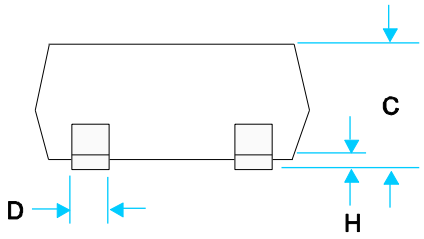


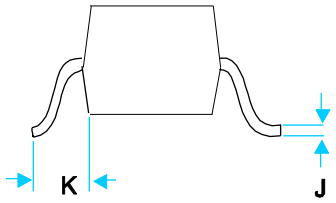
Normalized Thermal Transient Impedance, Junction-to-Ambient



大 SOT-23 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	2.80	3.1
B	1.20	1.7
C	0.89	1.25
D	0.37	0.50
G	1.78	2.04
H	0.013	0.15
J	0.085	0.2
K	0.45	0.7
L	0.89	1.02
S	2.10	3
V	0.45	0.60