N-Channel 20-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2312-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 33m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 40m\Omega @ V_{GS}=2.5V$
- $R_{DS(ON)} \leqq 51m\Omega @ V_{GS}=1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

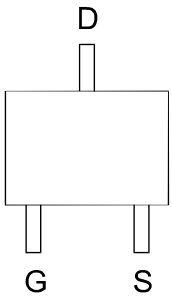
APPLICATIONS

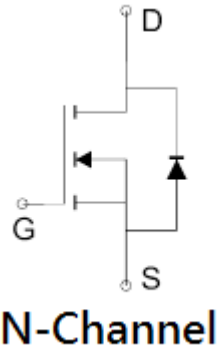
- Power Management in Note book
- Portable Equipment
- Load Switch
- DSC

PIN CONFIGURATION

(SOT-23)

Top View





Ordering Information: ME2312 /ME2312-G(Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	5.1	A
	T_A=70℃		4.1	
Pulsed Drain Current		I_{DM}	20.5	
Maximum Power Dissipation	T_A=25℃	P_D	1.3	W
	T_A=70℃		0.8	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Maximum Junction-to-Ambient		R_{thJA}	90	℃/W

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Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4	0.6	1	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS}=±8V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=4.5V, I_D= 5.0A		23	33	mΩ
		V_{GS}=2.5V, I_D= 4.5A		27	40	
		V_{GS}=1.8V, I_D= 4.0A		34	51	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		644		pF
Coss	Output Capacitance			85.7		
Crss	Reverse Transfer Capacitance			22.5		
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=5.0A		11		nC
Qgs	Gate-Source Charge			2.3		
Qgd	Gate-Drain Charge			2.6		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=10V, R_L =10Ω V_{GS}=4.5V, R_G=6Ω I_D=1.0A		9		ns
t_r	Rise Time			17		
$t_{d(off)}$	Turn-Off Delay Time			46		
t_f	Fall Time			2.7		

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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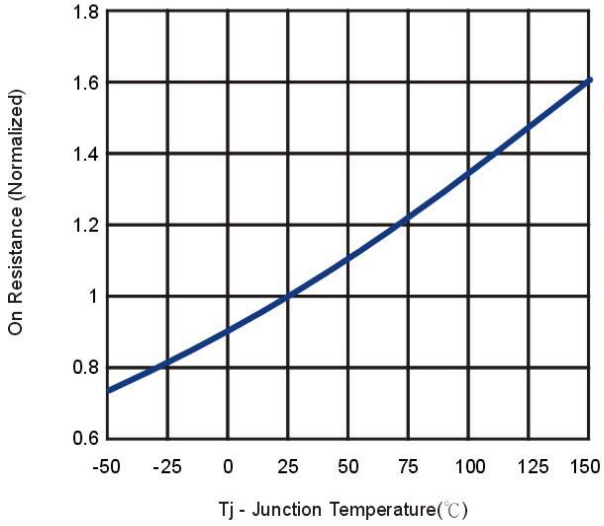
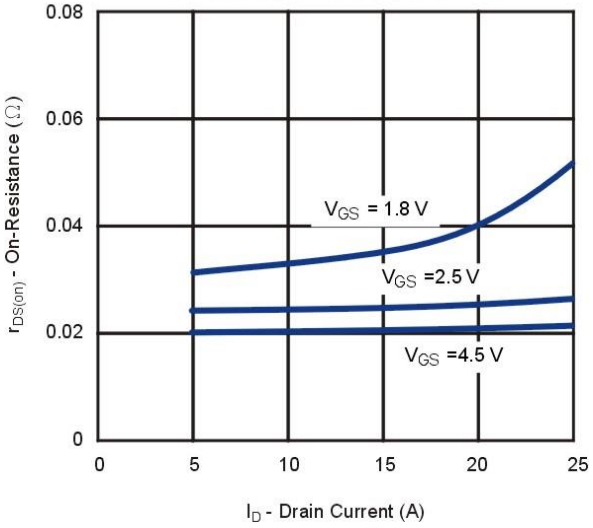
Typical Characteristics (T_J =25℃ Noted)

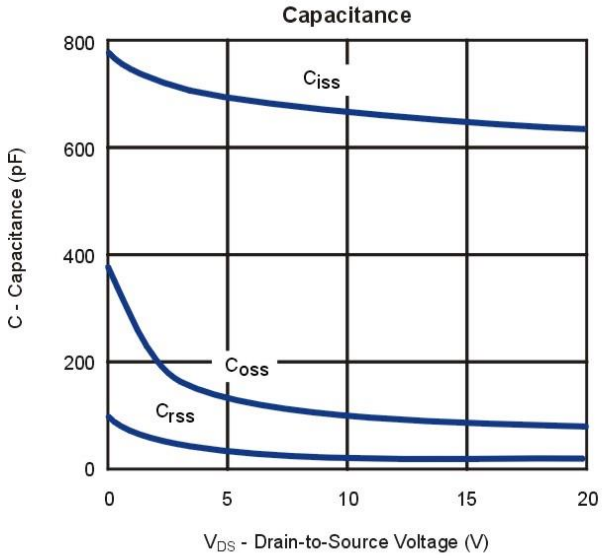
On Resistance vs. Junction Temperature



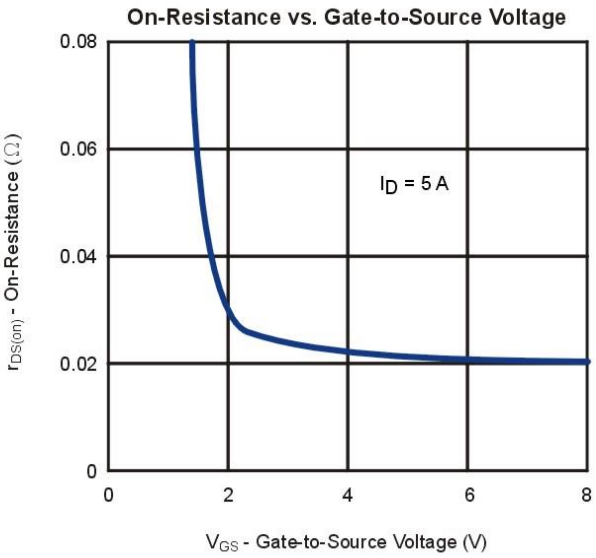
On-Resistance vs. Drain Current



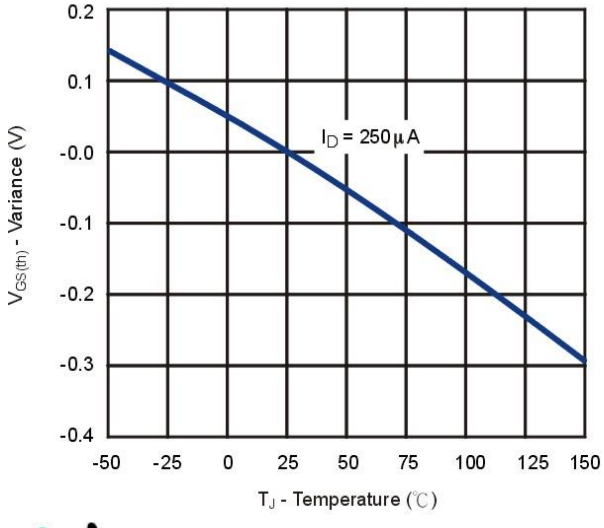
Capacitance



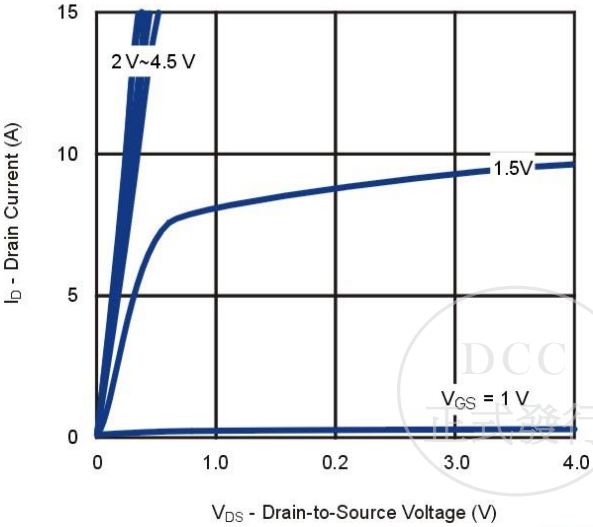
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



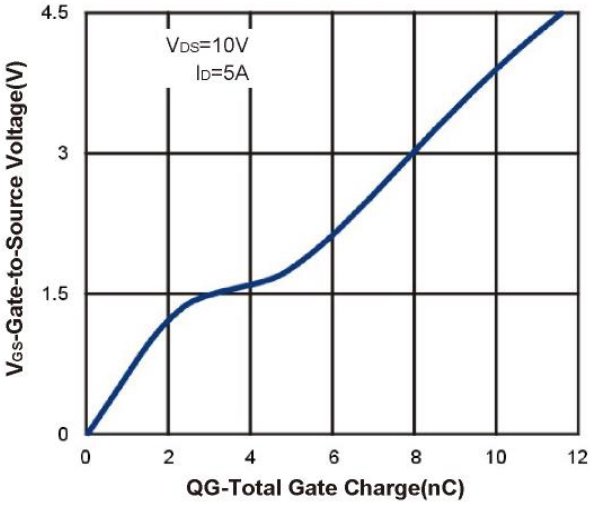
On-Region Characteristics



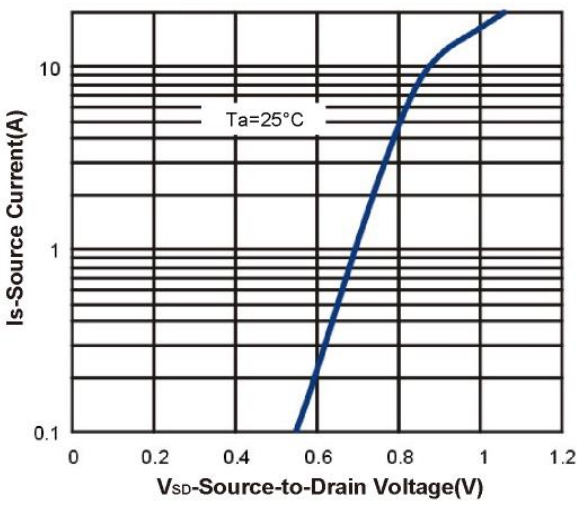
N-Channel 20-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

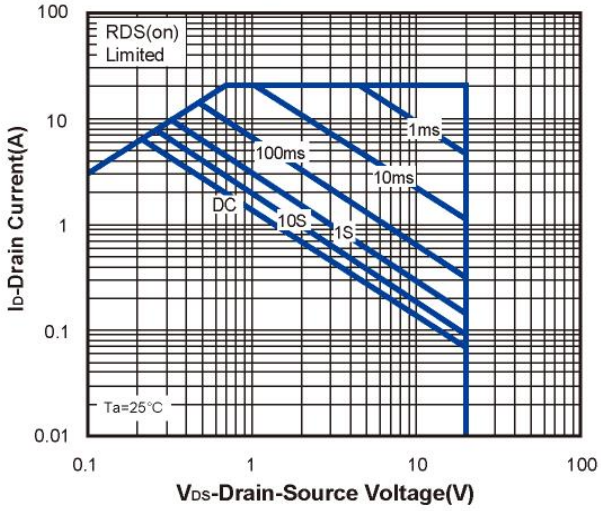
Gate Charge



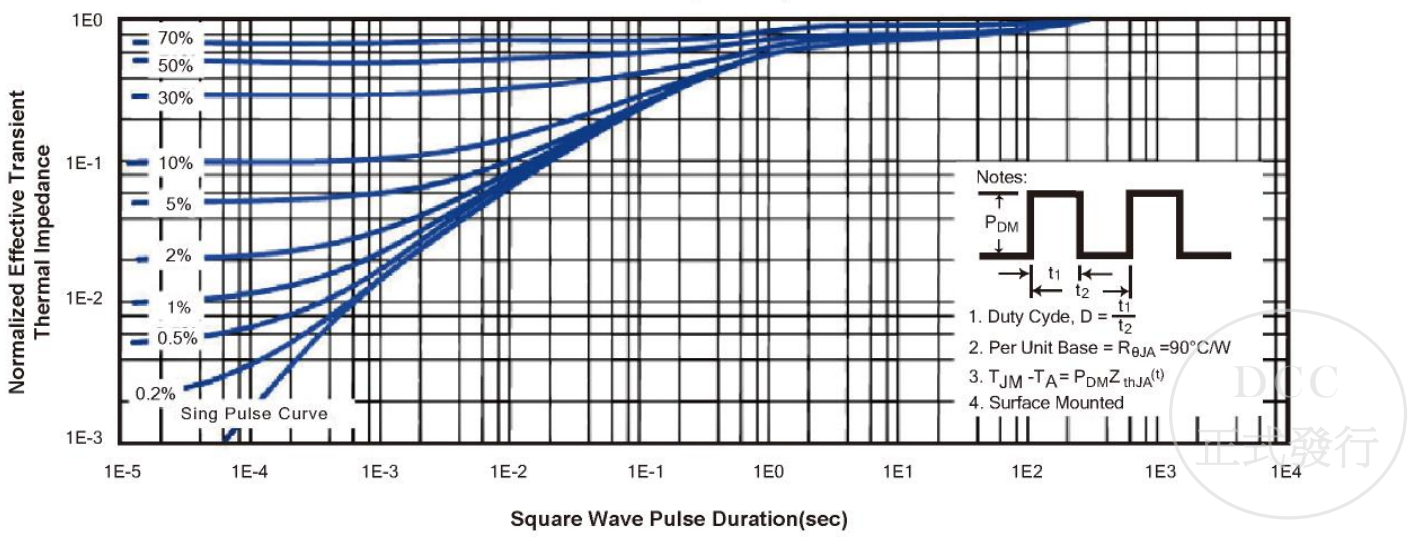
Body-diode characteristics



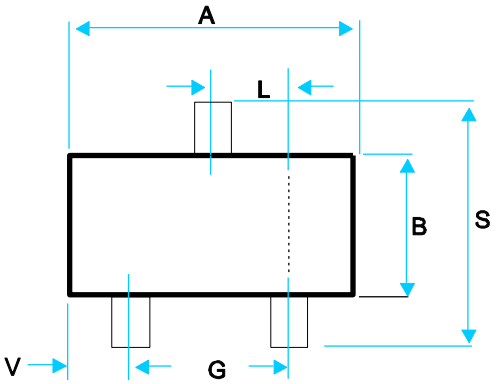
Maximum Forward Biased Safe Operating Area

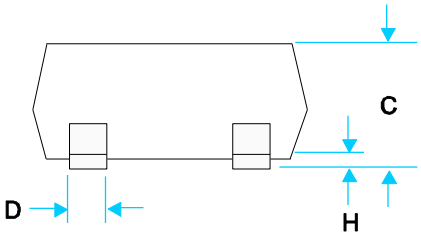


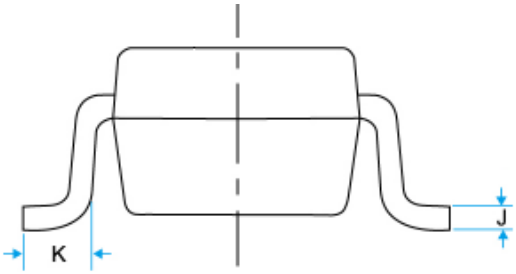
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60