

620 µA, 2 MHz Auto-Zeroed Op Amps

Features

- High DC Precision:
 - V_{OS} Drift: ±50 nV/°C (maximum)
 - V_{OS}: ±2 μV (maximum)
 - A_{OL}: 125 dB (minimum)
 - PSRR: 125 dB (minimum)
 - CMRR: 120 dB (minimum)
 - E_{ni} : 1.0 μV_{P-P} (typical), f = 0.1 Hz to 10 Hz
 - E_{ni} : 0.32 μV_{P-P} (typical), f = 0.01 Hz to 1 Hz
- Low Power and Supply Voltages:
 - I_Q: 620 µA/amplifier (typical)
 - Wide Supply Voltage Range: 2.3V to 5.5V
- · Easy to Use:
 - Rail-to-Rail Input/Output
 - Gain Bandwidth Product: 2 MHz (typical)
 - Unity Gain Stable
 - Available in Single and Dual
 - Single with Chip Select (CS): MCP6V28
- Extended Temperature Range: -40°C to +125°C

Typical Applications

- Portable Instrumentation
- · Sensor Conditioning
- · Temperature Measurement
- DC Offset Correction
- Medical Instrumentation

Design Aids

- SPICE Macro Models
- FilterLab[®] Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Parts

Parts with lower power, lower bandwidth and higher noise:

- MCP6V01/2/3: Spread clock
- MCP6V06/7/8: Non-spread clock

Description

The Microchip Technology Inc. MCP6V26/7/8 family of operational amplifiers provides input offset voltage correction for very low offset and offset drift. These devices have a wide gain bandwidth product (2 MHz, typical) and strongly reject switching noise. They are unity gain stable, have no 1/f noise, and have good power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). These products operate with a single supply voltage as low as 2.3V, while drawing 620 μ A/amplifier (typical) of quiescent current.

The Microchip Technology Inc. MCP6V26/7/8 op amps are offered as a single (MCP6V26), single with Chip Select (\overline{CS}) (MCP6V28) and dual (MCP6V27). They were designed using an advanced CMOS process.

Package Types (top view)



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$	6.5V
Current at Input Pins ††	±2 mA
Analog Inputs (V _{IN} + and V _{IN} -) $\uparrow \uparrow$ V _S	_S – 1.0V to V _{DD} +1.0V
All other Inputs and Outputs V_S	_S – 0.3V to V _{DD} +0.3V
Difference Input voltage	V _{DD} – V _{SS}
Output Short Circuit Current	Continuous
Current at Output and Supply Pins	±30 mA
Storage Temperature	65°C to +150°C
Max. Junction Temperature	+150°C
ESD protection on all pins (HBM, CDM, MM) ≥ 4 kV,1.5 kV, 300V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.2.1, Rail-to-Rail Inputs.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $\overline{CS} = GND$ (refer to Figure 1-5 and Figure 1-6).									
Parameters	Sym	Min	Тур	Max	Units	Conditions			
Input Offset									
Input Offset Voltage	V _{OS}	-2	—	+2	μV	T _A = +25°C (Note 1)			
Input Offset Voltage Drift with Temperature (linear Temp. Co.)	TC ₁	-50		+50	nV/°C	T _A = -40 to +125°C (Note 1)			
Input Offset Voltage Quadratic Temperature Coefficient	TC ₂	_	±0.2	—	nV/°C ²	T _A = -40 to +125°C			
Power Supply Rejection	PSRR	125	142	_	dB	(Note 1)			
Input Bias Current and Impedance									
Input Bias Current	I _B		+7	_	pА				
Input Bias Current across Temperature	Ι _Β		+110	—	pА	T _A = +85°C			
	I _B	_	+1.2	+5	nA	T _A = +125°C			
Input Offset Current	I _{OS}	_	±70	_	pА				
Input Offset Current across Temperature	I _{OS}	_	±50	—	pА	T _A = +85°C			
	I _{OS}	_	±60	_	pА	T _A = +125°C			
Common Mode Input Impedance	Z _{CM}	_	10 ¹³ 12	_	Ω pF				
Differential Input Impedance	Z _{DIFF}		10 ¹³ 12		Ω pF				

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC₁; see **Appendix B: "Offset Related Test Screens**").

2: Figure 2-18 shows how V_{CML} and V_{CMH} changed across temperature for the first production lot.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to $+5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $\overline{CS} = GND$ (refer to Figure 1-5 and Figure 1-6).									
Parameters	Sym	Min	Тур	Мах	Units	Conditions			
Common Mode	•		•	•		·			
Common-Mode Input Voltage Range Low	V _{CML}	—	_	V _{SS} – 0.15	V	(Note 2)			
Common-Mode Input Voltage Range High	V _{CMH}	V _{DD} + 0.2	_	_	V	(Note 2)			
Common-Mode Rejection	CMRR	120	136	_	dB	V _{DD} = 2.3V, V _{CM} = -0.15V to 2.5V (Note 1, Note 2)			
	CMRR	125	142	—	dB	V _{DD} = 5.5V, V _{CM} = -0.15V to 5.7V (Note 1, Note 2)			
Open-Loop Gain									
DC Open-Loop Gain (large signal)	A _{OL}	125	147		dB	V _{DD} = 2.3V, V _{OUT} = 0.2V to 2.1V (Note 1)			
	A _{OL}	133	155	_	dB	V _{DD} = 5.5V, V _{OUT} = 0.2V to 5.3V (Note 1)			
Output					•	·			
Minimum Output Voltage Swing	V _{OL}	_	V _{SS} + 5	V _{SS} + 15	mV	G = +2, 0.5V input overdrive			
Maximum Output Voltage Swing	V _{OH}	V _{DD} – 15	$V_{DD}-5$	_	mV	G = +2, 0.5V input overdrive			
Output Short Circuit Current	I _{SC}	—	±12	—	mA	V _{DD} = 2.3V			
	I _{SC}	—	±22	_	mA	V _{DD} = 5.5V			
Power Supply		•			r	1			
Supply Voltage	V _{DD}	2.3	—	5.5	V				
Quiescent Current per amplifier	l _Q	450	620	800	μA	I _O = 0			
POR Trip Voltage	V _{POR}	1.15	—	1.65	V				

Note 1: Set by design and characterization. Due to thermal junction and other effects in the production environment, these parts can only be screened in production (except TC₁; see Appendix B: "Offset Related Test Screens").

2: Figure 2-18 shows how V_{CML} and V_{CMH} changed across temperature for the first production lot.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$ (refer to Figure 1-5 and Figure 1-6).

Parameters	Sym	Min	Тур	Max	Units	Conditions
Amplifier AC Response						
Gain Bandwidth Product	GBWP	—	2.0	_	MHz	
Slew Rate	SR		1.0		V/µs	
Phase Margin	PM		65	_	0	G = +1
Amplifier Noise Response						
Input Noise Voltage	E _{ni}		0.32		μV _{P-P}	f = 0.01 Hz to 1 Hz
	E _{ni}	_	1.0		μV _{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e _{ni}		50	_	nV/√Hz	f < 5 kHz
	e _{ni}		29		nV/√Hz	f = 100 kHz
Input Noise Current Density	i _{ni}	_	0.6		fA/√Hz	
Amplifier Distortion (Note 1)						
Intermodulation Distortion (AC)	IMD	_	40		μV _{PK}	V _{CM} tone = 50 mV _{PK} at 1 kHz, G _N = 1
Amplifier Step Response						
Start Up Time	t _{STR}	—	75	_	μs	G = +1, V_{OS} within 50 μ V of its final value (Note 2)
Offset Correction Settling Time	t _{STL}	—	150	_	μs	G = +1, V _{IN} step of 2V, V _{OS} within 50 μ V of its final value
Output Overdrive Recovery Time	t _{ODR}	_	45	—	μs	G = -100, \pm 0.5V input overdrive to V _{DD} /2, V _{IN} 50% point to V _{OUT} 90% point (Note 3)

Note 1: These parameters were characterized using the circuit in Figure 1-7. In Figure 2-37 and Figure 2-38, there is an IMD tone at DC, a residual tone at 1 kHz, other IMD tones and clock tones.

2: High gains behave differently; see Section 4.3.3, Offset at Power Up.

3: t_{ODR} includes some uncertainty due to clock edge timing.

DIGITAL ELECTRICAL SPECIFICATIONS

TABLE 1-3: **Electrical Characteristics:** Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ kW to V_L , $C_L = 60$ pF, and $\overline{CS} = GND$ (refer to Figure 1-5 and Figure 1-6). **Parameters** Sym Min Max Units Conditions Тур CS Pull-Down Resistor (MCP6V28) CS Pull-Down Resistor MΩ R_{PD} 3 5 CS Low Specifications (MCP6V28) CS Logic Threshold, Low $0.3V_{DD}$ V VIL V_{SS} CS Input Current, Low 5 pА I_{CSL} $\overline{CS} = V_{SS}$ CS High Specifications (MCP6V28) CS Logic Threshold, High 0.7V_{DD} V VIH V_{DD} CS Input Current, High pA V_{DD}/R_{PD} I_{CSH} ____ _ $\overline{CS} = V_{DD}$ CS Input High, -0.4 μΑ I_{SS} $\overline{\text{CS}}$ = V_{DD}, V_{DD} = 2.3V GND Current per amplifier -1 ISS ____ μA $\overline{\text{CS}}$ = V_{DD}, V_{DD} = 5.5V Amplifier Output Leakage, 20 pА $\overline{CS} = V_{DD}$ IO_LEAK CS High CS Dynamic Specifications (MCP6V28) CS Low to Amplifier Output On 50 4 us t_{ON} $\overline{\text{CS}}$ Low = V_{SS}+0.3 V, G = +1 V/V, Turn-on Time $V_{OUT} = 0.9 V_{DD}/2$ CS High to Amplifier Output 1 $\overline{\text{CS}}$ High = V_{DD} – 0.3 V, G = +1 V/V, tOFF μs High-Z $V_{OUT} = 0.1 V_{DD}/2$

TABLE 1-4: TEMPERATURE SPECIFICATIONS

V_{HYST}

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = +2.3V to +5.5V, V_{SS} = GND.									
Parameters	Sym	Min	Тур	Max	Units	Conditions			
Temperature Ranges									
Specified Temperature Range	Τ _Α	-40		+125	°C				
Operating Temperature Range	T _A	-40		+125	°C	(Note 1)			
Storage Temperature Range	T _A	-65	_	+150	°C				
Thermal Package Resistances									
Thermal Resistance, 8L-4x4 DFN	θ_{JA}	—	48	—	°C/W	(Note 2)			
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W				
Thermal Resistance, 8L-SOIC	θ_{JA}	_	150	_	°C/W				
Thermal Resistance, 8L-2x3 TDFN	θ_{JA}	_	53	_	°C/W	(Note 2)			

0.2

V

Note 1: Operation must not cause T₁ to exceed Maximum Junction Temperature specification (+150°C).

2: Measured on a standard JC51-7, four layer printed circuit board with ground plane and vias.

Internal Hysteresis

1.3 Timing Diagrams



FIGURE 1-1: Amplifier S





FIGURE 1-2: Time.

Offset Correction Settling



FIGURE 1-3:

Output Overdrive Recovery.



1.4 Test Circuits

The circuits used for the DC and AC tests are shown in Figure 1-5 and Figure 1-6. Lay the bypass capacitors out as discussed in **Section 4.3.10**, **Supply Bypassing and Filtering**. R_N is equal to the parallel combination of R_F and R_G to minimize bias current effects.



FIGURE 1-5: AC and DC Test Circuit for Most Non-Inverting Gain Conditions.



FIGURE 1-6: AC and DC Test Circuit for Most Inverting Gain Conditions.

The circuit in Figure 1-7 tests the op amp input's dynamic behavior (i.e., IMD, t_{STR} , t_{STL} and t_{ODR}). The potentiometer balances the resistor network (V_{OUT} should equal V_{REF} at DC). The op amp's common mode input voltage is V_{CM} = V_{IN}/2. The error at the input (V_{ERR}) appears at V_{OUT} with a noise gain of 10 V/V.



FIGURE 1-7: Test Circuit for Dynamic Input Behavior.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^{\circ}$ C, $V_{DD} = +2.3$ V to 5.5V, $V_{SS} =$ GND, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = \text{GND}$.

2.1 **DC Input Precision**



FIGURE 2-1:

Input Offset Voltage.



FIGURE 2-2:

Input Offset Voltage Drift.



FIGURE 2-3: Input Offset Voltage Quadratic Temperature Coefficient.



FIGURE 2-4: Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CML}$.



FIGURE 2-5: Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CMH}$.



Output Voltage.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.3V to 5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/3$, V_{OUT} = $V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = \text{GND}$.



FIGURE 2-7: Input Offset Voltage vs. Common Mode Voltage with $V_{DD} = 2.3V$.



FIGURE 2-8: Input Offset Voltage vs. Common Mode Voltage with $V_{DD} = 5.5V$.









FIGURE 2-11: DC Open-Loop Gain.



FIGURE 2-12: CMRR and PSRR vs. Ambient Temperature.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.



FIGURE 2-13: DC Open-Loop Gain vs. Ambient Temperature.



FIGURE 2-14: Input Bias and Offset Currents vs. Common Mode Input Voltage with $T_A = +85$ °C.



FIGURE 2-15: Input Bias and Offset Currents vs. Common Mode Input Voltage with $T_A = +125$ °C.



FIGURE 2-16: Input Bias and Offset Currents vs. Ambient Temperature with $V_{DD} = +5.5V.$



FIGURE 2-17: Input Bias Current vs. Input Voltage (below V_{SS}).

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.

2.2 Other DC Voltages and Currents



FIGURE 2-18: Input Common Mode Voltage Headroom (Range) vs. Ambient Temperature.



FIGURE 2-19: Output Voltage Headroom vs. Output Current.



FIGURE 2-20: Output Voltage Headroom vs. Ambient Temperature.



FIGURE 2-21: Output Short Circuit Current vs. Power Supply Voltage.



FIGURE 2-22: Supply Current vs. Power Supply Voltage.



Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.



FIGURE 2-24: Power On Reset Voltage vs. Ambient Temperature.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.

2.3 Frequency Response



FIGURE 2-25: Frequency.



FIGURE 2-26: Open-Loop Gain vs. Frequency with $V_{DD} = 2.3V$.



FIGURE 2-27: Open-Loop Gain vs. Frequency with $V_{DD} = 5.5V$.



FIGURE 2-28: Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.



FIGURE 2-29: Gain Bandwidth Product and Phase Margin vs. Common Mode Input Voltage.



FIGURE 2-30: Gain Bandwidth Product and Phase Margin vs. Output Voltage.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.



FIGURE 2-31: Closed-Loop Output Impedance vs. Frequency with $V_{DD} = 2.3V$.



FIGURE 2-32: Closed-Loop Output Impedance vs. Frequency with $V_{DD} = 5.5V$.



FIGURE 2-33: Channel-to-Channel Separation vs. Frequency.



FIGURE 2-34: Maximum Output Voltage Swing vs. Frequency.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.

2.4 Input Noise and Distortion



FIGURE 2-35: Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.







FIGURE 2-37: Intermodulation Distortion vs. Frequency with V_{CM} Disturbance (see Figure 1-7).



FIGURE 2-38: Intermodulation Distortion vs. Frequency with V_{DD} Disturbance (see Figure 1-7).



FIGURE 2-39: Input Noise vs. Time with 1 Hz and 10 Hz Filters and V_{DD} =2.3V.



FIGURE 2-40: Input Noise vs. Time with 1 Hz and 10 Hz Filters and $V_{DD} = 5.5V$.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.

2.5 Time Response



FIGURE 2-41: Input Offset Voltage vs. Time with Temperature Change.



FIGURE 2-42: Input Offset Voltage vs. Time at Power Up.



FIGURE 2-43: The MCP6V26/7/8 Device Shows No Input Phase Reversal with Overdrive.



FIGURE 2-44:Non-inverting Small SignalStep Response.



FIGURE 2-45: Non-inverting Large Signal Step Response.



FIGURE 2-46: Response.

Inverting Small Signal Step

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$ and $\overline{CS} = GND$.



FIGURE 2-47: Inverting Large Signal Step Response.



FIGURE 2-48: Slew Rate vs. Ambient Temperature.



FIGURE 2-49: Output Overdrive Recovery vs. Time with G = -100 V/V.



FIGURE 2-50: Output Overdrive Recovery Time vs. Inverting Gain.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$, and $\overline{CS} = GND$.

2.6 Chip Select Response (MCP6V28 only)



FIGURE 2-51: Chip Select Current vs. Power Supply Voltage.



FIGURE 2-52: Power Supply Current vs. Chip Select Voltage with $V_{DD} = 2.3V$.



FIGURE 2-53: Power Supply Current vs. Chip Select Voltage with $V_{DD} = 5.5V$.



FIGURE 2-54: Chip Select Current vs. Chip Select Voltage.



FIGURE 2-55: Chip Select Voltage, Output Voltage vs. Time with $V_{DD} = 2.3V$.



FIGURE 2-56: Chip Select Voltage, Output Voltage vs. Time with $V_{DD} = 5.5V$.

Note: Unless otherwise indicated, $T_A = +25^{\circ}C$, $V_{DD} = +2.3V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L , $C_L = 60 \text{ pF}$, and $\overline{CS} = GND$.



FIGURE 2-57: Chip Select Relative Logic Thresholds vs. Ambient Temperature.



FIGURE 2-58:

Chip Select Hysteresis.



FIGURE 2-59: Chip Select Turn On Time vs. Ambient Temperature.



FIGURE 2-60: Chip Select's Pull-down Resistor (R_{PD}) vs. Ambient Temperature.



FIGURE 2-61: Quiescent Current in Shutdown vs. Power Supply Voltage.

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

N	MCP6V26		ICP6V27	MCP6V28		Symbol	Description
TDFN	MSOP, SOIC	DFN	MSOP, SOIC	TDFN	MSOP, SOIC	Symbol	Description
6	6	1	1	6	6	V _{OUT} , V _{OUTA}	Output (op amp A)
2	2	2	2	2	2	V _{IN} -, V _{INA} -	Inverting Input (op amp A)
3	3	3	3	3	3	V _{IN} +, V _{INA} +	Non-inverting Input (op amp A)
4	4	4	4	4	4	V _{SS}	Negative Power Supply
—	—	5	5	_	—	V _{INB} +	Non-inverting Input (op amp B)
—	—	6	6		—	V _{INB} –	Inverting Input (op amp B)
—	—	7	7		—	V _{OUTB}	Output (op amp B)
7	7	8	8	7	7	V _{DD}	Positive Power Supply
—	—	—	—	8	8	CS	Chip Select (op amp A)
1, 5, 8	1, 5, 8	—	—	1, 5	1, 5	NC	No Internal Connection
9	_	9	_	9	_	EP	Exposed Thermal Pad (EP); must be connected to V _{SS}

TABLE 3-1: PIN FUNCTION TABLE

3.1 Analog Outputs

The analog output pins (V_{OUT}) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs (V_{IN}+, V_{IN}-, \ldots) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.3V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Chip Select (CS) Digital Input

This pin (\overline{CS}) is a CMOS, Schmitt-triggered input that places the MCP6V28 op amp into a low power mode of operation.

3.5 Exposed Thermal Pad (EP)

There is an internal connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

4.0 APPLICATIONS

The MCP6V26/7/8 family of auto-zeroed op amps are manufactured using Microchip's state-of-the-art CMOS process. This family is designed for low cost, low power and high precision applications. Its low supply voltage, low quiescent current and wide bandwidth make the MCP6V26/7/8 devices ideal for battery-powered applications.

4.1 Overview of Auto-Zeroing Operation

Figure 4-1 shows a simplified diagram of the MCP6V26/7/8 auto-zeroed op amps. This will be used to explain how the DC voltage errors are reduced in this architecture.



FIGURE 4-1: Simplified Auto-Zeroed Op Amp Functional Diagram.

4.1.1 BUILDING BLOCKS

The Null Amplifier and Main Amplifier are designed for high gain and accuracy using a differential topology. They have a main input pair (+ and - pins at their top left) used for the signal. They have an auxiliary input pair (+ and - pins at their bottom left) used for correcting the offset voltages. Both input pairs are added together internally. The capacitors at the auxiliary inputs (C_{FW} and C_{H}) hold the corrected values during normal operation.

The Output Buffer is designed to drive external loads at the V_{OUT} pin. It also produces a single-ended output voltage (V_{REF} is an internal reference voltage).

All of these switches are make-before-break in order to minimize glitch-induced errors. They are driven by two clock phases (ϕ_1 and ϕ_2) that select between normal mode and auto-zeroing mode.

The clock is derived from an internal R-C oscillator running at a rate of f_{OSC1} = 850 kHz. The oscillator's output is divided down to the desired rate.

The internal POR ensures the part starts up in a known good state. It also provides protection against power supply brown-out events.

The Digital Control circuitry takes care of all of the housekeeping details of the switching operation. It also takes care of POR events.

4.1.2 AUTO-ZEROING ACTION

Figure 4-2 shows the connections between amplifiers during the Normal Mode of operation (ϕ_1). The hold capacitor (C_H) corrects the Null Amplifier's input offset. Since the Null Amplifier has very high gain, it dominates the signal seen by the Main Amplifier. This greatly reduces the impact of the Main Amplifier's input

offset voltage on overall performance. Essentially, the Null Amplifier and Main Amplifier behave as a regular op amp with very high gain (A_{OL}) and very low offset voltage (V_{OS}).





Figure 4-3 shows the connections between amplifiers during the Auto-zeroing Mode of operation (ϕ_2). The signal goes directly through the Main Amplifier, and the flywheel capacitor (C_{FW}) maintains a constant correction on the Main Amplifier's offset.

The Null Amplifier uses its own high open loop gain to drive the voltage across $C_{\rm H}$ to the point where its input offset voltage is almost zero. Because the signal input pair is connected to $V_{\rm IN}$ +, the auto-zeroing action corrects the offset at the current common mode input voltage ($V_{\rm CM}$) and supply voltage ($V_{\rm DD}$). This makes the DC CMRR and PSRR very high also.

Since these corrections happen every 40 $\mu s,$ or so, we also minimize slow errors, including offset drift with temperature ($\Delta V_{OS}/\Delta T_A),~1/f$ noise, and input offset aging.



FIGURE 4-3: Auto-zeroing Mode of Operation (ϕ_2); Equivalent Diagram.

4.1.3 INTERMODULATION DISTORTION (IMD)

The MCP6V26/7/8 op amps will show intermodulation distortion (IMD), products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the auto-zeroing circuitry's non-linear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock's harmonics has a series of IMD tones centered on it. See Figure 2-37 and Figure 2-38.

4.2 Other Functional Blocks

4.2.1 RAIL-TO-RAIL INPUTS

The input stage of the MCP6V26/7/8 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}, which is approximately equal to V_{IN}+ and V_{IN}- in normal operation) and the other at high V_{CM}. With this topology, the input operates with V_{CM} up to V_{DD} + 0.2V, and down to V_{SS} - 0.15V, at +25°C (see Figure 2-18). The input offset voltage (V_{OS}) is measured at V_{CM} = V_{SS} - 0.15V and V_{DD} + 0.2V to ensure proper operation.

The transition between the input stages occurs when $V_{CM} \approx V_{DD} - 1.2V$ (see Figure 2-7 and Figure 2-8). For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-43 shows an input voltage exceeding both supplies with no phase inversion.

4.2.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1, Absolute Maximum Ratings †**). This requirement is independent of the current limits discussed later on.

The ESD protection on the inputs can be depicted as shown in Figure 4-4. This structure was chosen to protect the input transistors against many (but not all) over-voltage conditions, and to minimize input bias current (I_B).



FIGURE 4-4: Simplified Analog Input ESD Structures.

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS} . They also clamp any voltages that are well above V_{DD} ; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond V_{DD}) events. Very fast ESD events (that meet the spec) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-5 shows one approach to protecting these inputs. D_1 and D_2 may be small signal silicon diodes, Schottky diodes for lower clamping voltages or diode-connected FETs for low leakage.



FIGURE 4-5: Protecting the Analog Inputs Against High Voltages.

4.2.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see Section 1.1, Absolute Maximum Ratings †). This requirement is independent of the voltage limits previously discussed.

Figure 4-6 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible current in or out of the input pins (and into D_1 and D_2). The diode currents will dump onto V_{DD} .



FIGURE 4-6: Protecting the Analog Inputs Against High Currents.

It is also possible to connect the diodes to the left of resistors R₁ and R₂. In this case, the currents through diodes D₁ and D₂ need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}-) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-17.

4.2.2 RAIL-TO-RAIL OUTPUT

The output voltage range of the MCP6V26/7/8 zero-drift op amps is V_{DD} – 15 mV (minimum) and V_{SS} + 15 mV (maximum) when R_L = 10 k Ω is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figure 2-19 and Figure 2-20.

This op amp is designed to drive light loads; use another amplifier to buffer the output from heavy loads.

4.2.3 CHIP SELECT (\overline{CS})

The single MCP6V28 has a Chip Select (\overline{CS}) pin. When \overline{CS} is pulled high, the supply current for the corresponding op amp drops to about 1 µA (typical), and is pulled through the \overline{CS} pin to V_{SS}. When this happens, the amplifier is put into a high impedance state. By pulling \overline{CS} low, the amplifier is enabled. If the \overline{CS} pin is left floating, the internal pull-down resistor (about 5 MΩ) will keep the part on. Figure 1-4 shows the output voltage and supply current response to a \overline{CS} pulse.

4.3 Application Tips

4.3.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

Table 1-1 gives both the linear and quadratic temperature coefficients (TC_1 and TC_2) of input offset voltage. The input offset voltage, at any temperature in the specified range, can be calculated as follows:

EQUATION 4-1:

$V_{OS}(T_A$) = V	$T_{OS} + TC_1 \Delta T + TC_2 \Delta T^2$
Where:		
ΔT	=	T _A – 25°C
$V_{OS}(T_A)$	=	input offset voltage at T _A
V _{OS}	=	input offset voltage at +25°C
TC ₁	=	linear temperature coefficient
TC ₂	=	quadratic temperature coefficient

4.3.2 DC GAIN PLOTS

Figure 2-9, Figure 2-10 and Figure 2-11 are histograms of the reciprocals (in units of μ V/V) of CMRR, PSRR and A_{OL}, respectively. They represent the change in input offset voltage (V_{OS}) with a change in common mode input voltage (V_{CM}), power supply voltage (V_{DD}) and output voltage (V_{OUT}).

The 1/A_{OL} histogram is centered near 0 μ V/V because the measurements are dominated by the op amp's input noise. The negative values shown represent noise, *not* unstable behavior. We validate the op amps' stability by making multiple measurements of V_{OS}; an unstable part would fail, because it would show either greater variability in V_{OS}, or the output stuck at one of the rails.

4.3.3 OFFSET AT POWER UP

When these parts power up, the input offset (V_{OS}) starts at its uncorrected value (usually less than ±5 mV). Circuits with high DC gain can cause the output to reach one of the two rails. In this case, the time to a valid output is delayed by an output overdrive time (like t_{ODR}), in addition to the startup time (like t_{STR}).

It can be simple to avoid this extra startup time. Reducing the gain is one method. Adding a capacitor across the feedback resistor (R_F) is another method.

4.3.4 SOURCE RESISTANCES

The input bias currents have two significant components; switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at +85°C and above.

Make the resistances seen by the inputs small and equal. This minimizes the output offset caused by the input bias currents.

The inputs should see a resistance on the order of 10Ω to $1 \ k\Omega$ at high frequencies (i.e., above 1 MHz). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.

Small input resistances are needed for high gains. Without them, parasitic capacitances can cause positive feedback and instability.

4.3.5 SOURCE CAPACITANCE

The capacitances seen by the two inputs should be small and matched. The internal switches connected to the inputs dump charges on these capacitors; an offset can be created if the capacitances do not match. Large input capacitances and source resistances, together with high gain, can lead to positive feedback and instability.

4.3.6 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. These auto-zeroed op amps have a different output impedance than most op amps, due to their unique topology.

When driving a capacitive load with these op amps, a series resistor at the output (R_{ISO} in Figure 4-7) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.



FIGURE 4-7: Output Resistor, R_{ISO}, Stabilizes Capacitive Loads.

Figure 4-8 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N^2). The y-axis is the normalized resistance (G_NR_{ISO}).

 G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).



FIGURE 4-8: Recommended R_{ISO} values for Capacitive Loads.

After selecting R_{ISO} for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_{ISO} 's value until the response is reasonable. Bench evaluation and simulations with the MCP6V26/7/8 SPICE macro model are helpful.

4.3.7 STABILIZING OUTPUT LOADS

This family of auto-zeroed op amps has an output impedance (Figure 2-31 and Figure 2-32) that has a double zero when the gain is low. This can cause a large phase shift in feedback networks that have low resistance near the part's bandwidth. This large phase shift can cause stability problems.

Figure 4-9 shows that the load on the output is $(R_L + R_{ISO})||(R_F + R_G)$, where R_{ISO} is before the load (like Figure 4-7). This load needs to be large enough to maintain stability; it should be at least $(2 \text{ k}\Omega)/G_N$.



FIGURE 4-9: Output Load.

4.3.8 GAIN PEAKING

Figure 4-10 shows an op amp circuit that represents non-inverting amplifiers (V_M is a DC voltage and V_P is the input) or inverting amplifiers (V_P is a DC voltage and V_M is the input). The capacitances C_N and C_G represent the total capacitance at the input pins; they include the op amp's common mode input capacitance (C_{CM}), board parasitic capacitance and any capacitor placed in parallel. The capacitance C_{FP} represents the parasitic capacitance coupling the output and non-inverting input pins.



FIGURE 4-10: Amplifier with Parasitic Capacitance.

 C_G acts in parallel with R_G (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing C_G or $R_F || R_G$.

 C_N and R_N form a low-pass filter that affects the signal at V_P . This filter has a single real pole at $1/(2\pi R_N C_N)$.

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The largest value of R_F that should be used depends on noise gain (see G_N in Section 4.3.6, Capacitive Loads), C_G and the open-loop gain's phase shift. An approximate limit for R_F is:

EQUATION 4-2:

$$R_F \le 2 \ k\Omega \times \frac{12 \ pF}{C_G} \times G_N^2$$

Some applications may modify these values to reduce either output loading or gain peaking (step response overshoot).

At high gains, R_G and C_G need to be small in order to prevent positive feedback and oscillations.

4.3.9 REDUCING UNDESIRED NOISE AND SIGNALS

Reduce undesired noise and signals with:

- · Low bandwidth signal filters:
 - Minimizes random analog noise
 - Reduces interfering signals
- · Good PCB layout techniques:
 - Minimizes crosstalk
 - Minimizes parasitic capacitances and inductances that interact with fast switching edges
- · Good power supply design:
 - Provides isolation from other parts
 - Filters interference on supply line(s)

4.3.10 SUPPLY BYPASSING AND FILTERING

With this family of op amps, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm of the pin for good high-frequency performance.

These parts also need a bulk capacitor (i.e., $1 \ \mu F$ or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other low noise, analog parts.

In some cases, high-frequency power supply noise (e.g., switched mode power supplies) may cause undue intermodulation distortion, with a DC offset shift; this noise needs to be filtered. Adding a resistor into the supply connection can be helpful. This resistor needs to be small enough to prevent a large drop in V_{DD} for the op amp, which would cause a reduced output range and possible load-induced power supply noise. It also needs to be large enough to dissipate little power when V_{DD} is turned on and off quickly. Figure 4-11 shows a circuit with resistors in the supply connections. It gives good rejection out to 1 MHz for switched mode power

supplies. Smaller resistors and capacitors are a better choice for designs where the power supply is not as noisy.



FIGURE 4-11: Additional Supply Filtering.

4.3.11 PCB DESIGN FOR DC PRECISION

In order to achieve DC precision on the order of $\pm 1 \mu$ V, many physical errors need to be minimized. The design of the Printed Circuit Board (PCB), the wiring and the thermal environment has a strong impact on the precision achieved. A poor PCB design can easily be more than 100 times worse than the MCP6V26/7/8 op amps minimum and maximum specifications.

4.3.11.1 PCB Layout

Any time two dissimilar metals are joined together, a temperature dependent voltage appears across the junction (the Seebeck or thermo-junction effect). This effect is used in thermocouples to measure temperature. The following are examples of thermo-junctions on a PCB:

- Components (resistors, op amps, ...) soldered to a copper pad
- · Wires mechanically attached to the PCB
- Jumpers
- · Solder joints
- PCB vias

Typical thermo-junctions have temperature to voltage conversion coefficients of 10 to 100 μ V/°C (sometimes higher).

Microchip's AN1258 (*"Op Amp Precision Design: PCB Layout Techniques"*) contains in depth information on PCB layout techniques that minimize thermo-junction effects. It also discusses other effects, such as crosstalk, impedances, mechanical stresses and humidity.

4.3.11.2 Crosstalk

DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:

- · Common mode noise (remote sensors)
- Ground loops (current return paths)
- · Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz), and other AC sources, can also affect the DC performance. Non-linear distortion can convert these signals to multiple tones, including a DC shift in voltage. When the signal is sampled by an ADC, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:

- Keep traces and wires as short as possible
- Use shielding (e.g., encapsulant)
- Use ground plane (at least a star ground)
- Place the input signal source near to the DUT
- Use good PCB layout techniques
- Use a separate power supply filter (bypass capacitors) for these auto-zeroed op amps

4.3.11.3 Miscellaneous Effects

Keep the resistances seen by the input pins as small and as near to equal as possible, to minimize bias current-related offsets.

Make the (trace) capacitances seen by the input pins small and equal. This is helpful in minimizing switching glitch-induced offset voltages.

Bending a coax cable with a radius that is too small causes a small voltage drop to appear on the center conductor (the tribo-electric effect). Make sure the bending radius is large enough to keep the conductors and insulation in full contact.

Mechanical stresses can make some capacitor types (such as ceramic) to output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electro-chemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

4.4 Typical Applications

4.4.1 WHEATSTONE BRIDGE

Many sensors are configured as Wheatstone bridges. Strain gauges and pressure sensors are two common examples. These signals can be small and the common mode noise large. Amplifier designs with high differential gain are desirable.

Figure 4-12 shows how to interface to a Wheatstone bridge with a minimum of components. Because the circuit is not symmetric, the ADC input is single ended, there is a minimum of filtering, and the CMRR is good enough for moderate common mode noise.



FIGURE 4-12: Simple Design.

Figure 4-13 shows a higher performance circuit for Wheatstone bridges. This circuit is symmetric and has high CMRR. Using a differential input to the ADC helps with the CMRR.



FIGURE 4-13: High Performance Design.

4.4.2 RTD SENSOR

The ratiometric circuit in Figure 4-14 conditions a three wire RTD. It corrects for the sensor's wiring resistance by subtracting the voltage across the middle R_W . The top R_1 does not change the output voltage; it balances the op amp inputs. Failure (open) of the RTD is detected by an out-of-range voltage.



FIGURE 4-14: RTD Sensor.

The voltages at the input of the ADC can be calculated with the following:

$$\begin{split} G_{RTD} &= 1 + 2 \cdot R_3 / R_2 \\ G_W &= G_{RTD} - R_3 / R_1 \\ V_{DM} &= G_{RTD} (V_T - V_B) + G_W V_W \\ V_{CM} &= \frac{V_T + V_B + (G_{RTD} + 1 - G_W) V_W}{2} \end{split}$$

Where:

$$\begin{array}{lll} V_{T} & = & \mbox{Voltage at the top of } R_{RTD} \\ V_{B} & = & \mbox{Voltage at the bottom of } R_{RTD} \\ V_{W} & = & \mbox{Voltage across top and middle } R_{W}'s \\ V_{CM} & = & \mbox{ADC's common mode input} \\ V_{DM} & = & \mbox{ADC's differential mode input} \end{array}$$

4.4.3 THERMOCOUPLE SENSOR

Figure 4-15 shows a simplified diagram of an amplifier and temperature sensor used in a thermocouple application. The type K thermocouple senses the temperature at the hot junction (T_{HJ}) , and produces a voltage at V₁ proportional to T_{HJ} (in °C). The amplifier's gain is set so that V₄/ T_{HJ} is 10 mV/°C. V₃ represents the output of a temperature sensor, which produces a voltage proportional to the temperature (in °C) at the cold junction (T_{CJ}), and with a 0.50V offset. V₂ is set so that V₄ is 0.50V when $T_{HJ} - T_{CJ}$ is 0°C.

EQUATION 4-3:

$$\begin{split} & \mathsf{V}_1 \approx \mathsf{T}_{\mathsf{HJ}}(40 \; \mu \mathsf{V}/^\circ \mathsf{C}) \\ & \mathsf{V}_2 = (1.00\mathsf{V}) \\ & \mathsf{V}_3 = \mathsf{T}_{\mathsf{CJ}}(10 \; \mathsf{mV}/^\circ \mathsf{C}) + (0.50\mathsf{V}) \\ & \mathsf{V}_4 = 250\mathsf{V}_1 + (\mathsf{V}_2 - \mathsf{V}_3) \\ & \approx (10 \; \mathsf{mV}/^\circ \mathsf{C}) \; (\mathsf{T}_{\mathsf{HJ}} - \mathsf{T}_{\mathsf{CJ}}) + (0.50\mathsf{V}) \end{split}$$



FIGURE 4-15: Thermocouple Sensor; Simplified Circuit.

Figure 4-16 shows a more complete implementation of this circuit. The dashed red arrow indicates a thermally conductive connection between the thermocouple and the MCP9700A; it needs to be very short and have low thermal resistance.



FIGURE 4-16: Thermocouple Sensor.

The MCP9700A senses the temperature at its physical location. It needs to be at the same temperature as the cold junction (T_{CJ}), and produces V₃ (Figure 4-15).

The MCP1541 produces a 4.10V output, assuming V_{DD} is at 5.0V. This voltage, tied to a resistor ladder of 4.100(R_{TH}) and 1.3224(R_{TH}), would produce a Thevenin equivalent of 1.00V and 250(R_{TH}). The 1.3224(R_{TH}) resistor is combined in parallel with the top right R_{TH} resistor (in Figure 4-15), producing the 0.5696(R_{TH}) resistor.

 V_4 should be converted to digital, then corrected for the thermocouple's non-linearity. The ADC can use the MCP1541 as its voltage reference. Alternately, an absolute reference inside a PICmicro[®] device can be used instead of the MCP1541.

4.4.4 OFFSET VOLTAGE CORRECTION

Figure 4-17 shows an MCP6V27 correcting the input offset voltage of another op amp. R_2 and C_2 integrate the offset error seen at the other op amp's input; the integration needs to be slow enough to be stable (with the feedback provided by R_1 and R_3).



FIGURE 4-17: Offset Correction.

4.4.5 PRECISION COMPARATOR

Use high gain before a comparator to improve the latter's performance. Do not use MCP6V26/7/8 as a comparator by itself; the V_{OS} correction circuitry does not operate properly without a feedback loop.



FIGURE 4-18: Precision Comparator.

NOTES:

5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6V26/7/8 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6V26/7/8 family of op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab[®] Software

Microchip's FilterLab[®] software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the Filter-Lab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase and Sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6V01 Thermocouple Auto-Zeroed Reference Design
- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- P/N SOIC8EV: 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board
- P/N SOIC14EV: 14-Pin SOIC/TSSOP/DIP Evaluation Board

5.5 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

ADN003: "Select the Right Operational Amplifier for your Filtering Circuits", DS21821

AN722: "Operational Amplifier Topologies and DC Specifications", DS00722

AN723: "Operational Amplifier AC Specifications and Applications", DS00723

AN884: "Driving Capacitive Loads With Op Amps", DS00884

AN990: "Analog Sensor Conditioning Circuits – An Overview", DS00990

AN1177: "Op Amp Precision Design: DC Errors", DS01177

AN1228: "Op Amp Precision Design: Random Noise", DS01228

AN1258: "Op Amp Precision Design: PCB Layout Techniques", DS01258

These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

NOTES:

6.0 PACKAGING INFORMATION

6.1 **Package Marking Information**

8-Lead DFN (4x4x0.9 mm) (MCP6V27)



8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]



Microchip Technology Drawing C04-131E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	3.40	3.50	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	ĸ	0.20	-	-

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package may have one or more exposed tie bars at ends.
- 3. Package is saw singulated
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimensior	MIN	NOM	MAX	
Contact Pitch	E 0.80 BSC			
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







	Units	MILLIMETERS			
Dir	mension Limits	MIN	NOM	MAX	
Number of Pins	N		8		
Pitch	е		0.65 BSC		
Overall Height	А	-	-	1.10	
Molded Package Thickness	A2	0.75	0.85	0.95	
Standoff	A1	0.00	-	0.15	
Overall Width	E	4.90 BSC			
Molded Package Width	E1		3.00 BSC		
Overall Length	D		3.00 BSC		
Foot Length	L	0.40	0.60	0.80	
Footprint	L1	0.95 REF			
Foot Angle	ф	0°	-	8°	
Lead Thickness	С	0.08	-	0.23	
Lead Width	b	0.22	-	0.40	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units			
Dimensio	Dimension Limits		NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Pins	N		8		
Pitch	е		1.27 BSC		
Overall Height	А	-	-	1.75	
Molded Package Thickness	A2	1.25	-	-	
Standoff §	A1	0.10	-	0.25	
Overall Width	Е	6.00 BSC			
Molded Package Width	E1	3.90 BSC			
Overall Length	D	4.90 BSC			
Chamfer (Optional)	h	0.25	-	0.50	
Foot Length	L	0.40	-	1.27	
Footprint	L1		1.04 REF		
Foot Angle	φ	0°	-	8°	
Lead Thickness	С	0.17	-	0.25	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Contact Pitch	E		1.27 BSC		
Contact Pad Spacing	С		5.40		
Contact Pad Width (X8)	X1			0.60	
Contact Pad Length (X8)	Y1			1.55	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



BOTTOM VIEW

Microchip Technology Drawing No. C04-129C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	Ν	MILLIMETERS		
Dimensior	n Limits	MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	е	0.50 BSC			
Overall Height	Α	0.70	0.75	0.80	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Length	D	2.00 BSC			
Overall Width	E	3.00 BSC			
Exposed Pad Length	D2	1.20	-	1.60	
Exposed Pad Width	E2	1.20	-	1.60	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.25	0.30	0.45	
Contact-to-Exposed Pad	K	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package may have one or more exposed tie bars at ends.

3. Package is saw singulated

4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	E	0.50 BSC			
Optional Center Pad Width	W2			1.46	
Optional Center Pad Length	T2			1.36	
Contact Pad Spacing	C1		3.00		
Contact Pad Width (X8)	X1			0.30	
Contact Pad Length (X8)	Y1			0.75	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision B (August 2011)

The following is the list of modifications:

- 1. Added the MCP6V26 and MCP6V28 single op amps.
 - a) Updated package drawings on page 1.
 - b) Updated the pinout table (Table 3-1).
 - c) Added 8-lead, 2×3 TDFN package to the Thermal Characteristics Table (Table 1-4).
 - d) Added 8-lead, 2×3 TDFN package to Section 6.0 "Packaging Information".
 - e) Added parts numbers to Product Identification System.
- 2. Added Chip Select (\overline{CS}) information.
 - a) Added Digital Electrical Specifications table (Table 1-3).
 - b) Added Timing Diagram (Figure 1-4).
 - c) Added Section 2.6 "Chip Select Response (MCP6V28 only)" to the Typical Performance Curves.
 - d) Added Section 4.2.3 "Chip Select (CS)" to the applications write up.
- 3. Added information on positive feedback and parasitic feedback capacitance.
 - a) Added to Section 4.3.4 "Source Resistances".
 - b) Added to Section 4.3.5 "Source Capacitance".
 - c) Modified Figure 4-10.
 - d) Added to Section 4.3.8 "Gain Peaking".
- 4. Other minor typographical corrections.

Revision A (March 2011)

• Original data sheet for the MCP6V27 dual op amps.

APPENDIX B: OFFSET RELATED TEST SCREENS

Input offset voltage-related specifications in the DC spec table (Table 1-1) are based on bench measurements (see Section 2.1 "DC Input Precision"). These measurements are much more accurate because:

- · More compact circuit
- Soldered parts on the PCB (to validate other measurements)
- More time spent averaging (reduces noise)
- · Better temperature control
 - Reduced temperature gradients
 - Greater accuracy

TABLE B-1: OFFSET RELATED TEST SCREENS

Electrical Characteristics: Unless otherwise indicated, T _A = +25°C, V _{DD} = +2.3V to +5.5V, V _{SS} = GND,							
$V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to V_L and $\overline{CS} = \text{GND}$ (refer to Figure 1-5 and Figure 1-6).							
Parameters	Sym	Min	Max	Units	Conditions		
Input Offset							
Input Offset Voltage	V _{OS}	-10	+10	μV	T _A = +25°C (Note 1, Note 2)		
Input Offset Voltage Drift with Temperature (linear Temp. Co.)	TC ₁	_	_	nV/°C	T _A = -40 to +125°C (Note 3)		
Power Supply Rejection	PSRR	115	_	dB	(Note 1)		
Common Mode							
Common Mode Rejection	CMRR	106		dB	V_{DD} = 2.3V, V_{CM} = -0.15V to 2.5V (Note 1)		
	CMRR	116	_	dB	V_{DD} = 5.5V, V_{CM} = -0.15V to 5.7V (Note 1)		
Open-Loop Gain							
DC Open-Loop Gain (large signal)	A _{OL}	114	_	dB	V _{DD} = 2.3V, V _{OUT} = 0.2V to 2.1V (Note 1)		
	A _{OL}	122	_	dB	V _{DD} = 5.5V, V _{OUT} = 0.2V to 5.3V (Note 1)		

Note 1: Due to thermal junctions and other errors in the production environment, these specifications are only screened in production.

2: V_{OS} is also sample screened at +125°C.

3: TC₁ is not measured in production.

We use production screens to ensure the quality of our outgoing products. These screens are set at wider limits to eliminate any fliers; see Table B-1.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. –X /XX		Examples:			
Device Temperature Package Range	a)	MCP6V26T-E/MNY:	Extended temperature, 8LD 2×3 TDFN package		
	b)	MCP6V26-E/MS:	Extended temperature, 8LD MSOP package		
Device: MCP6V26 Single Op Amp MCP6V26T Single Op Amp (Tape and Reel) MCP6V27 Dual Op Amp	a)	MCP6V26T-E/SN:	Tape and Reel, Extended temperature, 8LD SOIC package		
MCP6V2/1 Dual Op Amp (Tape and Reel) MCP6V28 Single Op Amp with Chip Select MCP6V28T Single Op Amp with Chip Select	a)	MCP6V27-E/MD:	Extended temperature, 8LD 4x4 DFN package		
(Tape and Reel)	b)	MCP6V27-E/MS:	Extended temperature, 8LD MSOP package		
Temperature Range: E = -40°C to +125°C	c)	MCP6V27-E/SN:	Extended temperature, 8LD SOIC package		
Package: MD = Plastic Dual Flat, No-Lead (4×4x0.9), 8-lead	a)	MCP6V28T-E/MNY:	Extended temperature, 8LD 2×3 TDFN package		
MS = Plastic Micro Small Outline Package, 8-lead SN = Plastic SOIC (150mil Body), 8-lead	b)	MCP6V28-E/MS:	Extended temperature, 8LD MSOP package		
* Y = Nickel Palladium gold manufacturing designator. Only available on the TDFN package.	c)	MCP6V28T-E/SN:	Tape and Reel, Extended temperature, 8LD SOIC package		

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