MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Product Preview 256K x 4 Bit Fast Static Random Access Memory

The MCM6728A is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static -- No Clock or Timing Strobes Necessary
- · All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise



MCM6728A



PIN ASSIGNMENT										
AC	1 •	28] A [
۸C	2	27] A							
ΑC	3	26] A							
AC	4	25] A							
Ē	5	24] A							
DQ0 [6	23] DQ3							
V _{CC} [7	22) v _{ss}							
V _{SS} [8	21] v _{cc}							
DQ1 [9	20	DQ2							
₩c	10	19] A							
٨C	11	18] A							
۸Ū	12	17] A							
٨C	13	16	D 🗛							
۸C	14	15	0 🗛							

PIN NA	MES
A0 – A17	Address Input
E	Chip Enable
W	Write Enable
DQ0 – DQ3	Data Input/Output
V _{CC} +	5 V Power Supply
V _{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

Ē	W	Mode	V _{CC} Current	Output	Cycle
н	×	Not Selected	ISB1, ISB2	High-Z	-
L	н	Read	ICCA	Dout	Read Cycle
L	L	Write	ICCA	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Vaiue	Unit
Power Supply Voltage	Vcc	- 0.5 to + 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	Vin, V _{out}	- 0.5 to V _{CC} + 0.5	V
Output Current	lout	± 30	mA
Power Dissipation	PD	1.0	w
Temperature Under Bias	T _{bias}	- 10 to + 85	°C
Operating Temperature	TA	0 to + 70	°C
Storage Temperature—Plastic	Tstg	- 55 to + 125	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER-ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V \pm 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage (Operating Voltage Range)	Vcc	4.5	5.0	5.5	V
Input High Voltage	VIH	2.2	-	V _{CC} + 0.3**	v
Input Low Voltage	VIL	- 0.5*	-	0.8	V

* V_{IL} (min) = -0.5 V dc; V_{IL} (min) = -2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width \leq 2.0 ns) for I \leq 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, Vin = 0 to V _{CC})	l _{ikg(i)}		±1.0	μA
Output Leakage Current ($\overline{E} = V_{IH}, V_{out} = 0$ to V_{CC})	likg(O)		± 1.0	μA
Output Low Voltage (I _{OL} = + 8.0 mA)	VOL	-	0.4	V
Output High Voltage (IOH = - 4.0 mA)	VOH	2.4	-	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6728A-8	6728A-10	6728A-12	6728A-15	Unit
AC Active Supply Current (I _{out} = 0 mA) (V _{CC} = max, f = f _{max})	ICCA	175	165	155	145	mA
Active Quiescent Current ($\vec{E} = V_{IL}$, $V_{CC} = max$, f = 0 MHz)	ICC2	90	90	90	90	mA
AC Standby Current ($\overline{E} = V_{IH}$, $V_{CC} = max$, $f = f_{max}$)	ISB1	60	60	60	60	mA
$\begin{array}{l} \mbox{CMOS Standby Current} (V_{CC} = max, f = 0 \mbox{ MHz}, \overline{E} \geq V_{CC} - 0.2 \mbox{ V}, \\ V_{in} \leq V_{SS} + 0.2 \mbox{ V}, or \geq V_{CC} - 0.2 \mbox{ V}) \end{array}$	ISB2	20	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, TA = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Тур	Max	Unit
Address Input Capacitance	C _{in}	-	6	рF
Control Pin Input Capacitance	C _{in}	-	6	рF
Input/Output Capacitance	CI/O	-	8	рF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V \pm 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse Levels	0 to 3.0 V
Input Rise/Fall Time	2 ns

READ CYCLE TIMING (See Notes 1 and 2)

	Sym	nbol	6728A-8		6728A-10		6728A-12		6728A-15			
Parameter	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read Cycle Time	^t AVAV	tRC	8	. —	10	—	12	-	15	—	ns	3
Address Access Time	tavqv	t _{AA}	—	8	-	10	-	12	—	15	ns	
Enable Access Time	^t ELQV	tACS	-	8	-	10	_	12	-	15	ns	
Output Hold from Address Change	†AXQX	tон	3	-	3	—	3	1	3	-	ns	
Enable Low to Output Active	^t ELQX	^t CLZ	3	—	3	-	3	-	3	-	ns	4,5,6
Enable High to Output High-Z	^t EHQZ	^t CHZ	0	4	0	5	0	6	0	7	ns	4,5,6

NOTES:

1. W is high for read cycle.

2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

3. All read cycle timings are referenced from the last valid address to the first transitioning address.

4. At any given voltage and temperature, tEHQZ max < tELQX min, for a given device.

5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.

6. This parameter is sampled and not 100% tested.

7. Device is continuously selected ($\overline{E} = V_{IL}$).

8. Addresses valid prior to or coincident with E going low.

AC TEST LOADS



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)



WRITE CYCLE 1 (W Controlled, See Notes 1 and 2)

	Symbol		6728	6728A-8 6728A-		A-10	10 6728A-12		6728A-15			
Parameter	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	tavav	twc	8	_	10	_	12		15	—	ns	3
Address Setup Time	tAVWL	tAS	0	-	0	-	0	—	0	-	ns	
Address Valid to End of Write	tavwh	tAW	8	_	9	_	10		12	—	ns	
Write Pulse Width	^t WLWH ^t WLEH	tWP tWP	8	-	9	-	10	-	12		ns	
Data Valid to End of Write	tDVWH	tDW	4	-	5	-	6	—	7	—	ns	
Data Hold Time	tWHDX	^t DH	0	_	0	—	0		0	—	ns	
Write Low to Data High-Z	twloz	twz	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	twhox	tow	3	_	3	-	3	—	3	-	ns	4,5,6
Write Recovery Time	twhax.	twR	0	—	0	—	0	-	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.

2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

3. All write cycle timings are referenced from the last valid address to the first transitioning address.

4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.

5. This parameter is sampled and not 100% tested.

6. At any given voltage and temperature, twLQZ max < twHQX min both for a given device and from device to device.

WRITE CYCLE 1



WRITE CYCLE 2 (E Controlled, See Notes 1 and 2)

· · · · · · · · · · · · · · · · · · ·	Syn	nbol	6728A-8		6728A-10		6728A-12		6728A-15			
Parameter	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	^t AVAV	twc	8	—	10	—	12	—	15	-	ns	3
Address Setup Time	^t AVEL	tAS	0	-	0	-	0	—	0		ns	
Address Valid to End of Write	^t AVEH	tAW	7	—	8	-	9	-	10		ns	
Enable to End of Write	^t ELEH	tcw	7	-	8	—	9	—	10	—	ns	4,5
Enable to End of Write	tELWH	tcw	7	-	8	-	9	-	10	—	ns	4,5
Data Valid to End of Write	^t DVEH	tDW	4	—	5	—	6	—	7	—	ns	
Data Hold Time	^t EHDX	^t DH	0	-	0	-	0	-	0		ns	
Write Recovery Time	^t EHAX	twR	0	—	0	-	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.

2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

3. All write cycle timings are referenced from the last valid address to the first transitioning address.

If E goes low coincident with or after W goes low, the output will remain in a high impedance condition.
If E goes high coincident with or before W goes high, the output will remain in a high impedance condition.



WRITE CYCLE 2