Freescale Semiconductor
Data Sheet: Technical Data

An Energy Efficient Solution by Freescale

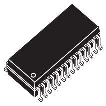
Document Number: MC9S08QE8
Rev. 7, 4/2009

MC9S08QE8

MC9S08QE8 Series

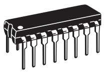
Covers: MC9S08QE8 and MC9S08QE4

32-Pin LQFP
Case 873A

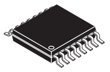


28-Pin SOIC
751F-05

20-Pin SOIC
751D-07



16-Pin PDIP
648



16-Pin TSSOP
948F

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 3.6 V to 1.8 V across temperature range of –40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes
  - Reduced power wait mode
  - Low power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
  - 6 µs typical wake-up time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies from 1 MHz to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
  - **ADC** — 10-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
  - **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - **SCI** — Full-duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake-up on active edge
  - **SPI** — Full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - **IIC** — Up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supporting broadcast mode and 10-bit addressing
  - **TPMx** — Two 3-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wakeup without external components; runs in all MCU modes
- Input/Output
  - 26 GPIOs, one output-only pin and one input-only pin
  - Eight KBI interrupts with selectable polarity
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins.
- Package Options
  - 32-pin LQFP, 28-pin SOIC, 20-pin SOIC, 16-pin PDIP, 16-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
2	Nov 7 2007	Initial preliminary product preview release.
3	Jan 22 2008	Initial public release.
4	March 13 2008	Added Figure 11.
5	October 8 2008	Updated the Stop2 and Stop3 mode supply current in the Table 8. Replaced the stop mode adders section from Table 8 with an individual Table 9 with new specifications. Added a footnote to the Min. of the suppply voltage in Table 7. Changed the typical value of $\|I_{In}\|$ and $\|I_{OZ}\|$ to — (no typical value) in Table 7. Added t_{VRR} to Table 12. Updated “How to reach us” information.
6	Nov. 4 2008	Updated the operating voltage in Table 7.
7	April 29 2009	Changed V_{DDAD} to V_{DDA}, I_{DDAD} to I_{DDA}, and V_{SSAD} to V_{SSA}. In Table 7, added $\|I_{OZTOT}\|$. In Table 11, updated the DCO output frequency range-trimmed, and changed some symbols. Updated typicals and Max. for $t_{IRST.}$ Updated Table 17.

Related Documentation

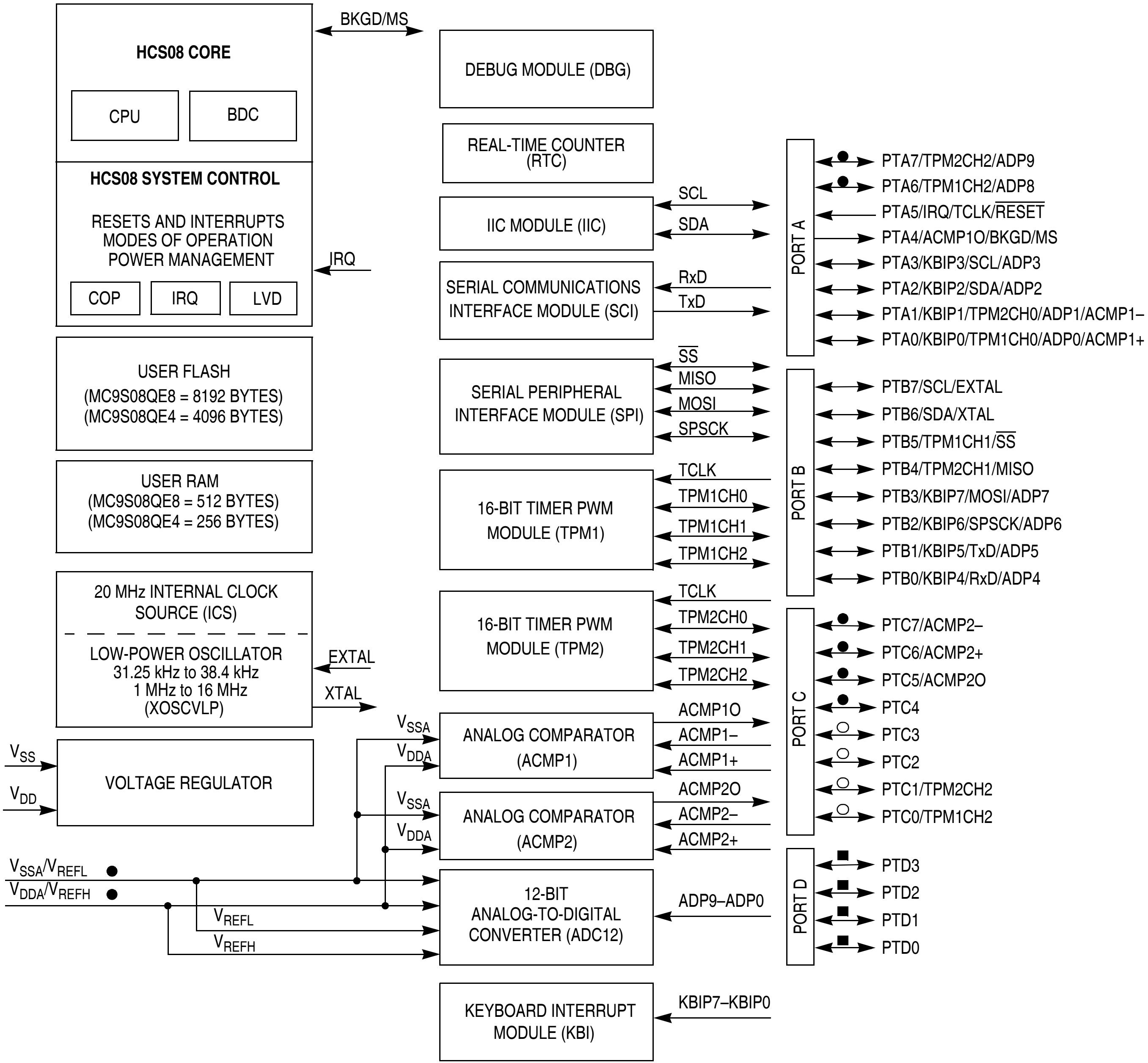
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08QE8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of MC9S08QE8 series MCU.



○ pins not available on 16-pin packages

● pins not available on 16-pin or 20-pin packages

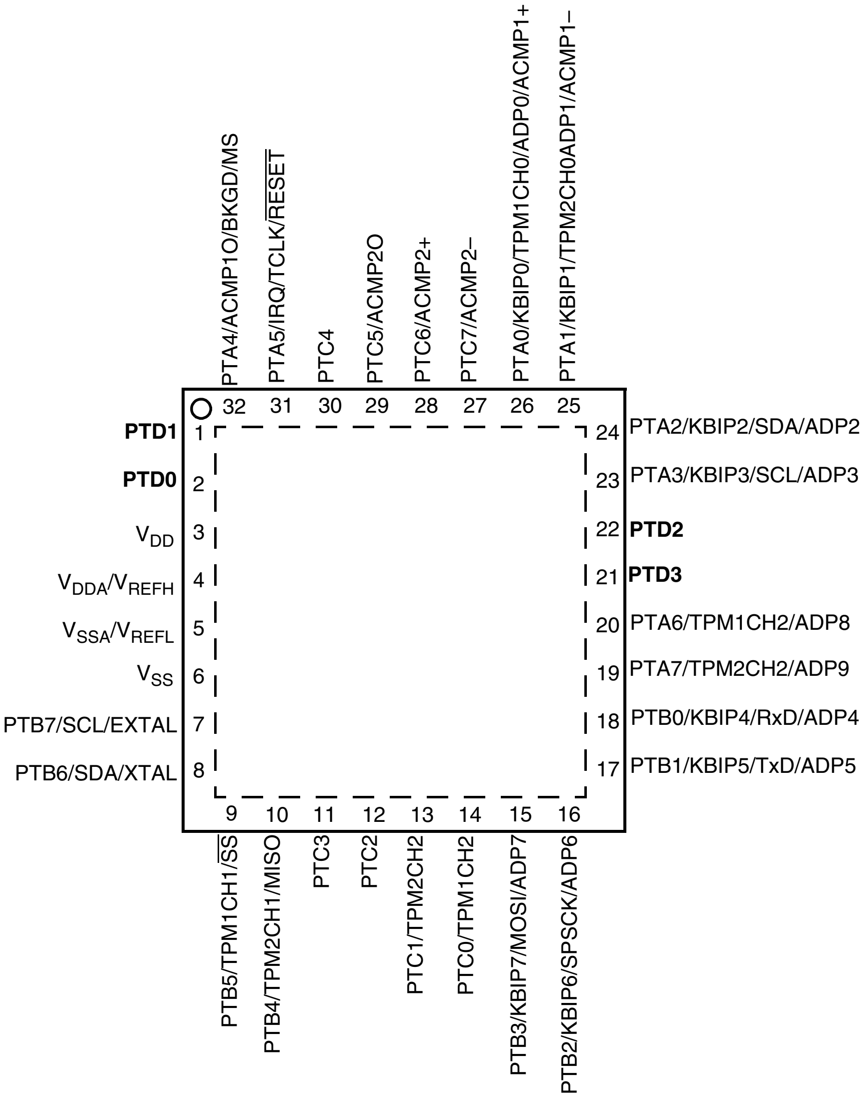
■ pins not available on 16-pin, 20-pin or 28-pin packages

Notes: When PTA5 is configured as $\overline{RESET}$, pin becomes bi-directional with output being open-drain drive containing an internal pullup device.
When PTA4 is configured as BKGD, pin becomes bi-directional.
For the 16-pin and 20-pin packages, V_{SSA}/V_{REFL} and V_{DDA}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.

Figure 1. MC9S08QE8 Series Block Diagram

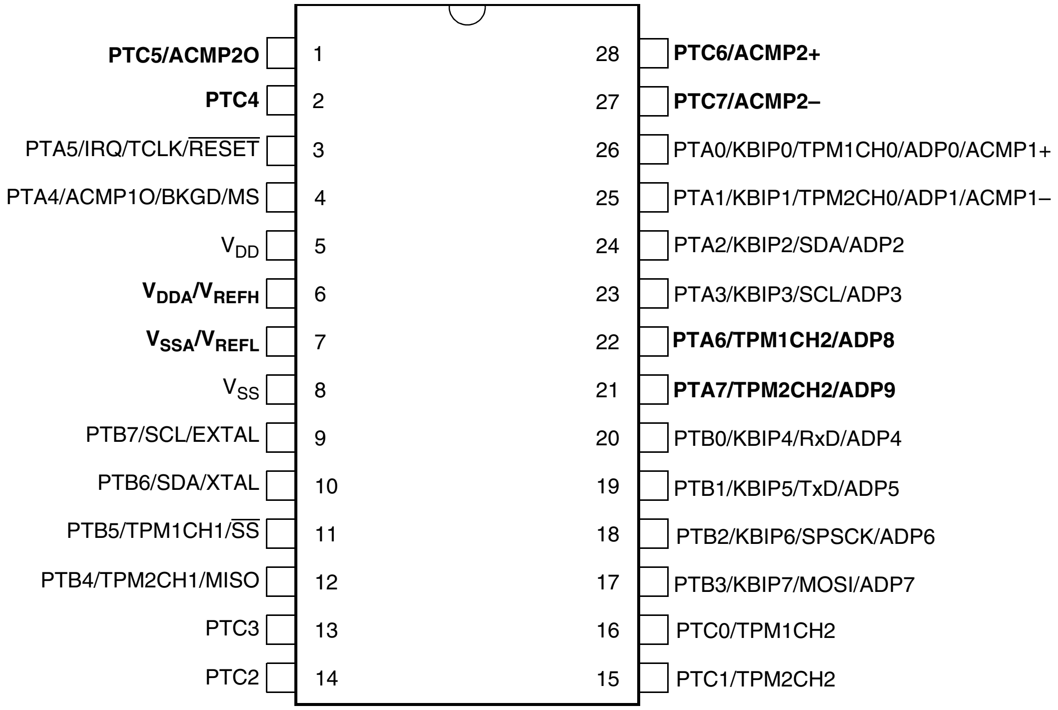
2 Pin Assignments

This section shows the pin assignments for the MC9S08QE8 series devices.



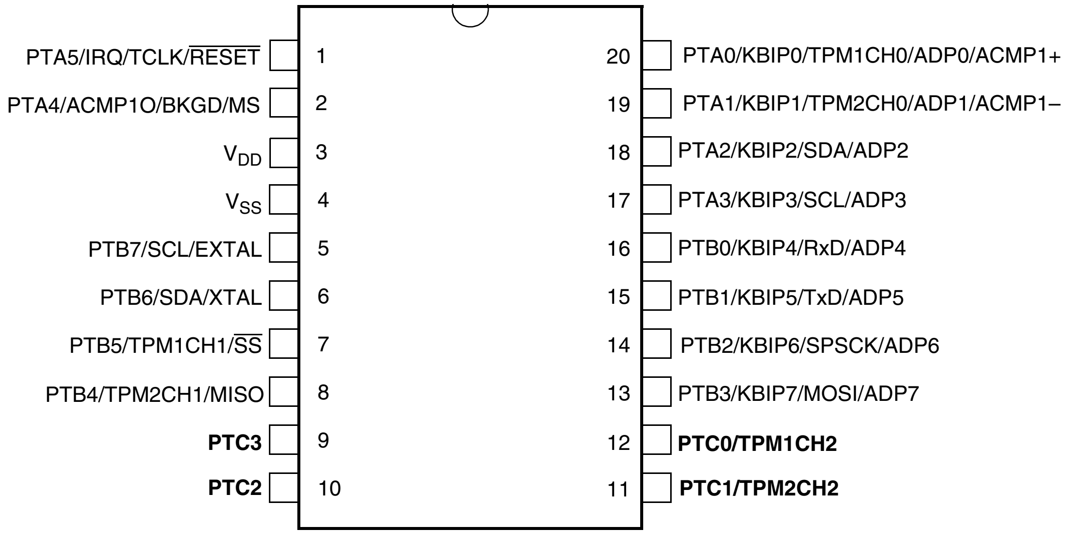
Pins shown in bold type are lost in the next lower pin count package.

Figure 2. MC9S08QE8 Series in 32-Pin LQFP Package



Pins shown in bold type are lost in the next lower pin count package.

Figure 3. MC9S08QE8 Series in 28-pin SOIC Package



Pins shown in bold type are lost in the next lower pin count package.

Figure 4. MC9S08QE8 Series in 20-pin SOIC Package

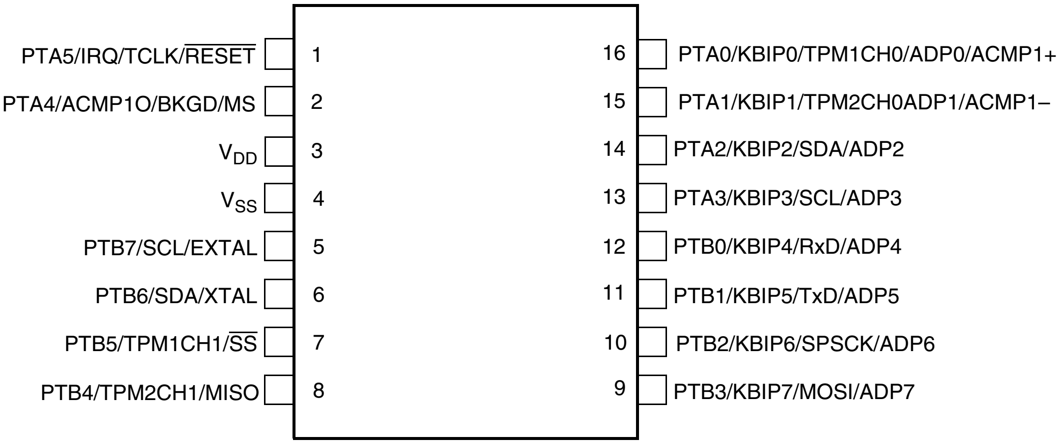


Figure 5. MC9S08QE8 Series in 16-pin PDIP and TSSOP Packages

Table 1. Pin Availability by Package Pin-Count

Pin Number				<-- Lowest **Priority** --> Highest				
32	**28**	**20**	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	—	—	—	PTD1				
2	—	—	—	PTD0				
3	5	3	3					V_{DD}
4	6	—	—					V_{DDA}/V_{REFH}
5	7	—	—					V_{SSA}/V_{REFL}
6	8	4	4					V_{SS}
7	9	5	5	PTB7	SCL[1]			EXTAL
8	10	6	6	PTB6	SDA[1]			XTAL
9	11	7	7	PTB5	TPM1CH1	$\overline{\text{SS}}$		
10	12	8	8	PTB4	TPM2CH1	MISO		
11	13	9	—	PTC3				
12	14	10	—	PTC2				
13	15	11	—	PTC1	TPM2CH2[2]			
14	16	12	—	PTC0	TPM1CH2[3]			
15	17	13	9	PTB3	KBIP7	MOSI	ADP7	
16	18	14	10	PTB2	KBIP6	SPSCK	ADP6	
17	19	15	11	PTB1	KBIP5	TxD	ADP5	
18	20	16	12	PTB0	KBIP4	RxD	ADP4	
19	21	—	—	PTA7	TPM2CH2[2]		ADP9	
20	22	—	—	PTA6	TPM1CH2[3]		ADP8	
21	—	—	—	PTD3				
22	—	—	—	PTD2				
23	23	17	13	PTA3	KBIP3	SCL[1]	ADP3	
24	24	18	14	PTA2	KBIP2	SDA[1]	ADP2	
25	25	19	15	PTA1	KBIP1	TPM2CH0	ADP1[4]	ACMP1–[4]

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number				<-- Lowest **Priority** --> Highest				
32	**28**	**20**	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
26	26	20	16	PTA0	KBIP0	TPM1CH0	ADP0[4]	ACMP1+[4]
27	27	—	—	PTC7				ACMP2–
28	28	—	—	PTC6				ACMP2+
29	1	—	—	PTC5				ACMP2O
30	2	—	—	PTC4				
31	3	1	1	PTA5	IRQ	TCLK	$\overline{\text{RESET}}$	
32	4	2	2	PTA4	ACMP1O	BKGD	MS	

[1] IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2, default reset locations are PTA3 and PTA2.

[2] TPM2CH2 pin can be repositioned using TPM2CH2PS in SOPT2, default reset location is PTA7.

[3] TPM1CH2 pin can be repositioned using TPM1CH2PS in SOPT2, default reset location is PTA6.

[4] If ADC and ACMP1 are enabled, both modules will have access to the pin.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance Single-layer board			
32-pin LQFP	θ_{JA}	66	°C/W
28-pin SOIC		57	
20-pin SOIC		71	
16-pin PDIP		64	
16-pin TSSOP		108	
Thermal resistance Four-layer board			
32-pin LQFP	θ_{JA}	47	°C/W
28-pin SOIC		42	
20-pin SOIC		52	
16-pin PDIP		47	
16-pin TSSOP		78	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min.	Typical[1]	Max.	Unit
1		Operating voltage V_{DD} rising V_{DD} falling				2.0[2] 1.8		3.6	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage	All digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 × V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 × V_{DD}	—	—	
7	P	Input low voltage	All digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 × V_{DD}	
	C				V_{DD} > 1.8 V	—	—	0.30 × V_{DD}	
8	C	Input hysteresis	All digital inputs	V_{hys}	—	0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	All input only pins (per pin)	$\|I_{In}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
10	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$\|I_{OZ}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
11	P	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$\|I_{OZTOT}\|$	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
12a	P	Pullup, pulldown resistors	All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/$\overline{\text{RESET}}$	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ

Table 7. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min.	Typical[1]	Max.	Unit
12b	C	Pullup, pulldown resistors	(PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD} (Note[3])	—	17.5	—	52.5	kΩ
13	C	DC injection current[4, 5, 6]	Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
14	C	Input capacitance, all pins		C_{In}	—	—	—	8	pF
15	C	RAM retention voltage		V_{RAM}	—	—	0.6	1.0	V
16	C	POR re-arm voltage[7]		V_{POR}	—	0.9	1.4	2.0	V
17	D	POR re-arm time		t_{POR}	—	10	—	—	μs
18	P	Low-voltage detection threshold		V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V
19	P	Low-voltage warning threshold		V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.24	V
20	P	Low-voltage inhibit reset/recover hysteresis		V_{hys}	—	—	80	—	mV
21	P	Bandgap voltage reference[8]		V_{BG}	—	1.15	1.17	1.18	V

[1] Typical values are measured at 25 °C. Characterized, not tested

[2] As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

[3] The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear higher when measured externally on the pin.

[4] All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

[5] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[6] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[7] Maximum is highest voltage that POR is guaranteed.

[8] Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

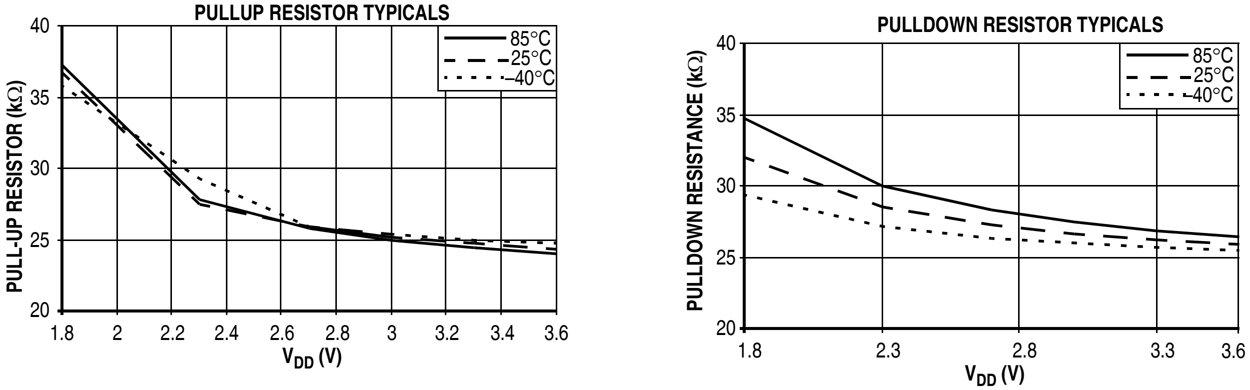


Figure 6. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

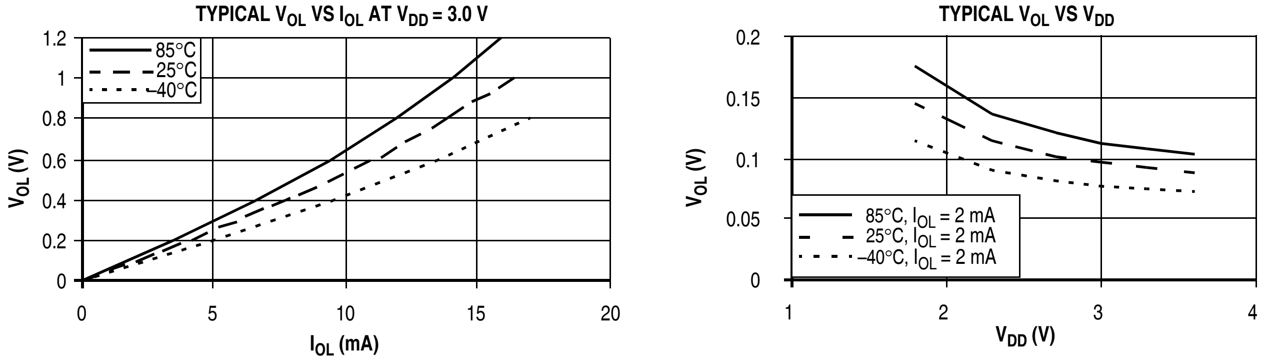


Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

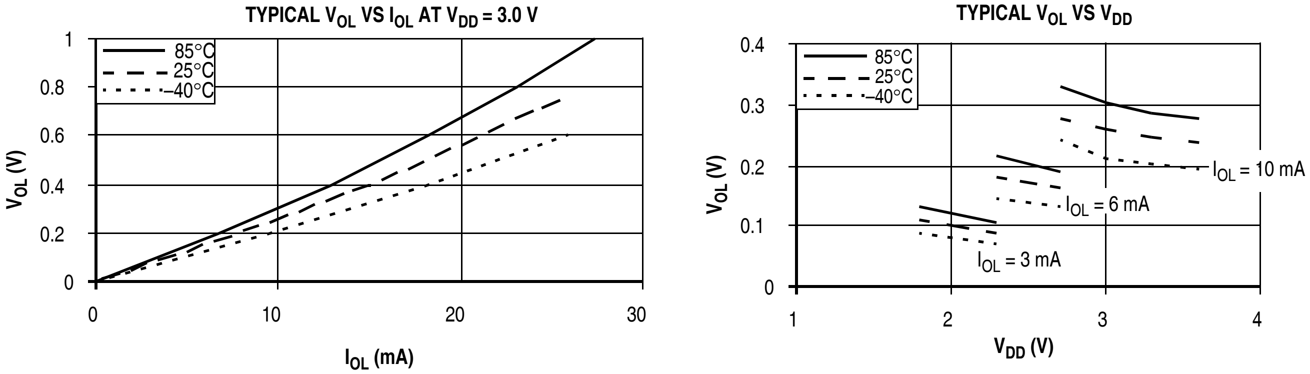


Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

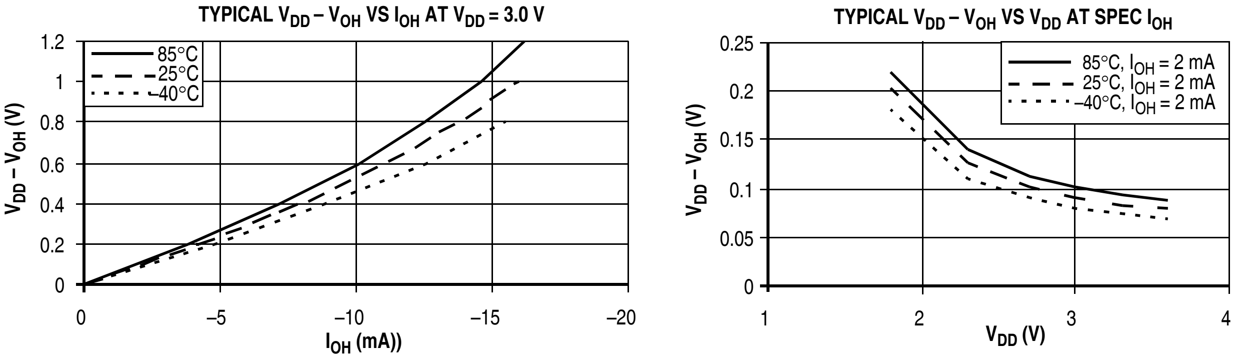


Figure 9. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

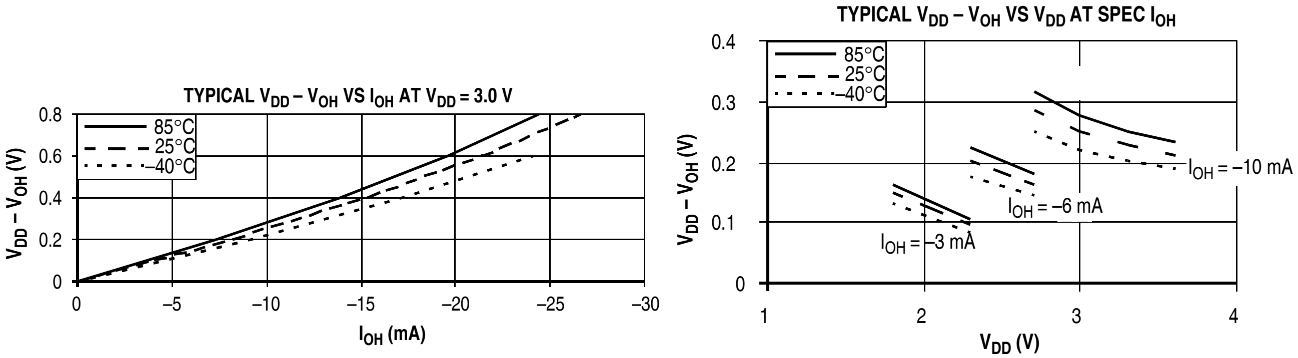


Figure 10. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	10 MHz	3	5.60	8.2	mA	–40 to 85 °C
	T			1 MHz		0.80	—		
2	T	Run supply current FEI mode, all modules off	RI_{DD}	10 MHz	3	3.60	—	mA	–40 to 85 °C
	T			1 MHz		0.51	—		
3	T	Run supply current LPRS = 0, all modules off	RI_{DD}	16 kHz FBILP	3	165	—	µA	–40 to 85 °C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS = 1, all modules off; running from flash	RI_{DD}	16 kHz FBILP	3	77	—	µA	–40 to 85 °C
	T			16 kHz FBELP		21	—		

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
5	T	Run supply current LPRS = 1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	77	—	μA	–40 to 85 °C
	T			16 kHz FBELP		7.3	—		
6	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	10 MHz	3	570	—	μA	–40 to 85 °C
	T			1 MHz		290	—		
7	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBELP	3	1	—	μA	–40 to 85 °C
8	P	Stop2 mode supply current	$S2I_{DD}$	—	3	0.3	0.65	μA	–40 to 25 °C
	C			—		0.5	0.8		70 °C
	P			—		1	2.5		85 °C
	C			—	2	0.25	0.50		–40 to 25 °C
	C			—		0.3	0.6		70 °C
	C			—		0.7	2.0		85 °C
9	P	Stop3 mode supply current no clocks active	$S3I_{DD}$	—	3	0.4	0.8	μA	–40 to 25 °C
	C			—		1.0	1.8		70 °C
	P			—		3	6		85 °C
	C			—	2	0.35	0.60		–40 to 25 °C
	C			—		0.8	1.5		70 °C
	C			—		2.5	5.5		85 °C

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	**25**°C	**70**°C	**85**°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]	—	63	70	77	81	μA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	μA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	22	23	μA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	μA

[1] Not available in stop2 mode.

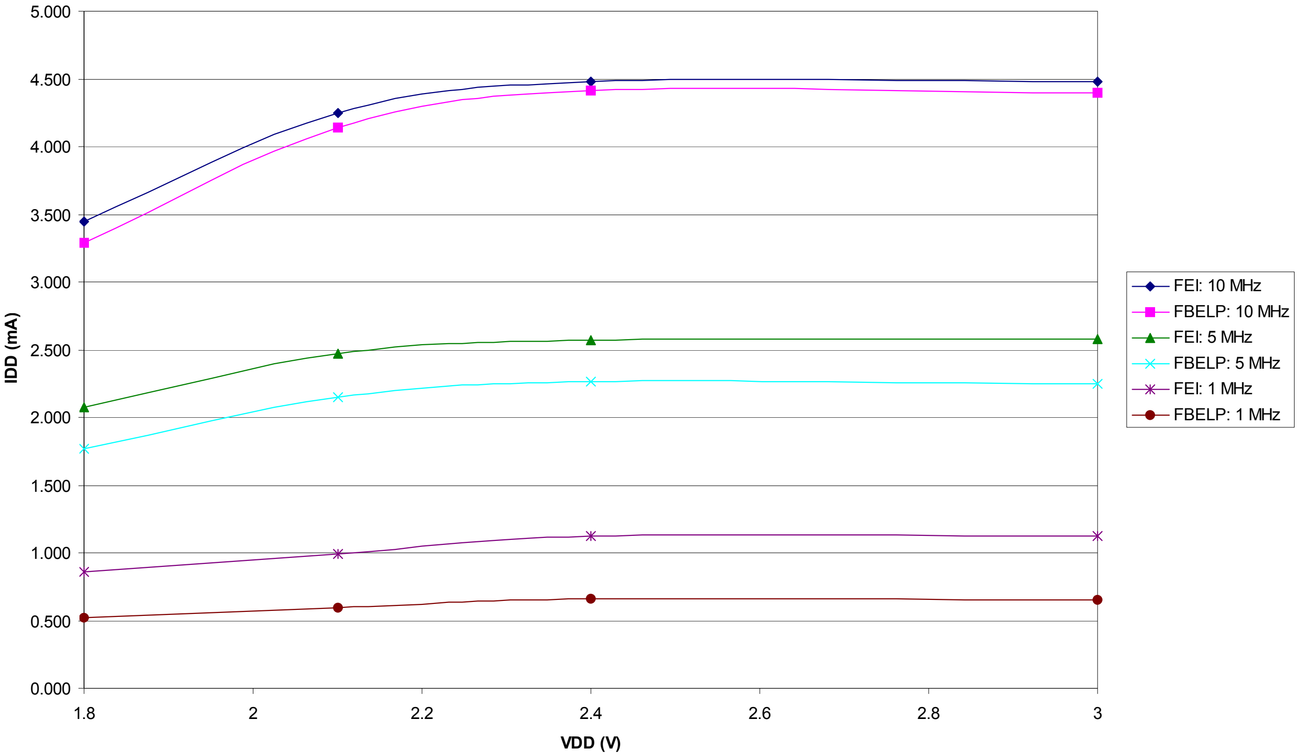


Figure 11. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD}
(ADC off, All Other Modules Enabled)

3.8 External Oscillator (XOSCVLP) Characteristics

Refer to Figure 12 and Figure 13 for crystal or resonator circuits.

Table 10. XOSCVLP Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1), FBELP mode High range (RANGE = 1), low power (HGO = 0), FBELP mode	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO = 0) Other oscillator settings	C_1,C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time[4] Low range, low power Low range, high gain High range, low power High range, high gain	t_{CSTL} t_{CSTH}	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

---

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

[2] Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.

[3] See crystal or resonator manufacturer's recommendation.

[4] Proper PC board layout procedures must be followed to achieve specifications.

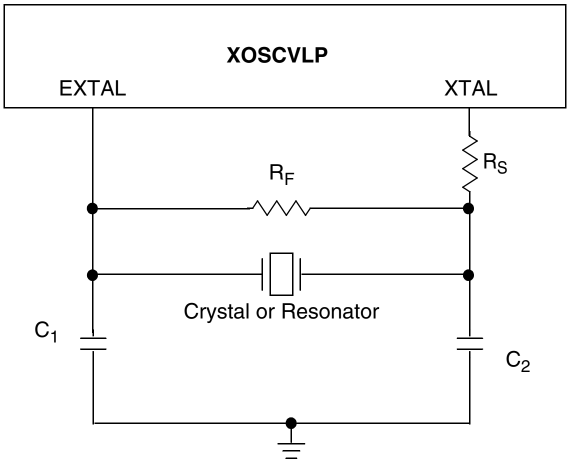


Figure 12. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

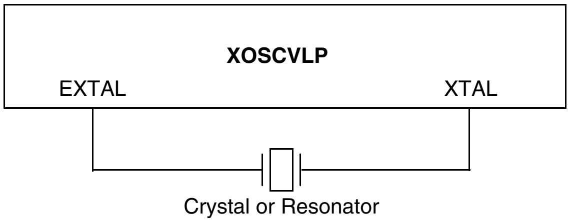


Figure 13. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min.	Typical[1]	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25 °C		f_{int_t}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	5	10	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1		f_{dco_DMX32}	—	19.92	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation of DCO output from trimmed frequency[3] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	± 2 ± 1	$\%f_{dco}$
10	C	FLL acquisition time[4]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[5]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

[2] The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

[3] This parameter is characterized and not tested on each device.

[4] This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[5] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

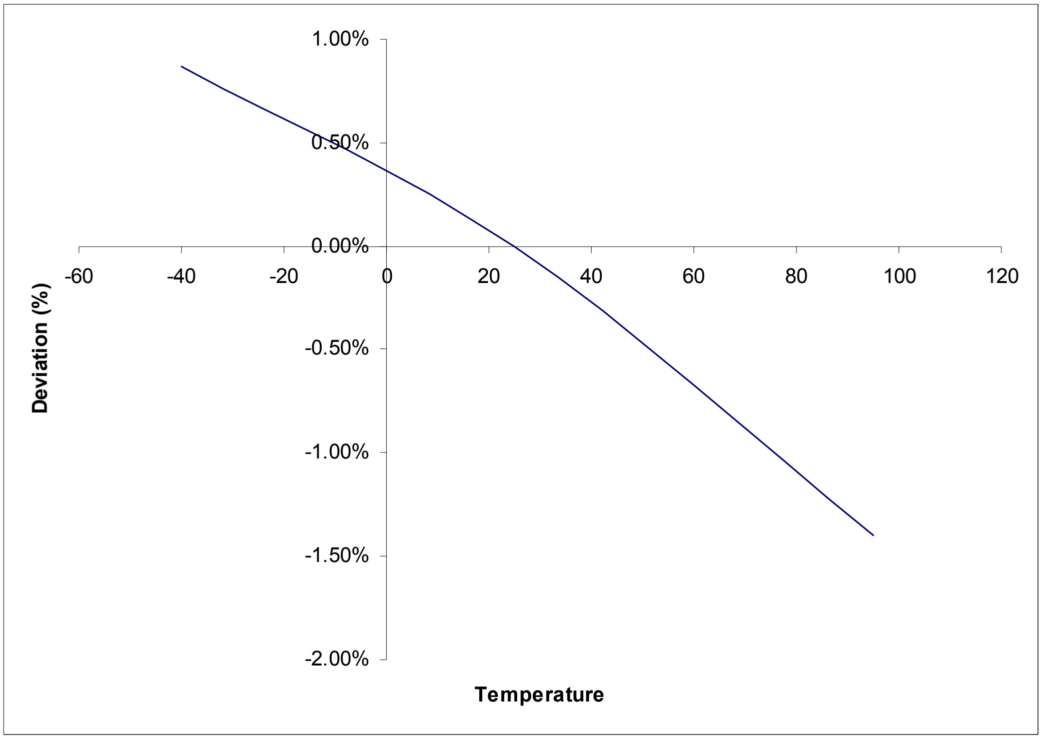


Figure 14. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 $1.5 \times t_{cyc}$	 — —	 — —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage regulator recovery time	t_{VRR}	—	4	—	μs

[1] Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

[3] To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

[4] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

[5] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

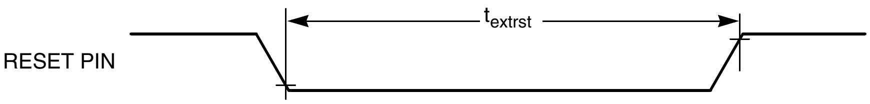


Figure 15. Reset Timing

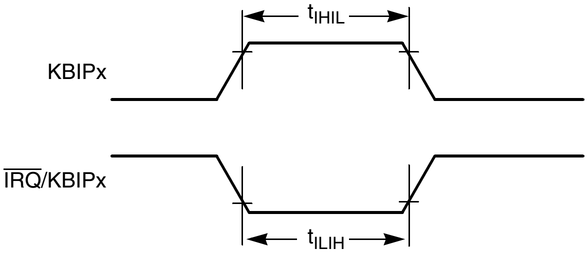


Figure 16. $\overline{\text{IRQ}}$/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

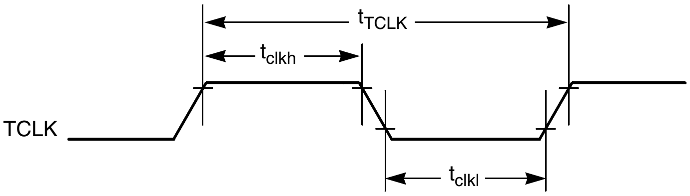


Figure 17. Timer External Clock

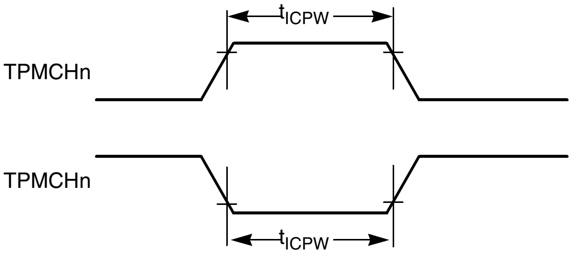


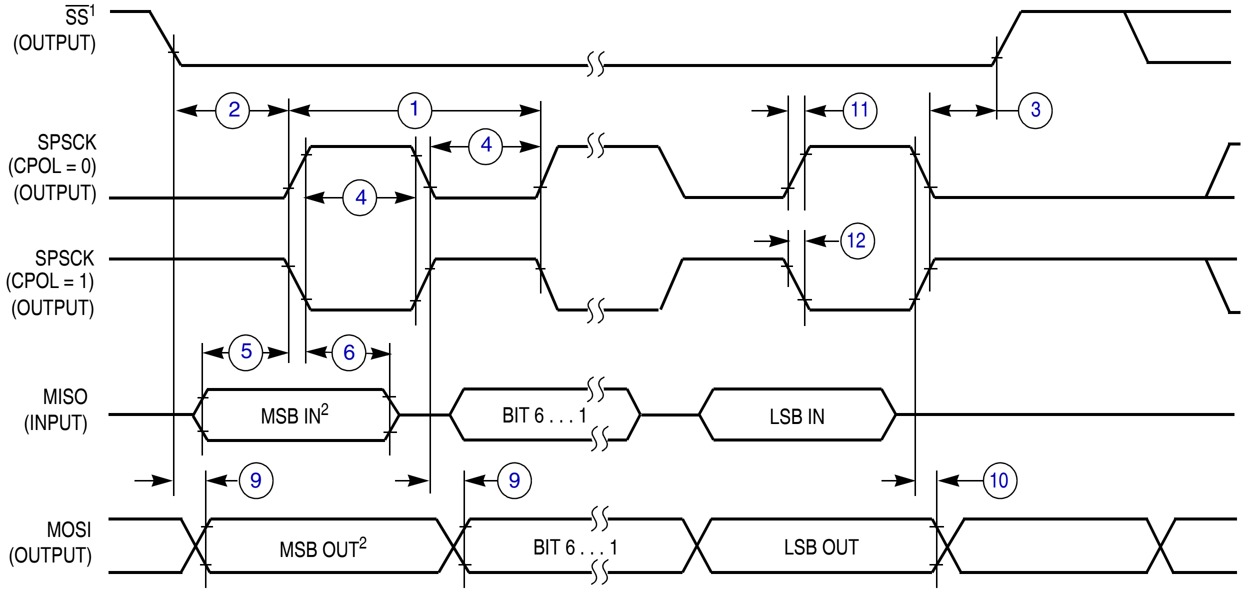
Figure 18. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 14 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

Table 14. SPI Timing

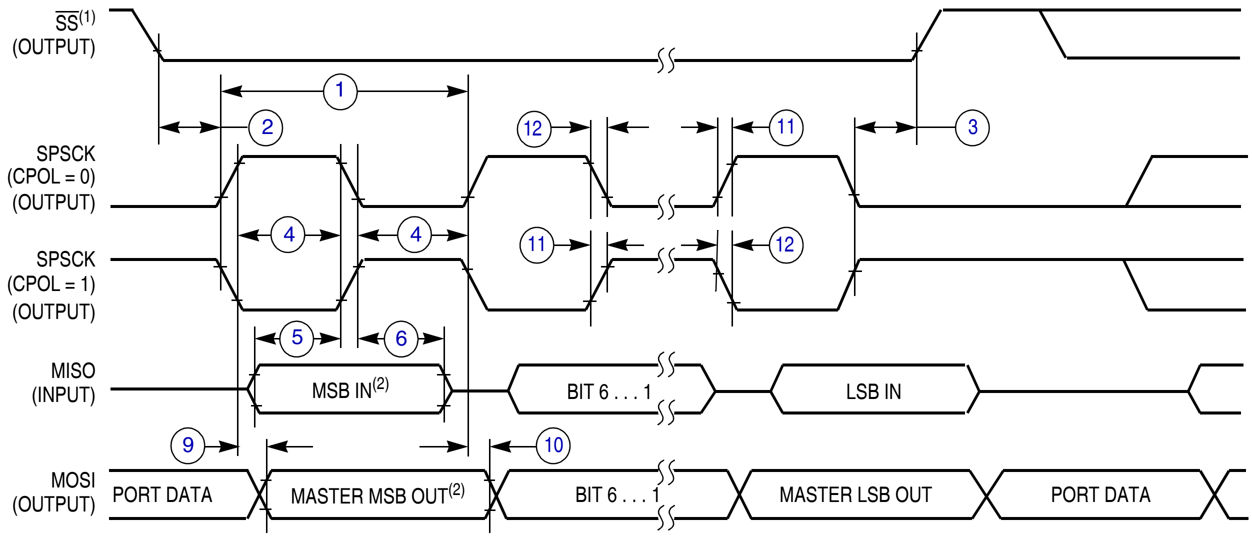
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

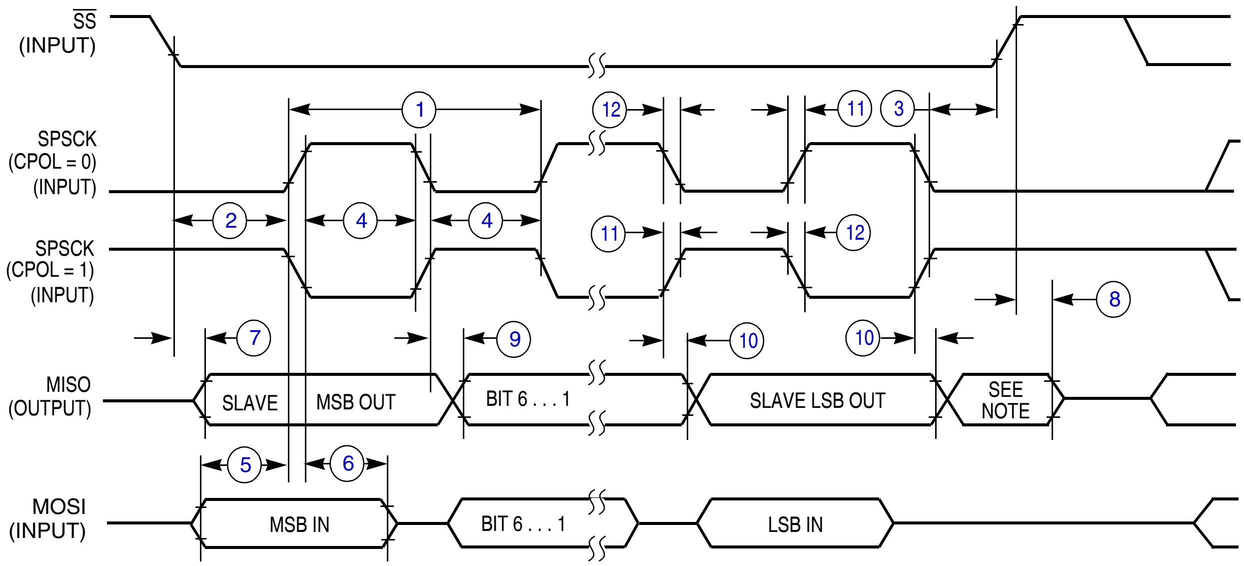
Figure 19. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

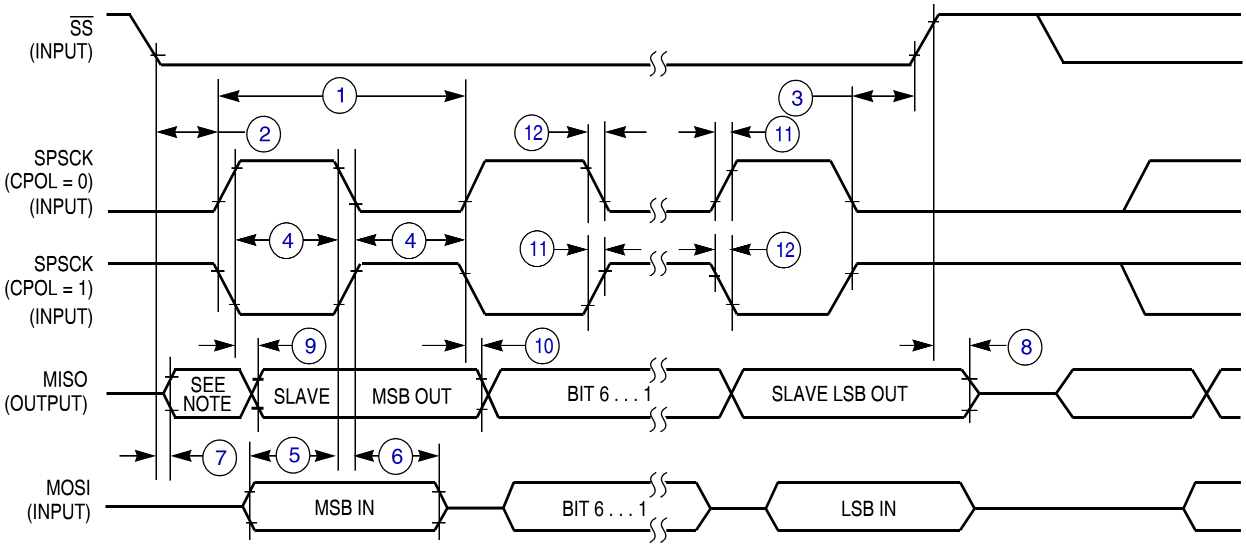
Figure 20. SPI Master Timing (CPHA =1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 21. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 22. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	µA

Table 15. Analog Comparator Electrical Specifications (continued)

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

3.12 ADC Characteristics

Table 16. 12-Bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	—
	Delta to V_{DD} ($V_{DD} - V_{DDA}$)[2]	ΔV_{DDA}	–100	0	100	mV	—
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)[2]	ΔV_{SSA}	–100	0	100	mV	—
Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
Input resistance	—	R_{ADIN}	—	5	7	kΩ	—
Analog source resistance	12-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz		 — —	 — —	 5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock freq.	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC = 1)		0.4	—	4.0		

[1] Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

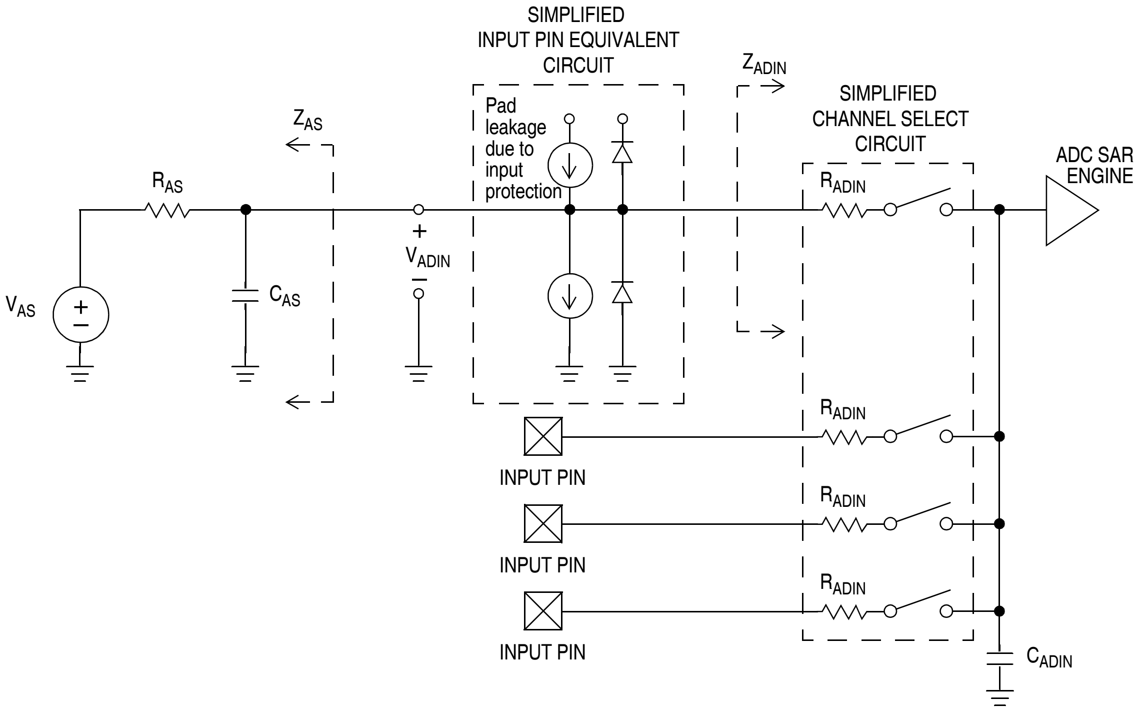


Figure 23. ADC Input Impedance Equivalency Diagram

Table 17. ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	120	—	μA	
T	Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDA}	—	202	—	μA	
T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	288	—	μA	
P	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.532	1	mA	
P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low power (ADLPC = 1)		1.25	2	3.3		

Table 17. ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See QE8 reference manual for conversion time variances
		Long sample (ADLSMP = 1)		—	40	—		
P	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long sample (ADLSMP = 1)		—	23.5	—		
D	Temp sensor slope	–40 °C– 25 °C	m	—	1.646	—	mV/°C	
		25 °C– 85 °C		—	1.769	—		
D	Temp sensor voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	
Characteristics for devices with dedicated analog supply (28- and 32-pin packages only)								
T	Total unadjusted error	12-bit mode, 3.6> V_{DDA} > 2.7	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
T		12-bit mode, 2.7> V_{DDA} > 1.8V		—	–1 to 3	–3.0 to 6.5		
P		10-bit mode		—	±1	±2.5		
P		8-bit mode		—	±0.5	±1.0		
T	Differential non-linearity	12-bit mode	DNL	—	±1.0	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	12-bit mode	INL	—	±1.5	–2.5 to 2.75	LSB[2]	
T		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		
T	Zero-scale error	12-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
P		10-bit mode		—	±0.5	±1.5		
P		8-bit mode		—	±0.5	±0.5		
T	Full-scale error	12-bit mode	E_{FS}	—	±1.0	–3.5 to 1.0	LSB[2]	$V_{ADIN} = V_{DDA}$
P		10-bit mode		—	±0.5	±1		
P		8-bit mode		—	±0.5	±0.5		
D	Quantization error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		

Table 17. ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
D	Input leakage error	12-bit mode	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		
Characteristics for devices with shared supply (16- and 20-pin packages only)								
T	Total unadjusted error	12-bit mode	E_{TUE}	Not recommended usage			LSB[2]	Includes quantization
P		10-bit mode		—	±1.5	±3.5		
P		8-bit mode		—	±0.7	±1.5		
T	Differential non-linearity	12-bit mode	DNL	Not recommended usage			LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	12-bit mode	INL	Not recommended usage			LSB[2]	
T		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		
T	Zero-scale error	12-bit mode	E_{ZS}	Not recommended usage			LSB[2]	$V_{ADIN} = V_{SSA}$
P		10-bit mode		—	±1.5	±2.1		
P		8-bit mode		—	±0.5	±0.7		
T	Full-scale error	12-bit mode	E_{FS}	Not recommended usage			LSB[2]	$V_{ADIN} = V_{DDA}$
P		10-bit mode		—	±1	±1.5		
P		8-bit mode		—	±0.5	±0.5		
D	Quantization error	12-bit mode	E_Q	Not recommended usage			LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		
D	Input leakage error	12-bit mode	E_{IL}	Not recommended usage			LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		

[1] Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

[3] Monotonicity and No-missing-codes guaranteed in 10-bit and 8-bit modes

[4] Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
P	Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
	Byte program current[3]	RI_{DDBP}	—	4	—	mA
	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

[1] The frequency of this clock is controlled by a software setting.

[2] These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

[3] The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

[4] **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

[5] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology is based on IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below Table 19.

Table 19. Conducted Susceptibility, EFT/B

Parameter	Symbol	Conditions	f_{OSC}/f_{BUS}	Result	Amplitude[1] (Min)	Unit
Conducted susceptibility, electrical fast transient/burst (EFT/B)	V_{CS_EFT}	V_{DD} = 3.3 V T_A = 25 ^oC package type 32-pin LQFP	8 MHz crystal 8 MHz bus	A	2.3	kV
				B	4.0	
				C	>4.0	
				D	>4.0	

[1] Data based on qualification test results. Not tested in production.

The susceptibility performance classification is described in Table 20.

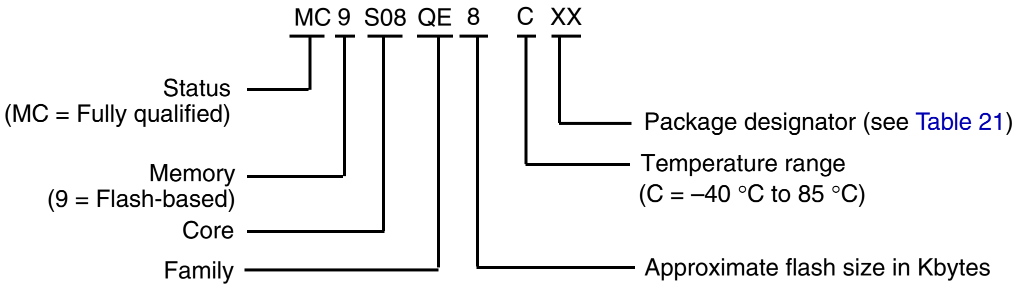
Table 20. Susceptibility Performance Classification

Result	Performance Criteria	
A	No failure	The MCU performs as designed during and after exposure.
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the $\overline{\text{RESET}}$ pin is asserted.
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.

4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



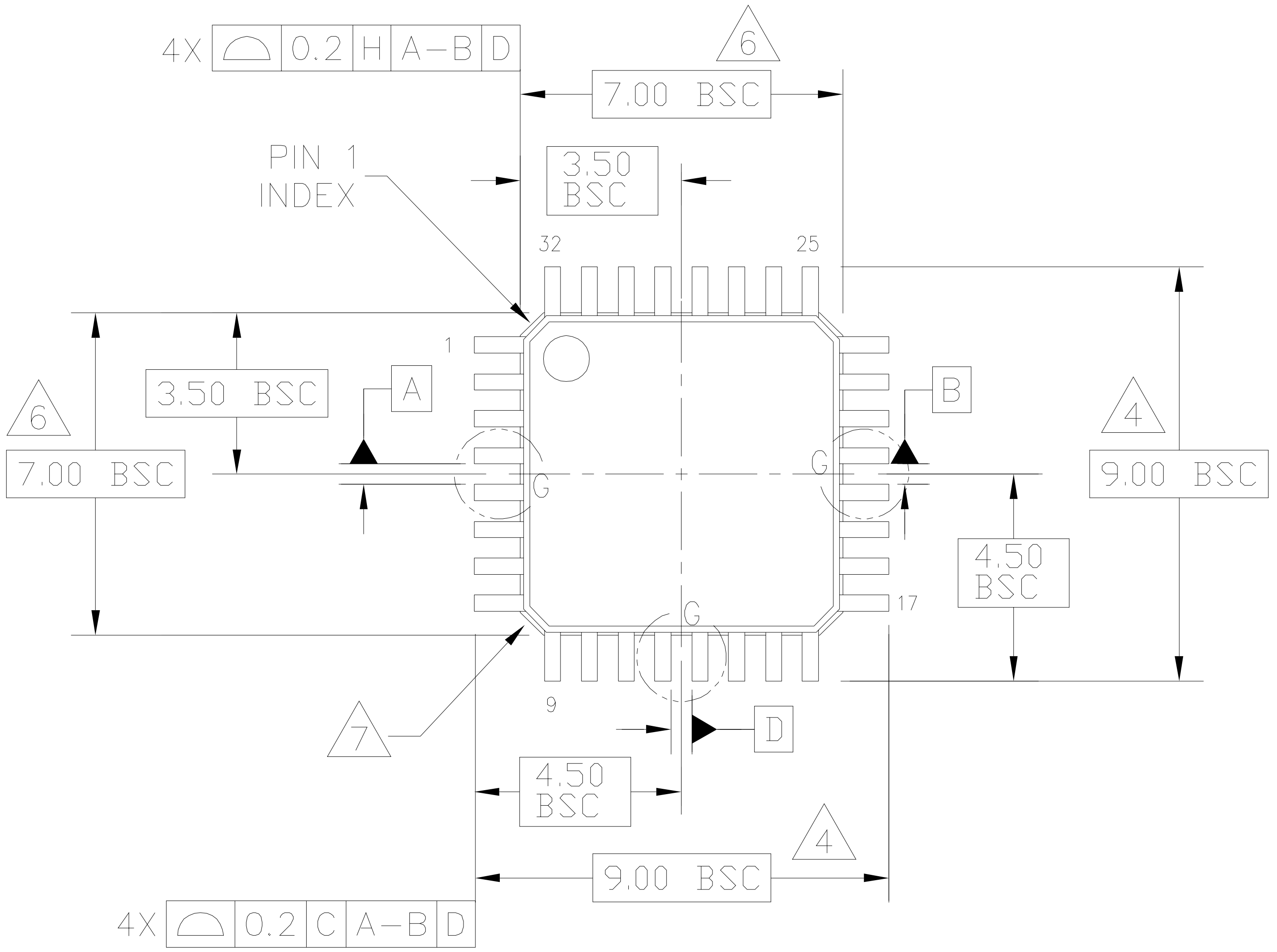
5 Package Information

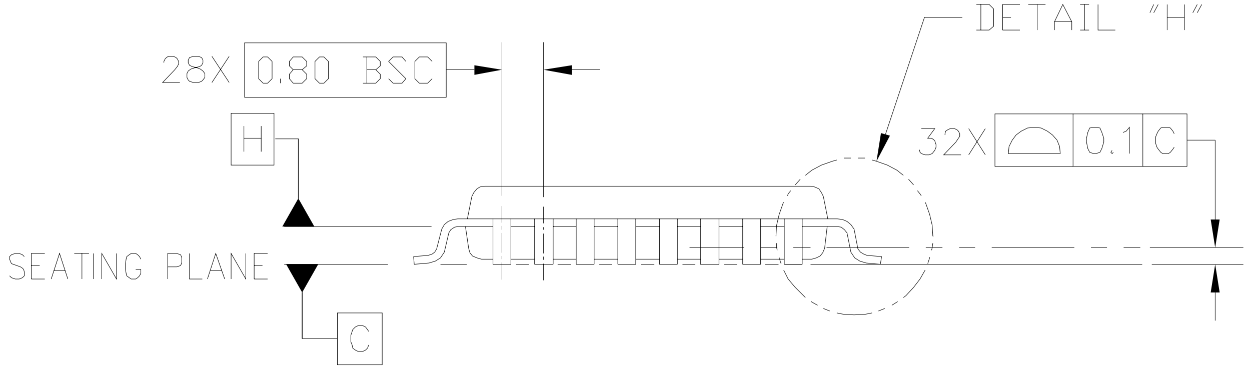
Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
20	Small Outline Integrated Circuit	SOIC	WJ	751D	98ASB42343B
16	Plastic Dual In-line Package	PDIP	PG	648	98ASB42431B
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 21.





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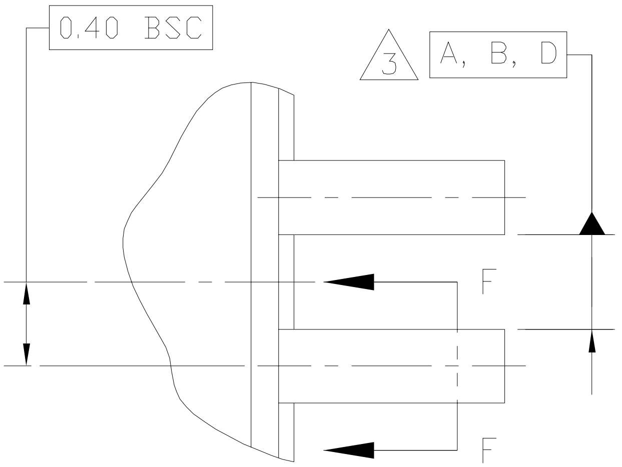
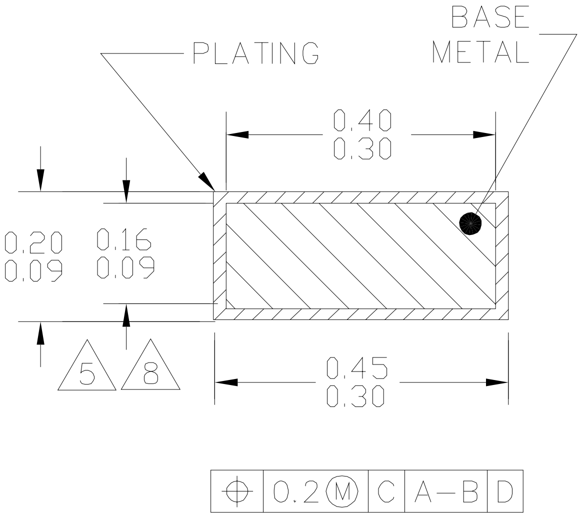
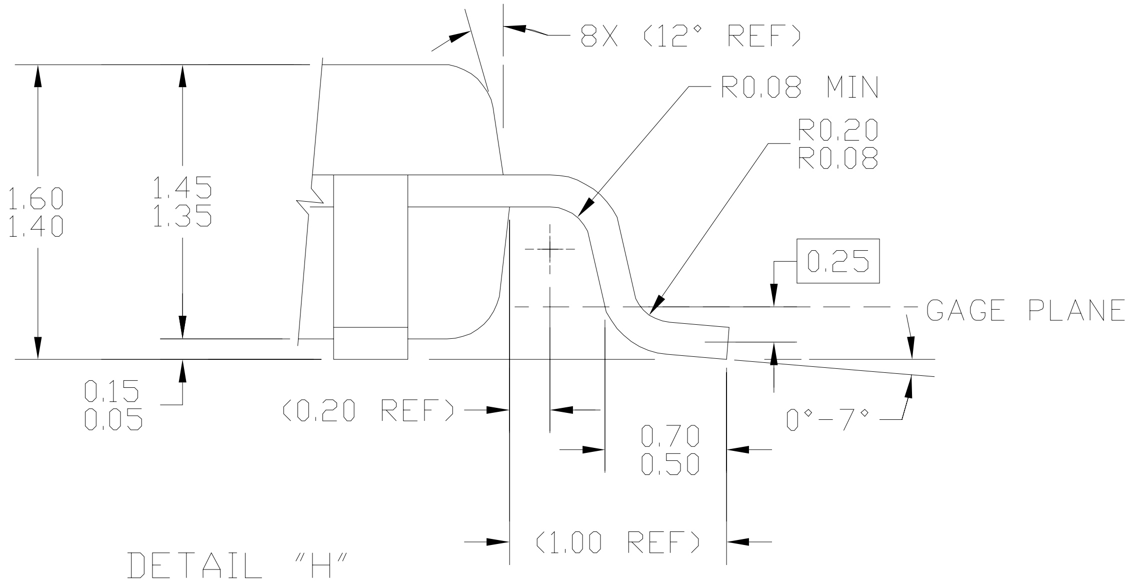
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	



DETAIL G



SECTION F–F
ROTATED 90°CW
32 PLACES



DETAIL "H"

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TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5—1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

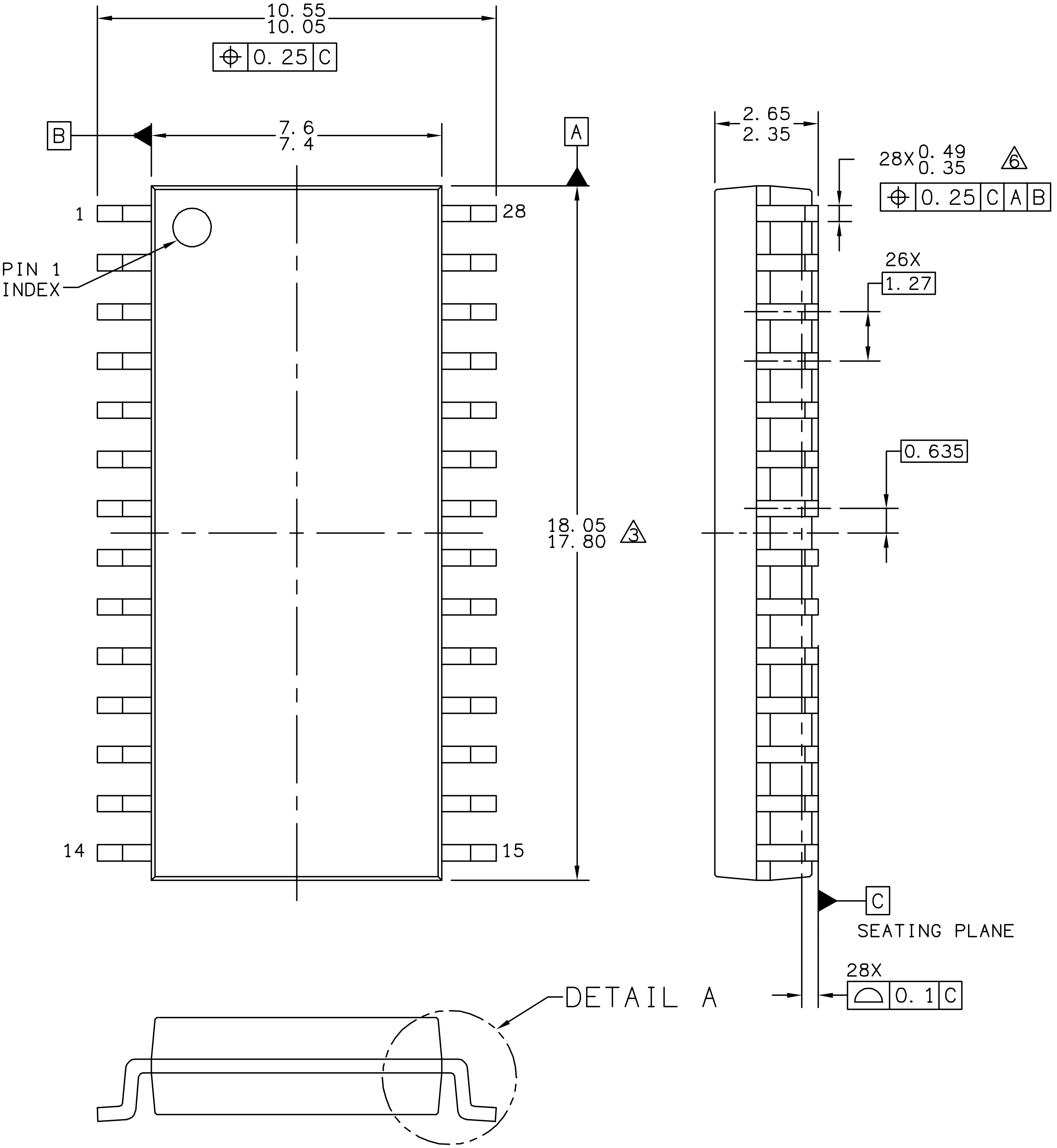
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

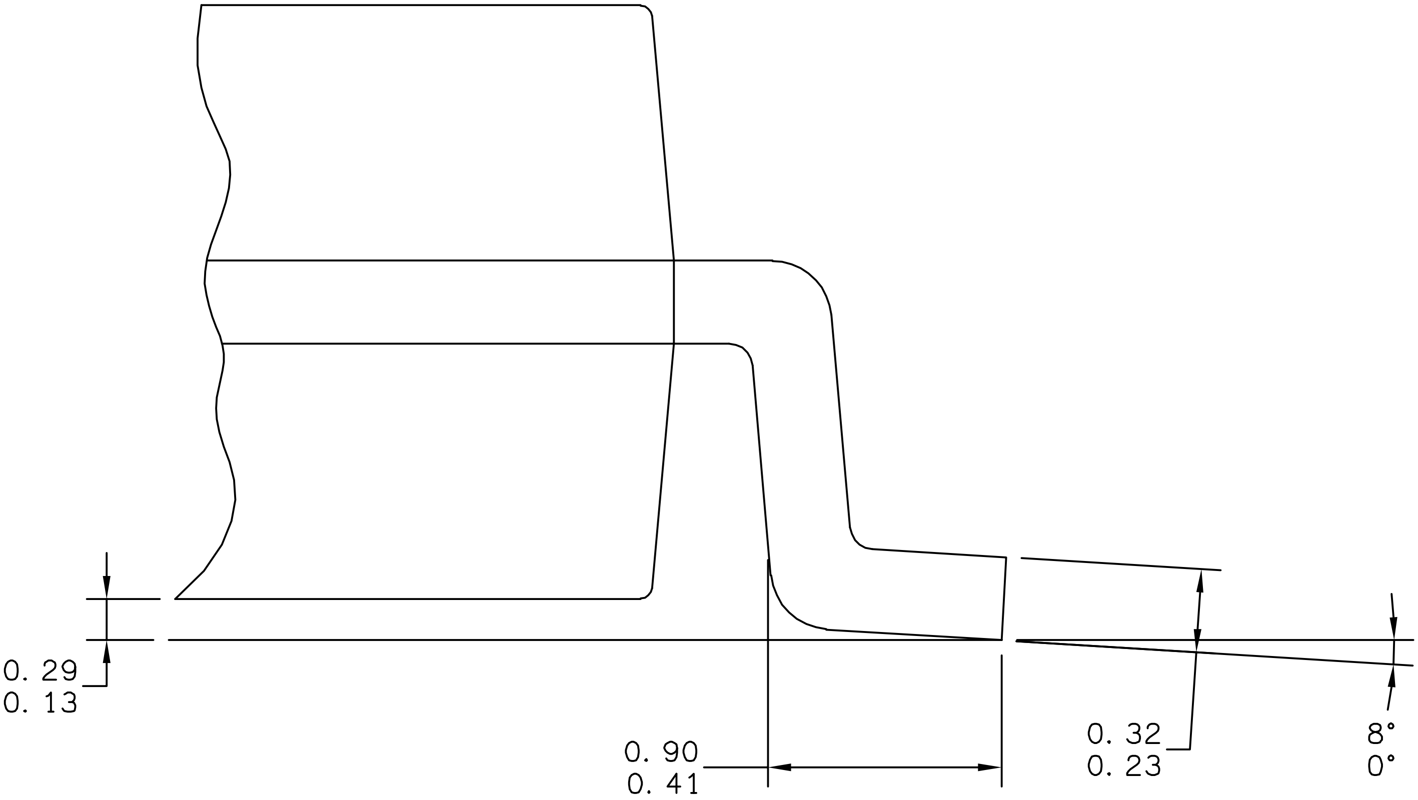
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BB	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	



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TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

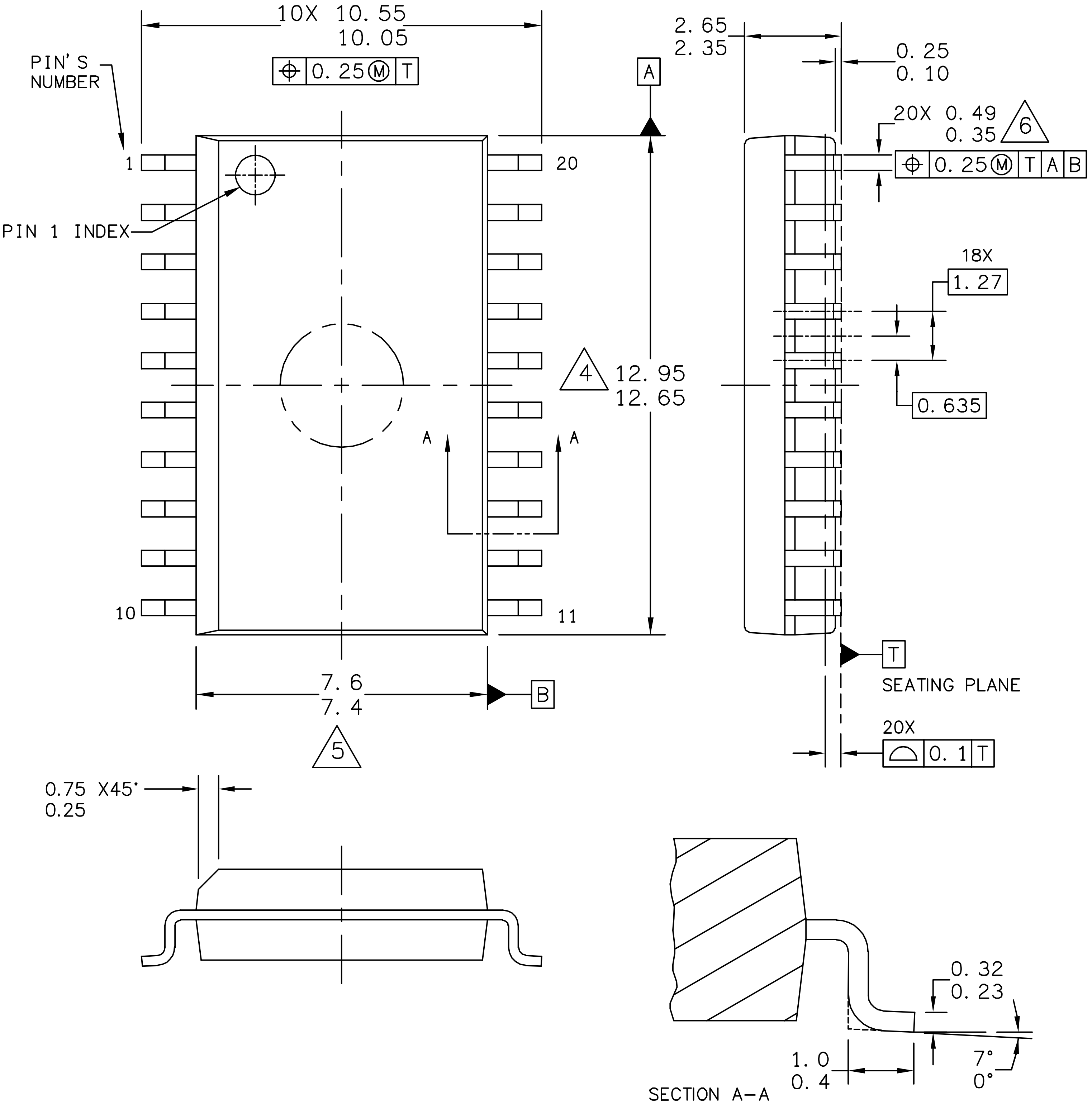
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

△3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05

△5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F–05	10 MAR 2005
	STANDARD: MS–013AE	



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TITLE: 20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42343B	REV: J
	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

△4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

△5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

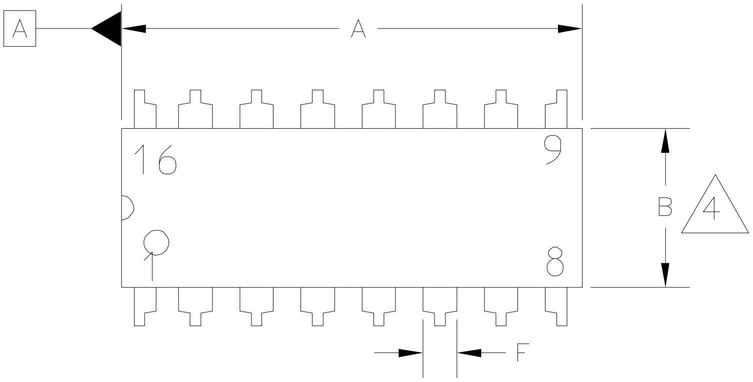
△6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

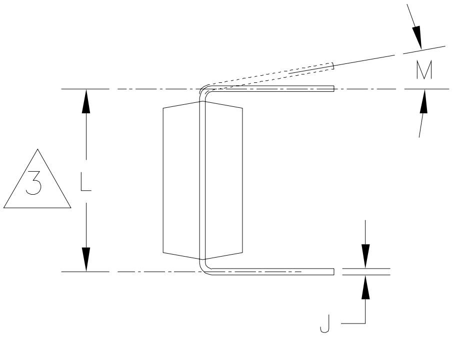
MECHANICAL OUTLINE

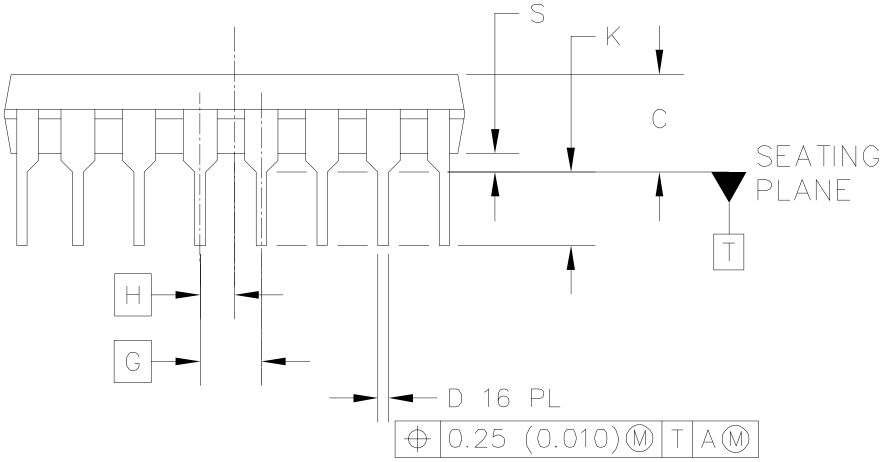
PRINT VERSION NOT TO SCALE

TITLE:
20LD SOIC W/B, 1.27 PITCH,
CASE OUTLINE

DOCUMENT NO: 98ASB42343B
REV: J
CASE NUMBER: 751D-07
23 MAR 2005
STANDARD: JEDEC MS-013AC







MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

16 LD PDIP

DOCUMENT NO: 98ASB42431B

REV: T

CASE NUMBER: 648-08

19 MAY 2005

STANDARD: NON-JEDEC

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -08 OBSOLETE, NEW STANDARD 648-09.

	MILLIMETERS		INCHES			MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770					
B	6.35	6.85	0.250	0.270					
C	3.69	4.44	0.145	0.175					
D	0.39	0.53	0.015	0.021					
F	1.02	1.77	0.040	0.070					
G	2.54 BSC		0.100 BSC						
H	1.27 BSC		0.050 BSC						
J	0.21	0.38	0.008	0.015					
K	2.80	3.30	0.110	0.130					
L	7.50	7.74	0.295	0.305					
M	0°	10°	0°	10°					
S	0.51	1.01	0.020	0.040					

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:
16 LD PDIP

DOCUMENT NO: 98ASB42431B
REV: T
CASE NUMBER: 648-08
19 MAY 2005
STANDARD: NON-JEDEC

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:
16 LD PDIP

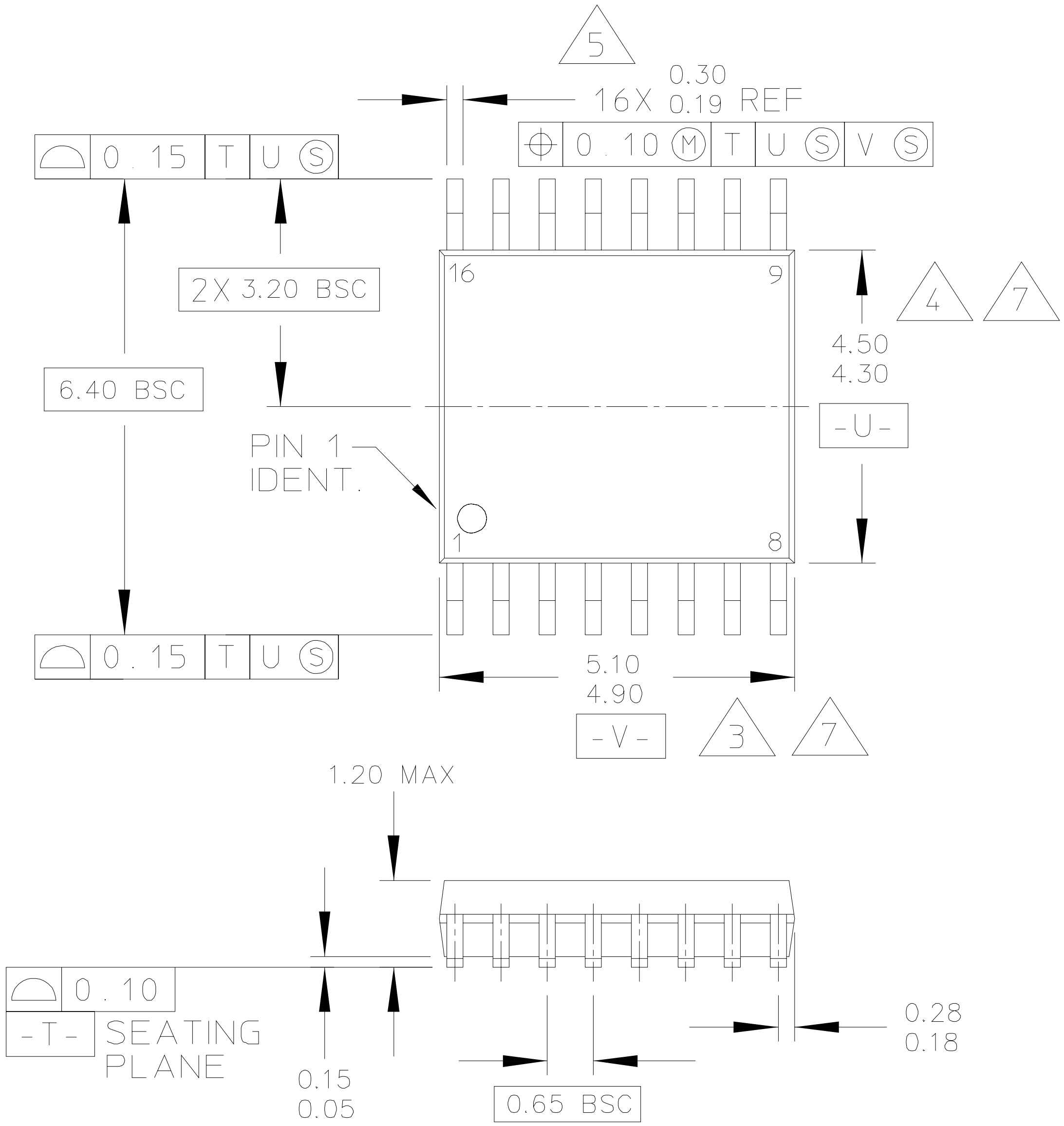
DOCUMENT NO: 98ASB42431B

REV: T

CASE NUMBER: 648-08

19 MAY 2005

STANDARD: NON-JEDEC



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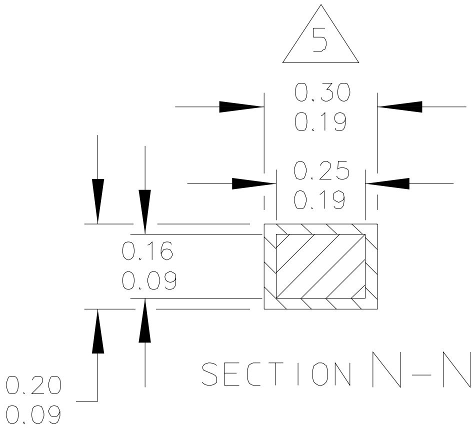
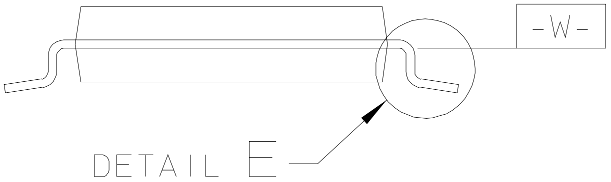
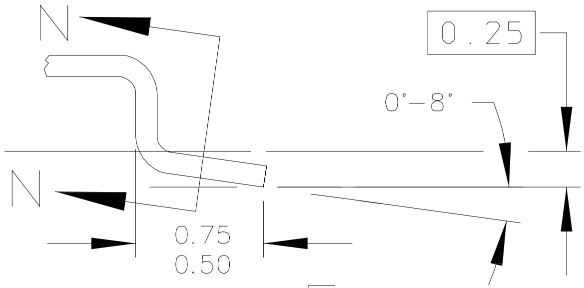
TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	



SECTION N-N





DETAIL E

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TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:

16 LD TSSOP, PITCH 0.65MM

DOCUMENT NO: 98ASH70247A

REV: B

CASE NUMBER: 948F-01

19 MAY 2005

STANDARD: JEDEC

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MC9S08QE8
Rev. 7
4/2009