ABOV SEMICONDUCTOR Co., Ltd.
8-BIT MICROCONTROLLERS

MC96P0202

User's Manual (Ver. 1.1)

REVISION HISTORY

VERSION 0.0 (December 1, 2010)

VERSION 1.0 (December 31, 2010)

Change LVR's Detection Values at Low Voltage Reset characteristics

VERSION 1.1 (July 5, 2011) This book

Add Figure7.4 Recommended Circuit and Layout in Electrical Characteristics.

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Table of Contents

List of Figures

List of Tables

MC96P0202

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

1. Overview

1.1 Description

The MC96P0202 is advanced CMOS 8-bit microcontroller with 2k bytes of OTP. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 2k bytes of OTP, 72 bytes of IRAM, general purpose I/O, basic interval timer, watchdog timer, 8-bit timer/counter, carrier generation, 8-bit PWM, inverter ampilifier, 12V open-drain port, on-chip POR, LVR, on-chip oscillator and clock circuitry. The MC96P0202 also supports power saving modes to reduce power consumption.

Device Name	OTP	IRAM	I/O PORT	Package
MC96P0202D	2k bytes	72 bytes	10	16 SOPN
MC96P0202B				16 PDIP

1.2 Features

- **CPU**
  - 8 Bit CISC Core (8051 Compatible)
- **ROM(OTP) Capacity**
  - 2k Bytes
- **72 Bytes IRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 10 Ports
    (P0[7:0], P1[2:1])
  - Input only : 1 Port
    (P10)
- **Basic Interval Timer (BIT)**
  - 8Bit × 1ch
  - **Watch Dog Timer (WDT)**
  - 8Bit × 1ch
- **Timer/ Counter**
  - 8Bit × 2ch (T0/T1)
- **Carrier Generation**
  - Carrier Generation (by T1), T0 Clock source
- **PWM Generator**
  - Two 8-Bit PWM
- **Inverter Amplifier**
  - Two high-gain inverter amplifier
- **12V Open-Drain Port**
  - Two channels with 20mA
- **Power On Reset**
  - Reset release level (2.0V)
- **Low Voltage Reset**
  - 3 level detect (2.2V/ 2.3V/ 2.5V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0, EINT1, EINT2) (3)
  - Timer(0/1) (2)
  - WDT (1)
  - BIT (1)
  - PWM (1)
- **Internal RC Oscillator**
  - Internal RC frequency
    8MHz ± 5% @ VDD=2.4V~5.5V
    (T_A= -20°C ~ +50°C)
    8MHz ± 8% @ VDD=2.2V~5.5V
    (T_A= -20°C ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.2V ~ 5.5V (@1.0 ~ 4.0MHz)
  - 2.4V ~ 5.5V (@1.0 ~ 8.0MHz)
- **Minimum Instruction Execution Time**
  - 250nS (@ 8MHz system clock)
- **Operating Temperature:** – 20 ~ + 85℃
- **Package Type**
  - 16 SOPN/PDIP

1.3 Ordering Information

Table 1-1 Ordering Information of MC96P0202

Device name	ROM size	IRAM size	Package
MC96P0202D	2k bytes OTP	72 bytes	16 SOPN
MC96P0202B			16 PDIP

1.4 Development Tools

1.4.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96P0202 is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

1.4.2 OCD Emulator and Debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site.

Connection:

- DSCL (MC96P0202D-EVA pin 9)
- DSDA (MC96P0202D-EVA pin 12)

Note) Pin assignment of MC96P0202D-EVA refer to Figure 14.1.

OCD connector diagram: Connect OCD with user system

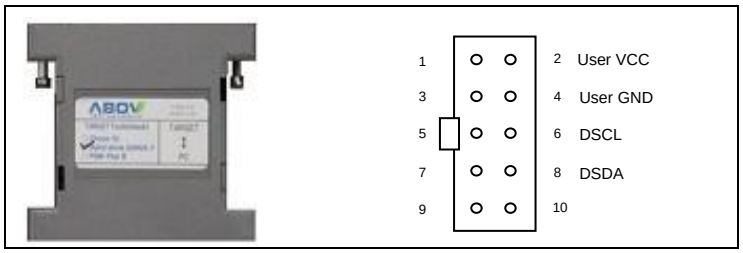


Figure 1.1 OCD Debugger and Pin Description

1.4.3 Programmer

Single programmer:

PGMplus USB: It programs MCU device directly.

Figure 1.2 PGMplusUSB (Single Writer)

StandAlone PGMplus: It programs MCU device directly.

Figure 1.3 StandAlone PGMplus (Single Writer)

OCD emulator: It can write code in MCU device too, because OCD debugging supports ISP (In System Programming).

It does not require additional H/W, except developer's target system.

Gang programmer:

It programs 8 MCU devices at once.

So, it is mainly used in mass production line.

Gang programmer is standalone type, it means it does not require host PC, after a program is downloaded from host PC to Gang programmer.

Figure 1.4 StandAlone Gang8 (for Mass Production)

1.5 OTP Progrmming

1.5.1 Overview

The program memory of MC96P0202 is OTP Type. This EPROM is accessed by serial data format. There are five pins(SCLK, SDAT, VPP, VDD, VSS) for programming/reading the EPROM.

Table 1-2 Discriptions of pins used to programming/reading the EPROM

Pin name	Pin number	During programming		Main chip pin name
		I/O	Discription	
SCLK	6	I	Serial clock pin. Input only pin.	P04
SDAT	10	I/O	Serial data pin. Output port when reading and input port when programming. Can be asigned as a input/push-pull output port.	P00
VPP	12	I	Power supply pin for EPROM cell programming (indicates that OTP enters into the programming mode). This pis is always applied with +11.5 V.	P11
VDD, VSS	13, 2	-	Logic power supply pin. VDD should be tied to +5 V during programming.	VDD, VSS

1.5.2 On Board Programming

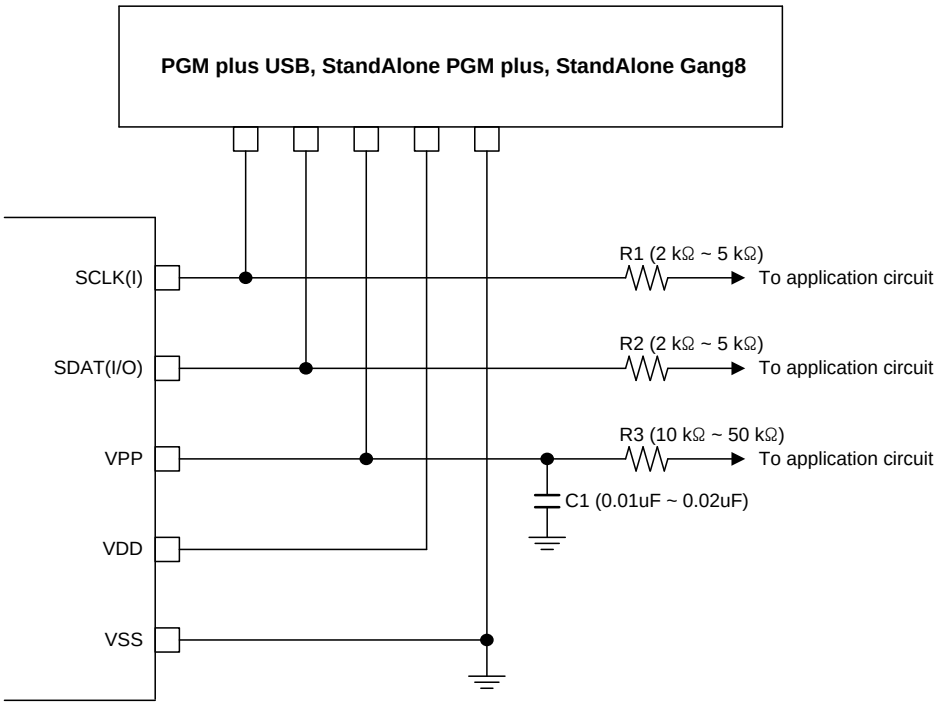
The MC96P0202 needs only five signal lines including VDD and VSS pins for programming EPROM with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.5.2.1 Circuit Design Guide

At the EPROM programming, the programming tool needs 5 signal lines that are SCLK, SDAT, VPP, VDD, and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.

In case of VPP pin when programming mode, a resistor should be inserted between the VPP pin and VSS. The SDAT and SCLK should be treated under the same consideration.

Please be careful to design the related circuit of these signal pins because rising/falling timing of VPP, SCLK and SDAT is very important for proper programming.



NOTES) 1. In on-board programming mode, very high-speed signal will be provided to pin SCLK and SDAT. And it will cause some damages to the application circuits connected to SCLK or SDAT port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of SDAT, SCLK pins had better be set to input mode.

2. C1 is used to improve the noise effect.

3. The value of R1~R3 and C is recommended value. It varies with circuit of system.

Figure 1.5 PCB Design Guide for On Board Programming

2. Block Diagram

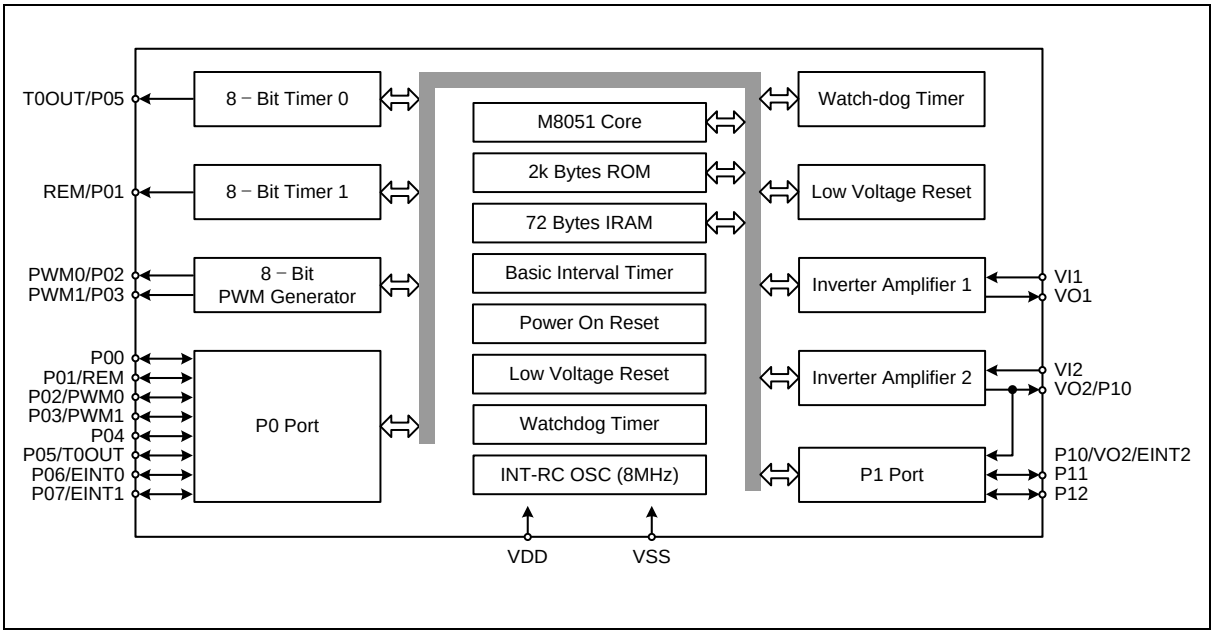


Figure 2.1 MC96P0202 Block Diagram

3. Pin Assignment

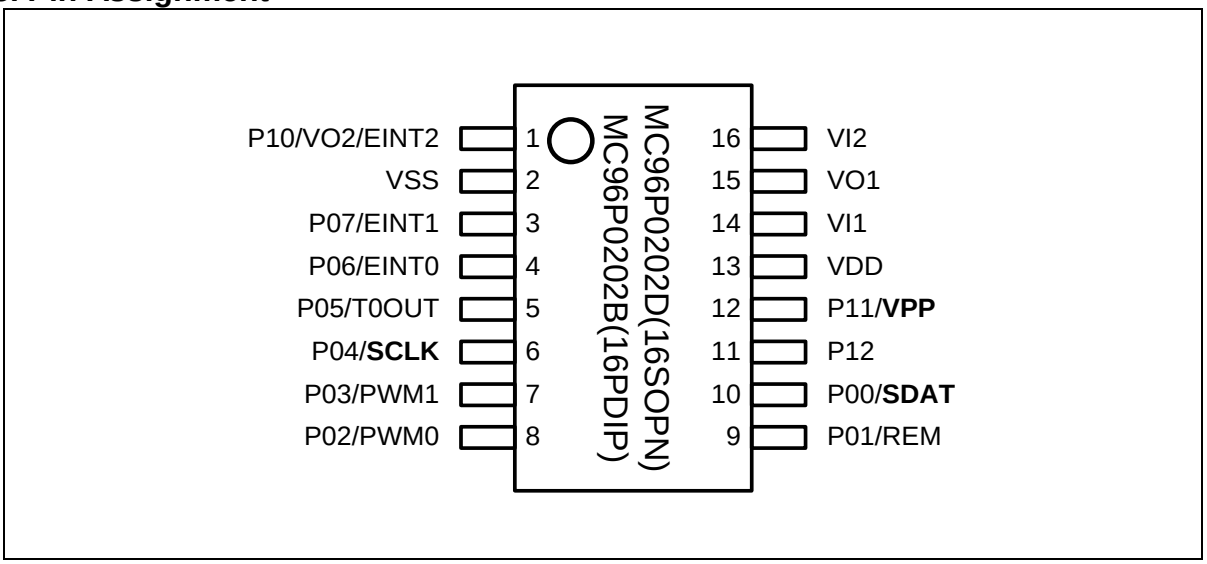
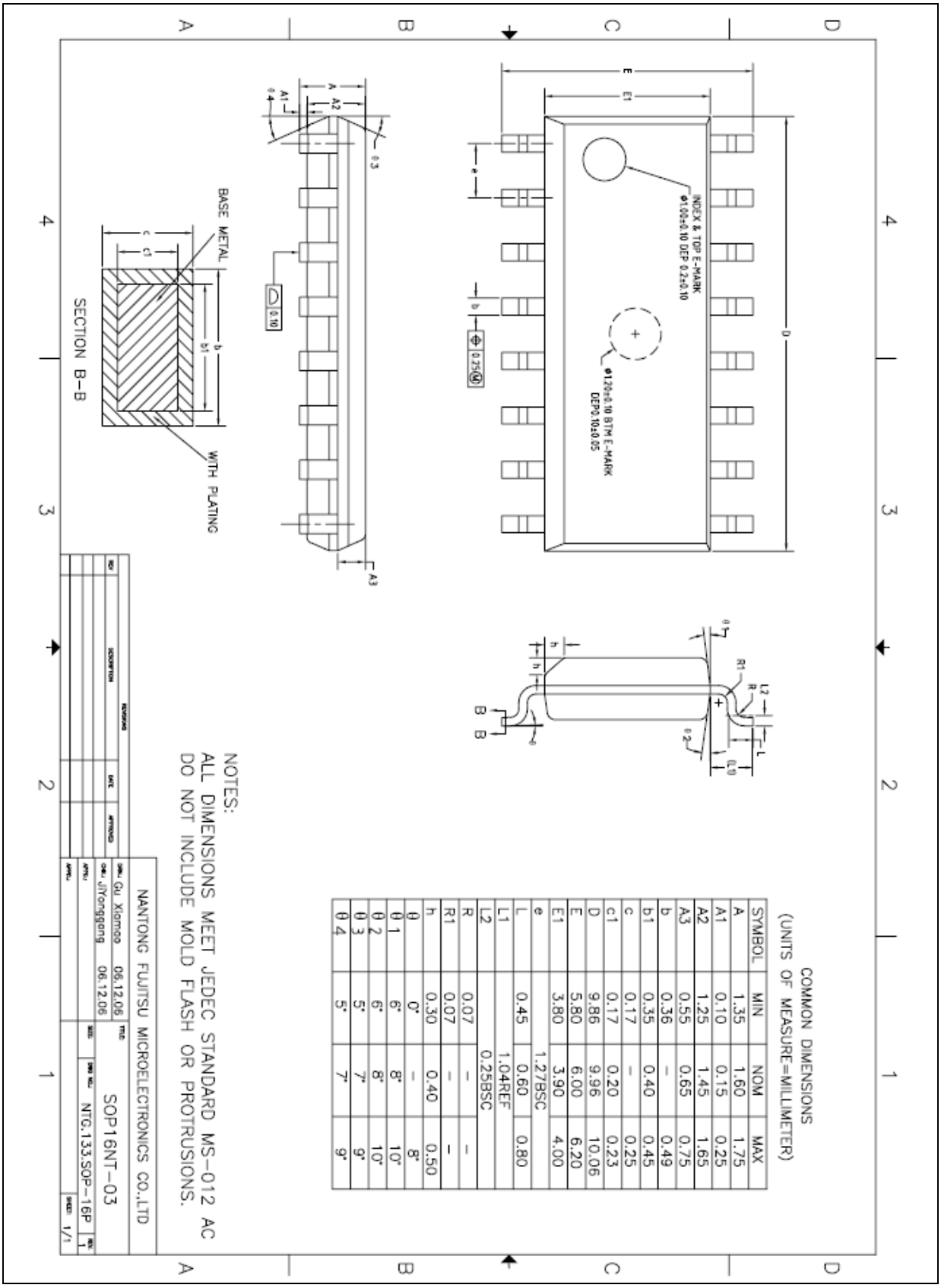


Figure 3.1 MC96P0202 16SOPN/16PDIP Pin Assignment

NOTES) 1. The OTP programming uses P04, P00, and P11 pin as SCLK, SDAT, and VPP, refer to the chapter 1.5 OTP Progrmming.

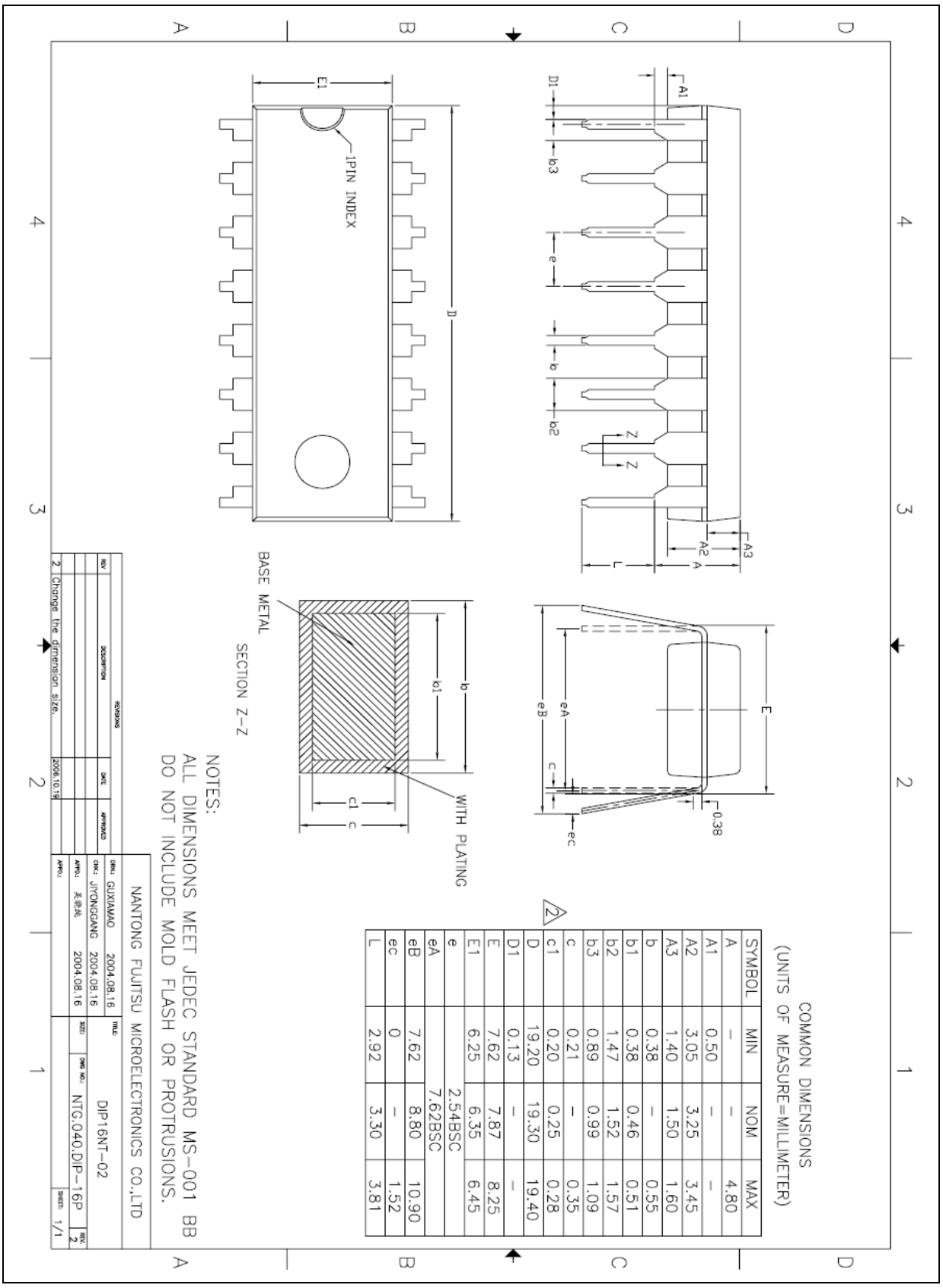
2. There is EVA Chip(MC96P0202D-EVA) for On-Chip Debugging, refer to the chapter 14. On-chip Debug System

4. Package Diagram



SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36	–	0.49
b1	0.35	0.40	0.45
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	9.86	9.96	10.06
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

Figure 4.1 16-Pin SOPN Package



SYMBOL	MIN	NOM	MAX
A	—	—	4.80
A1	0.50	—	—
A2	3.05	3.25	3.45
A3	1.40	1.50	1.60
b	0.38	—	0.55
b1	0.38	0.46	0.51
b2	1.47	1.52	1.57
b3	0.89	0.99	1.09
c	0.21	—	0.35
c1	0.20	0.25	0.28
D	19.20	19.30	19.40
D1	0.13	—	—
E	7.62	7.87	8.25
E1	6.25	6.35	6.45
e		2.54BSC	
eA		7.62BSC	
eB	7.62	8.80	10.90
ec	0	—	1.52
L	2.92	3.30	3.81

Figure 4.2 16-Pin PDIP Package

5. Pin Description

Table 5-1 Normal pin description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	P00 – P05 are a bit-programmable I/O port which can be configured as a schmitt trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SDAT
P01				REM
P02				PWM0
P03				PWM1
P04				SCLK
P05				T0OUT
P06	I/O	P06 and P07 are a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up/pull-down resistor can be specified in 1-bit unit.	Input	EINT0
P07				EINT1
P10	–	P10 is an input with a 2.2kΩ series resistor which is internally connected to the VO2. This pin is used for reading output of AMP2. So, this port should not be used for external input from VO2 pin.	Input	VO2/EINT2
P11	I/O	P11 and P12 are a bit-programmable I/O port which can be configured as a schmitt trigger input or an open-drain output.	Output	VPP
P12				–
VI1	I	The input of a high gain inverter amplifier 1	Input	–
VI2	I	The input of a high gain inverter amplifier 2	Input	–
VO1	O	The output of a high gain inverter amplifier 1	Output	–
VO2	O	The output of a high gain inverter amplifier 2	Output	P10/EINT2
PWM0	I/O	PWM0 output	Input	P02
PWM1	I/O	PWM1 output	Input	P03
REM	I/O	Carrier generation output	Input	P01
T0OUT	I/O	Timer 0 interval output	Input	P05
EINT0	I/O	An external interrupt input	Input	P06
EINT1	I/O	An external interrupt input	Input	P07
EINT2	–	An interrupt input which is internally connected to the VO2	Input	P10/VO2
SDAT	I/O	Serial data pin for OTP programming	Input	P00
SCLK	I/O	Serial clock pin for OTP programming	Input	P04
VPP	I/O	Power supply pin for OTP programming	Output	P11
V_{DD}, V_{SS}	–	Power input pins	–	–

6. Port Structures

6.1 General Purpose I/O Port

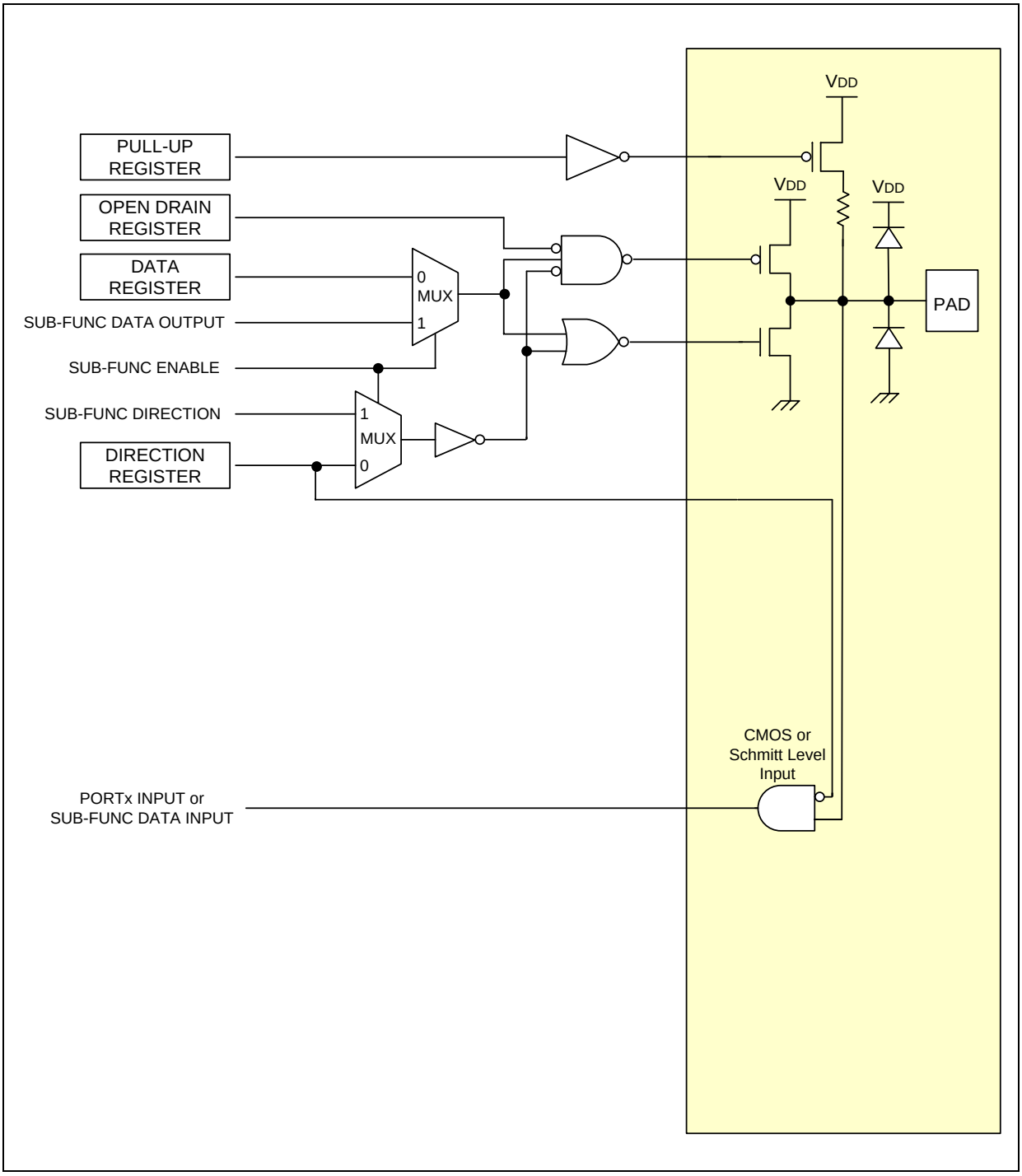


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

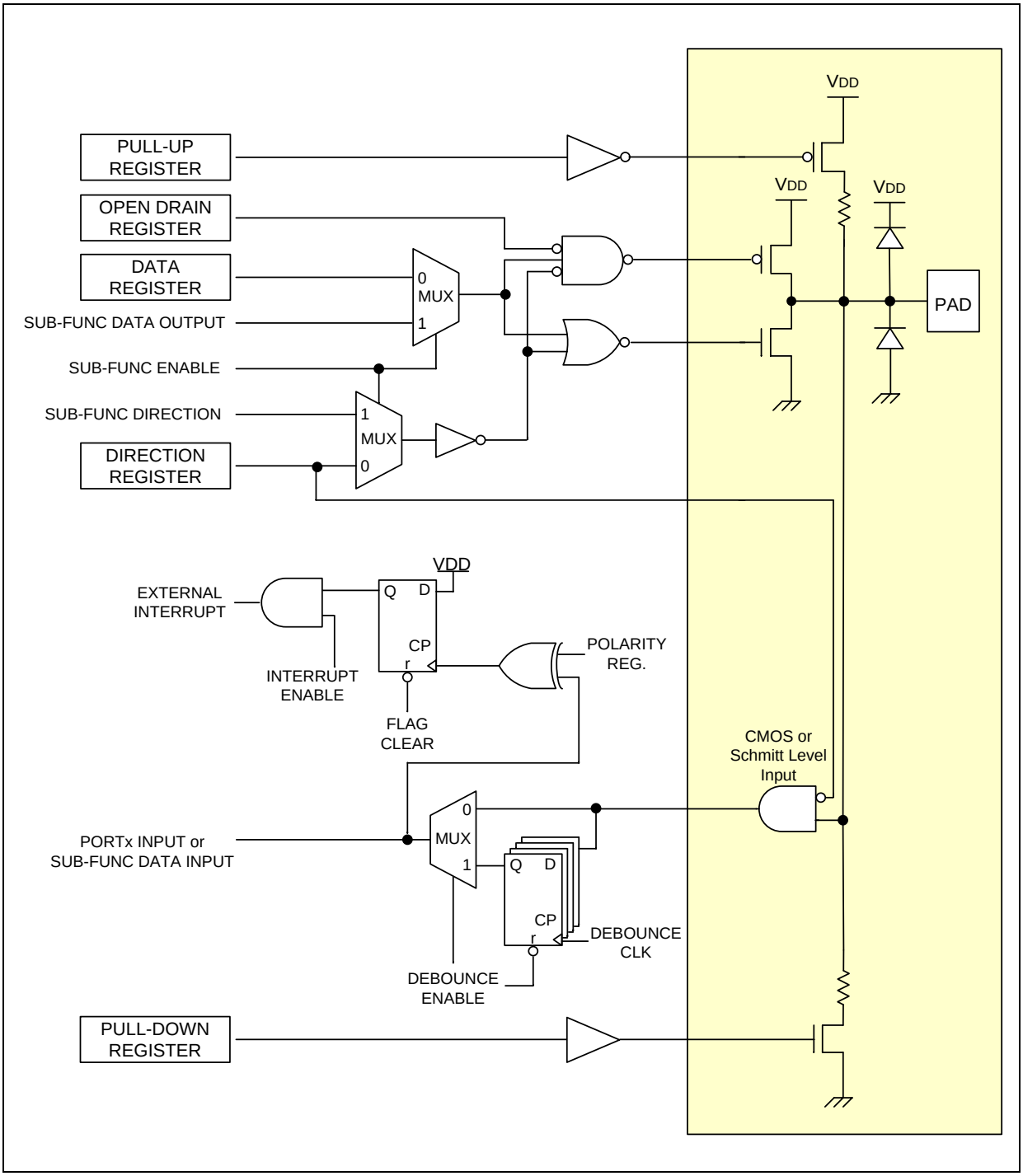


Figure 6.2 External Interrupt I/O Port

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.0	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 ~ +150	°C	–

NOTE) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Table 7-2 Recommended Operating Conditions

(T_A= -20°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Supply Voltage	VDD	f_X= 1.0 ~ 4.0MHz	Internal RC	2.2	–	5.5	V
		f_X= 1.0 ~ 8.0MHz		2.4	–	5.5	
Operating Temperature	T_{OPR}	VDD= 2.2 ~ 5.5V		-20	–	85	°C

7.3 Power-On Reset Characteristics

Table 7-3 Power-On Reset Characteristics

(T_A= -20°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	T_A= 25°C	–	2.00	–	V
VDD Voltage Rising Time	t_R	–	0.02	–	–	V/mS

7.4 Low Voltage Reset Characteristics

Table 7-4 LVR Characteristics

(T_A= -20°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Detection Level	V_{LVR}	T_A= 25°C	2.00	2.20	2.40	V
			2.10	2.30	2.50	
			2.25	2.50	2.75	
Hysteresis	△V	T_A= 25°C	-	40	100	mV
Minimum Pulse Width	t_{LW}	–	100	–	–	µS

7.5 Internal RC Oscillator Characteristics

Table 7-5 Internal RC Oscillator Characteristics

(T_A= -20°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	–		–	8.0	–	MHz
Tolerance	–	V_{DD} = 2.4V ~ 5.5V	T_A = -20°C ~ +50°C	-5	–	+5	%
		V_{DD} = 2.2V ~ 5.5V		-8	–	+8	
Clock Duty Ratio	TOD	–		40	50	60	%
Stabilization Time	t_{FS}	T_A= 25°C		–	–	100	µS

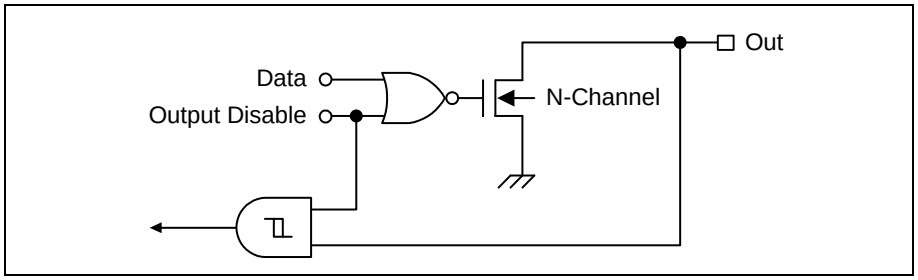
7.6 DC Characteristics

Table 7-6 DC Characteristics

(T_A= -20°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P00~P05, P11, P12		0.8VDD	–	VDD	V
	V_{IH2}	VDD= 3.0V, P06, P07, P10		0.55VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P00~P05, P11, P12		–	–	0.2VDD	V
	V_{IL2}	VDD= 3.0V, P06, P07, P10		–	–	0.40VDD	V
Input Peak to Peak Voltage	V_{INP-P}	$f_{IN} \leq$ 10kHz (Sine wave with a capacitor and a feedback resistor) V_{DD} = 3.0 V; VI1, VI2		0.03	–	VDD	V
Output Open-drain Voltage	V_{OD}	P11, P12(NOTE1)		–	–	12.0	V
Output High Voltage	V_{OH}	P0; I_{OH}= -5mA, VDD= 3.5V ~ 4.5V		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	P0; I_{OL}= 10mA, VDD= 3.5V ~ 4.5V		–	–	1.0	V
	V_{OL2}	P11, P12(NOTE1); I_{OL}= 20mA, VDD= 3.5V ~ 4.5V		–	–	2.0	
Output Source/Sink Current	I_{OH}	VDD= 3.0V, VO1, VO2(NOTE2) V_{OH} = VDD - 0.5V		200	500	900	µA
	I_{OL}	VDD= 3.0V, VO1, VO2(NOTE2) V_{OL} = VSS + 0.5V		200	500	900	µA
Input High Leakage Current	I_{IH}	All input ports		–	–	1	µA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	µA
Pull-Up Resistor	R_{PU}	VI=0V, T_A= 25°C P0	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
Pull-Down Resistor	R_{PD}	VI=VDD, T_A= 25°C P06, P07	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	

NOTE 1) P11 and P12 can be configured as a schmitt trigger input or an open-drain output as below figure.



NOTE 2) The I_{OH}/I_{OL} of the VO2 is the source/sink current at the output node of the inverter 2. So, the current at the pad will be diminished by a 2.2kΩ series resistor between the output node and the pad of the inverter 2

Table 7-6 DC Characteristics (Continued)

(T_A= -20°C ~ +85°C, VDD= 2.2V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Current	I_{DD1} (RUN)	f_{IRC} = 8MHz, VDD= 5V±10%	–	6.0	9.0	mA
		f_{IRC} = 8MHz, VDD= 3V±10%	–	4.0	6.0	
	I_{DD2} (IDLE)	f_{IRC} = 8MHz, VDD= 5V±10%	–	2.0	3.0	mA
		f_{IRC} = 8MHz, VDD= 3V±10%	–	1.0	2.0	
	I_{DD5} (STOP)	VDD= 3V±10%, T_A= 25°C	–	3.0	10.0	µA
		VDD= 3V±10%, T_A= -20°C ~ +70°C	–	–	20.0	µA

NOTES) 1. Supply current does not include current drawn through internal pull-up resistors.
2. All supply current include the current of the power-on reset(POR) and low voltage reset(LVR) blocks.
3. The IDD5 is current when the internal RC oscillation stops.

7.7 AC Characteristics

Table 7-7 AC Characteristics

(T_A= -20°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	nS

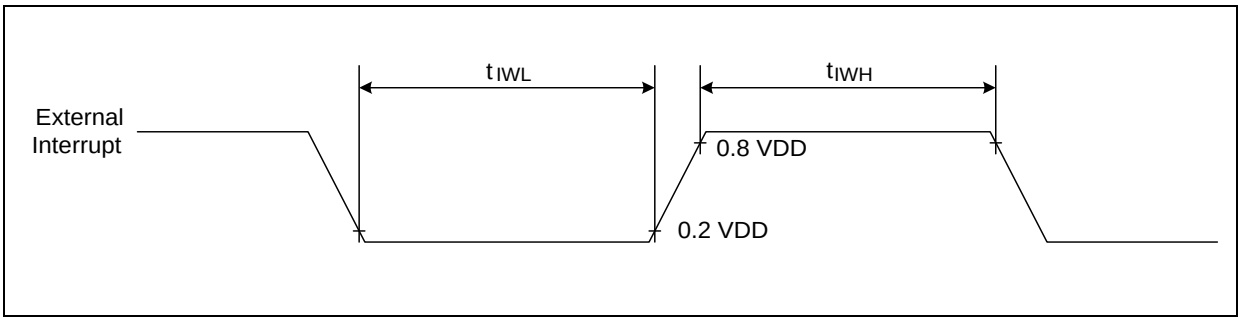


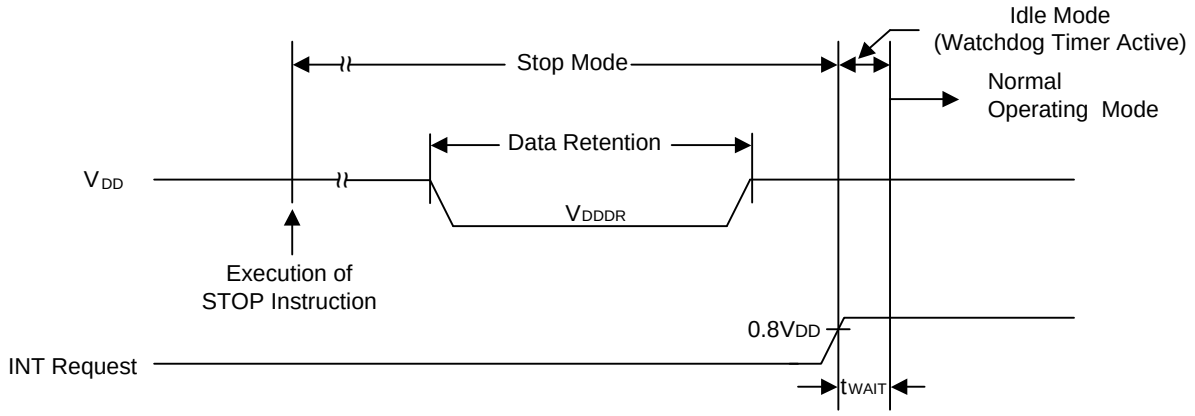
Figure 7.1 Input Timing for External Interrupts

7.8 Data Retention Voltage in Stop Mode

Table 7-8 Data Retention Voltage in Stop Mode

(T_A= -20°C ~ +85°C, VDD= 2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.2	–	5.5	V
Data retention supply current	I_{DDDR}	VDDDR= 2.2V, (T_A= 25°C), Stop mode	–	–	20	μA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.2 Stop Mode Release Timing when Initiated by an Interrupt

7.9 Input/Output Capacitance

Table 7-9 Input/Output Capacitance

(T_A= -20°C ~ +85°C, VDD= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

7.10 Operating Voltage Range

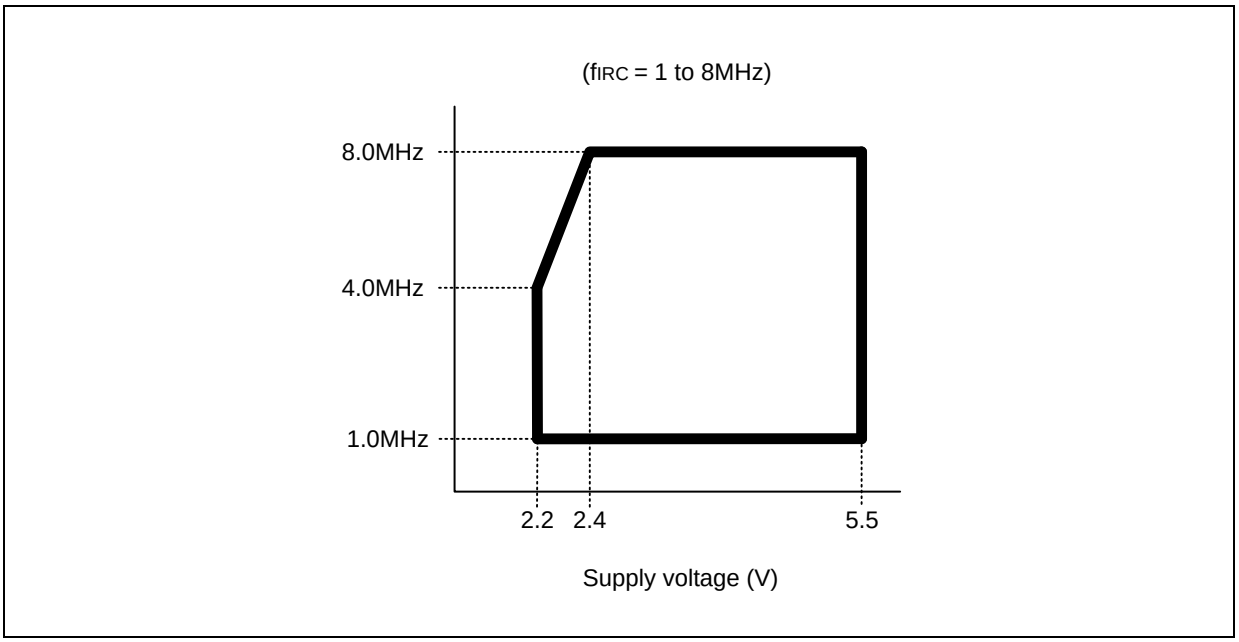


Figure 7.3 Operating Voltage Range

7.11 Recommended Circuit and Layout

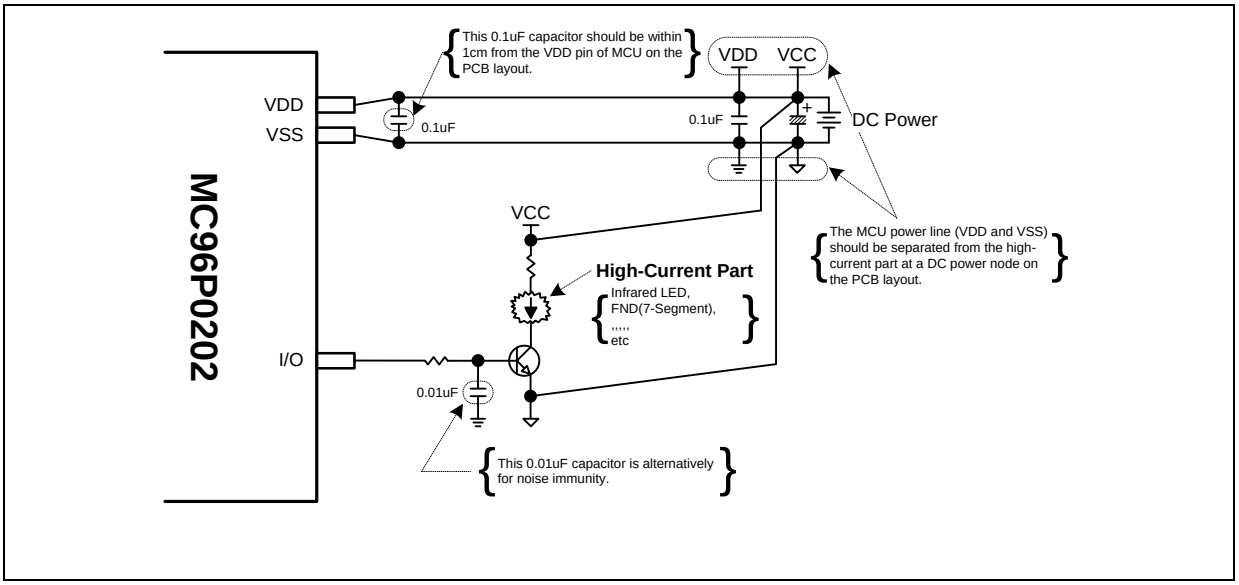


Figure 7.4 Recommended Circuit and Layout

7.12 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

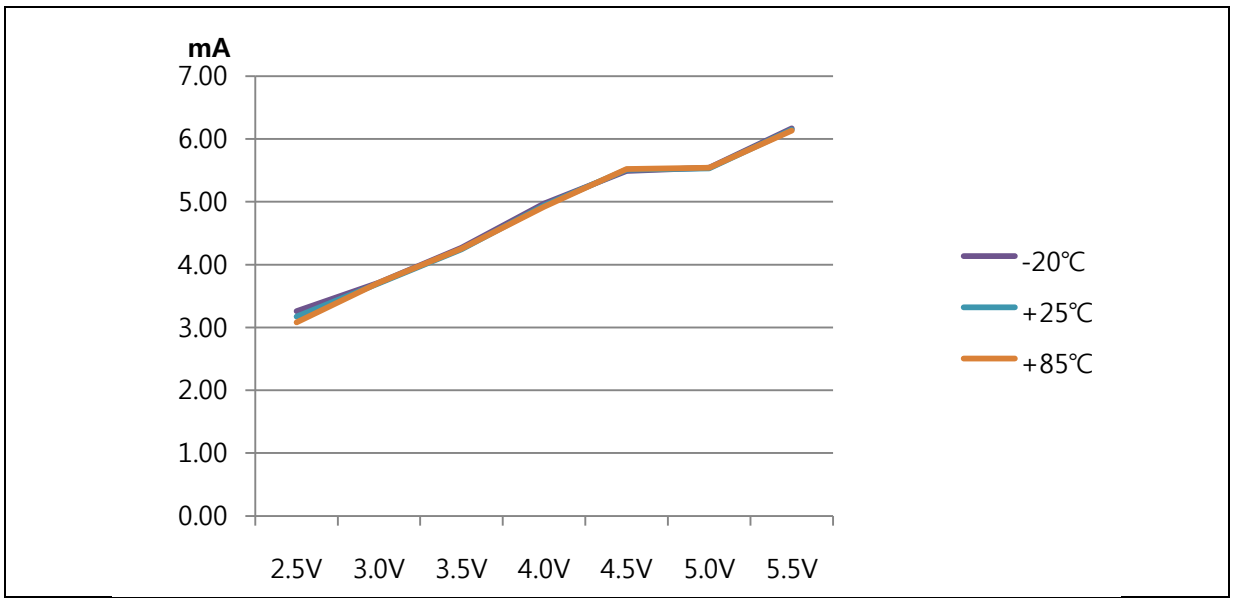


Figure 7.5 RUN (IDD1) Currnet

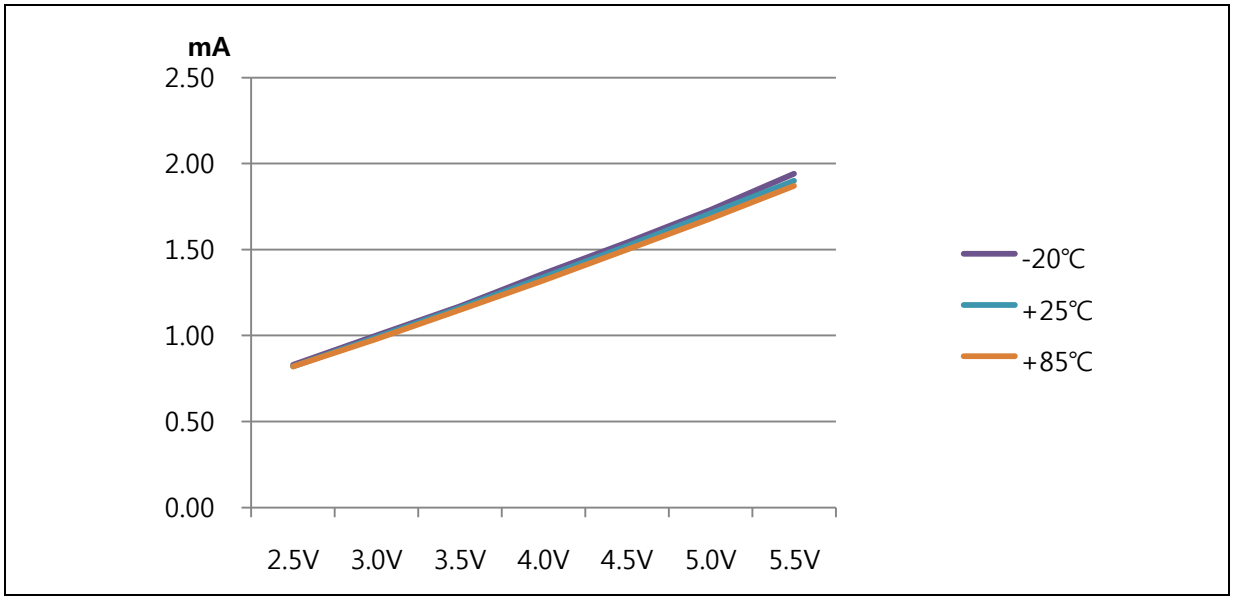


Figure 7.6 IDLE (IDD2) Current

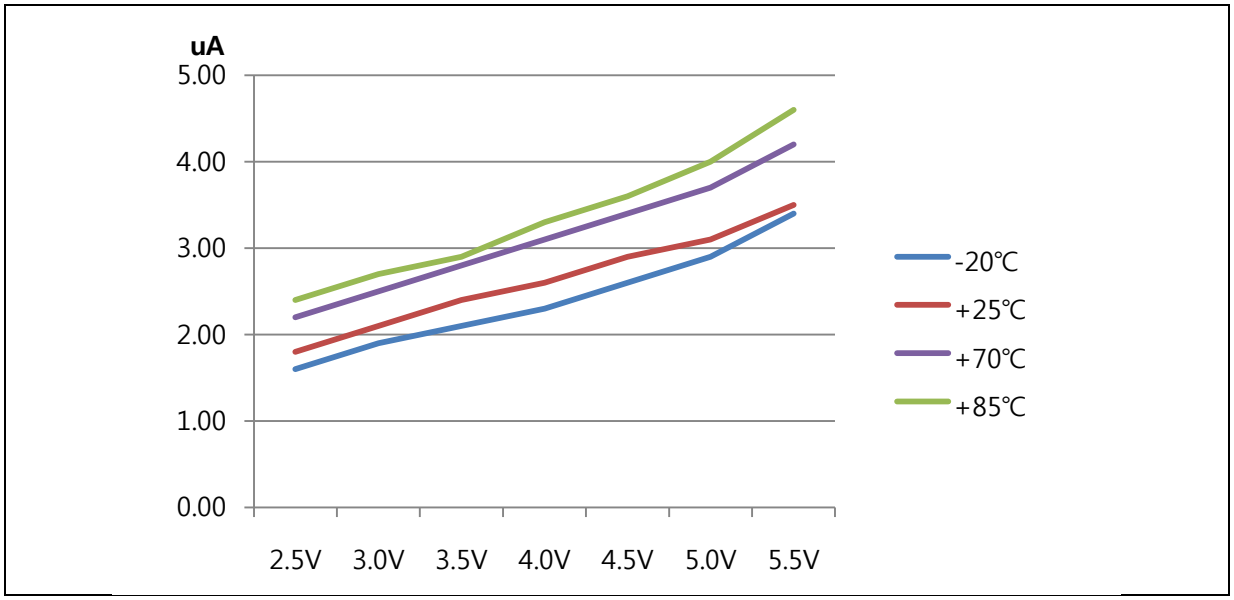


Figure 7.7 STOP (IDD5) Current

8. Memory

The MC96P0202 addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

MC96P0202 provides on-chip 2k bytes of the OTP type program memory. Internal data memory (IRAM) is 72 bytes and it includes the stack area.

8.1 Program Memory

A 16-bit program counter is capable of addressing up to 64k bytes, but this device has just 2k bytes program memory space.

Figure 8-1 shows the map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 1, for example, is assigned to location 000BH. If external interrupt 1 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8 byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

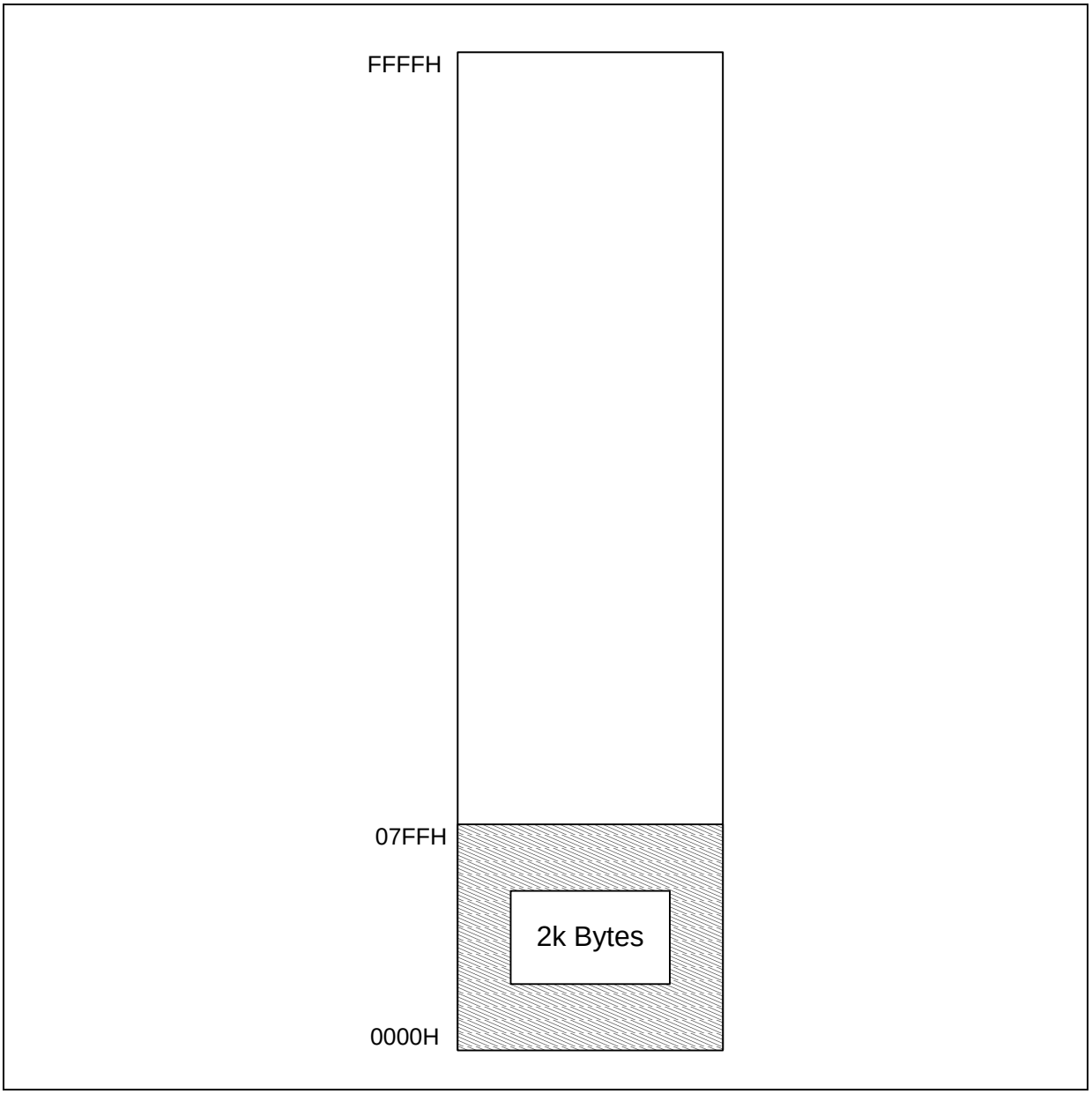


Figure 8.1 Program Memory

- 2k Bytes Including Interrupt Vector Region

8.2 Data Memory

Figure 8-2 shows the internal data memory space available.

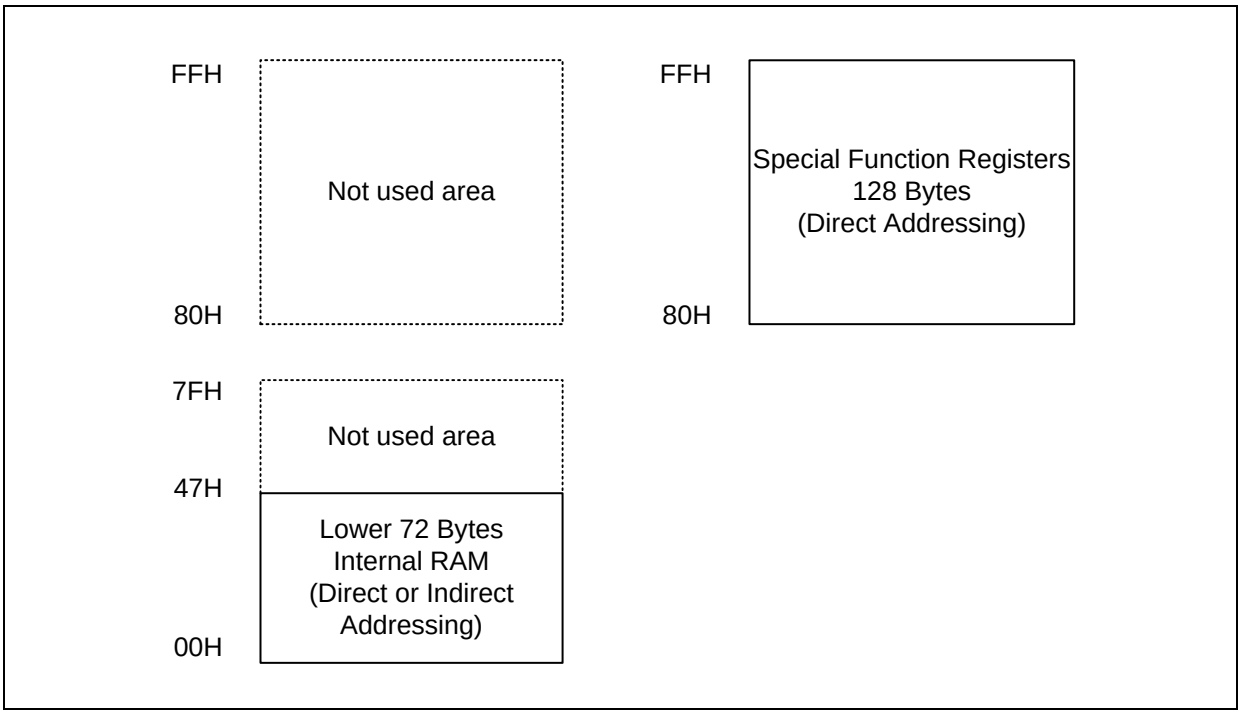


Figure 8.2 Data Memory Map

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128 bytes, upper 128 bytes, and SFR space.

Internal data memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, in fact the addressing modes for internal RAM can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 8-2 shows the upper 128 bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 8-3. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128 bytes can be accessed by either direct or indirect addressing. The upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

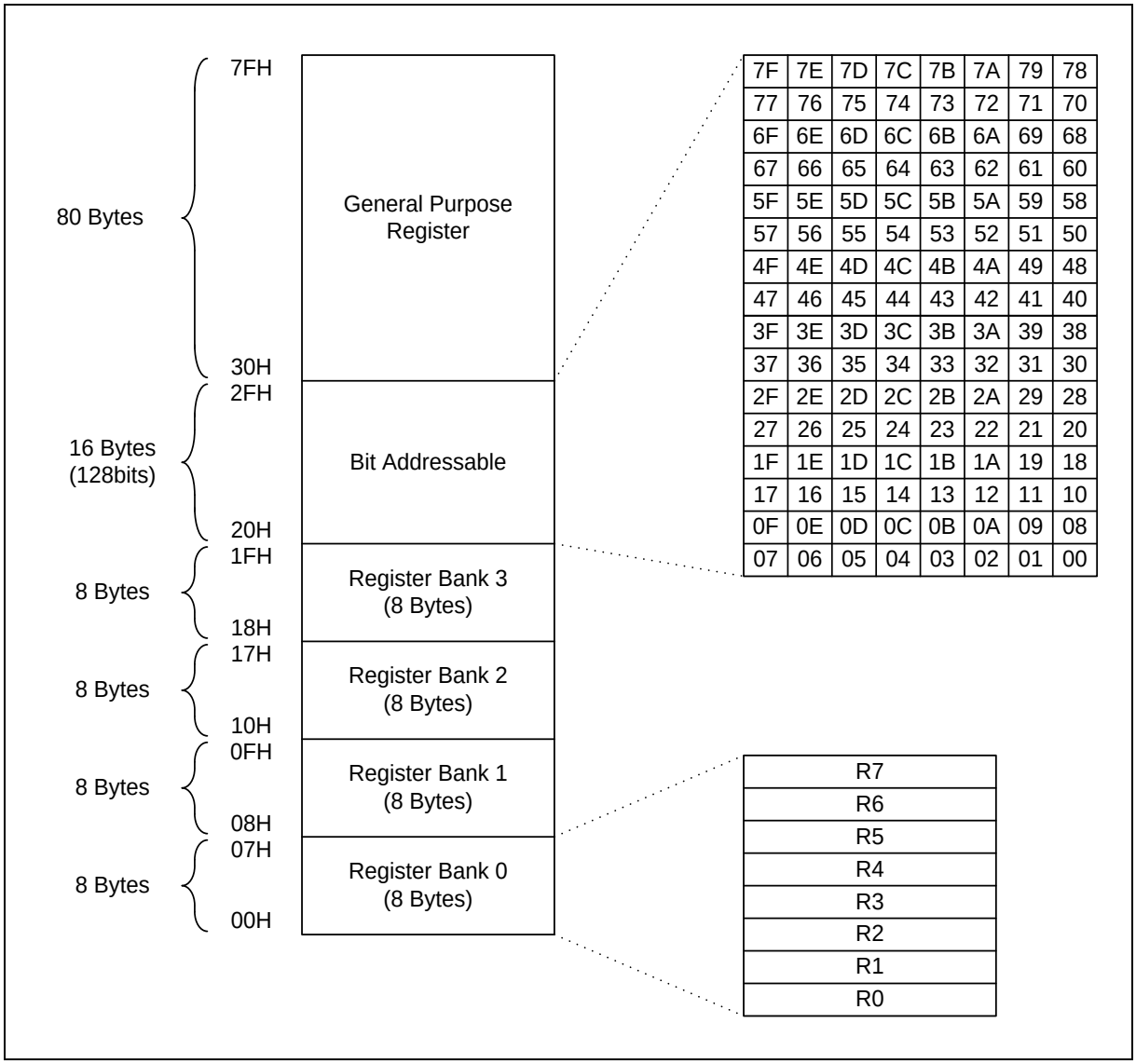


Figure 8.3 Lower 128 Bytes RAM

8.3 SFR Map

8.3.1 SFR Map Summary

Table 8-1 SFR Map Summary

-	Reserved
	M8051 compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	–	–	–	–	–	–
0F0H	B	–	–	–	–	–	–	–
0E8H	RSTFR	–	–	–	–	–	–	–
0E0H	ACC	–	–	–	–	–	–	–
0D8H	LVRCR	–	–	–	–	–	–	–
0D0H	PSW	–	–	–	–	–	–	–
0C8H	OSCCR	–	–	–	–	–	–	–
0C0H	PWMFGR	–	–	PWMCNT	PWM0DR	PWM1DR	–	–
0B8H	IP	–	–	T1CNT	T1DRL	T1DRH	CARCR	–
0B0H	EIFLAG	EIPOL	–	T0CNT	T0DR	–	–	–
0A8H	IE	IE1	IE2	IE3	–	–	–	–
0A0H	PWMCR	–	EO	–	–	–	–	–
98H	T1CR	P1IO	–	–	–	–	–	–
90H	T0CR	P0IO	P0PU	P0PD	P0OD	P01DB	P0FSR	–
88H	P1	–	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	–
80H	P0	SP	DPL	DPH	DPL1	DPH1	–	PCON

NOTE) (1)These registers are bit-addressable.

8.3.2 SFR Map

Table 8-2 SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Reserved	–	–	–							
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	–	–	–	–	–	1	1	0
89H	Reserved	–	–	–							
8AH	System and Clock Control Register	SCCR	R	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	–	–	–	0	0	1	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	–	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	Reserved	–	–	–							
90H	Timer 0 Control Register	T0CR	R/W	0	0	0	0	0	0	0	0
91H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
92H	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
93H	P0 Pull-down Resistor Selection Register	P0PD	R/W	0	0	–	–	–	–	–	–
94H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
95H	P0/P1 Debounce Enable Register	P01DB	R/W	0	0	–	–	–	0	0	0
96H	Port 0 Function Selection Register	P0FSR	R/W	–	–	–	–	0	0	0	0
97H	Reserved	–	–	–							
98H	Timer 1 Control Register	T1CR	R/W	0	0	0	0	0	0	0	0
99H	P1 Direction Register	P1IO	R/W	–	–	–	–	–	1	1	–
9AH	Reserved	–	–	–							
9BH	Reserved	–	–	–							
9CH	Reserved	–	–	–							
9DH	Reserved	–	–	–							
9EH	Reserved	–	–	–							
9FH	Reserved	–	–	–							

Table 8-2 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	PWM Generator Control Register	PWMCR	R/W	0	0	0	0	0	0	0	0
A1H	Reserved	–	–	–							
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	Reserved	–	–	–							
A4H	Reserved	–	–	–							
A5H	Reserved	–	–	–							
A6H	Reserved	–	–	–							
A7H	Reserved	–	–	–							
A8H	Interrupt Enable Register	IE	R/W	0	–	–	–	–	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	–	–	–	–	–
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	–	–	–	0	0	–
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	–	0	0	–	–	–
ACH	Reserved	–	–	–							
ADH	Reserved	–	–	–							
AEH	Reserved	–	–	–							
AFH	Reserved	–	–	–							
B0H	External Interrupt Flag Register	EIFLAG	R/W	–	–	–	–	–	0	0	0
B1H	External Interrupt Polarity Register	EIPOL	R/W	–	–	0	0	0	0	0	0
B2H	Reserved	–	–	–							
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
B5H	Reserved	–	–	–							
B6H	Reserved	–	–	–							
B7H	Reserved	–	–	–							
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	Reserved	–	–	–							
BAH	Reserved	–	–	–							
BBH	Timer 1 Counter Register	T1CNT	R	0	0	0	0	0	0	0	0
BCH	Timer 1 Data Low Register	T1DRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 Data High Register	T1DRH	R/W	1	1	1	1	1	1	1	1
BEH	Carrier Control Register	CARCR	R/W	0	–	0	0	–	–	0	0
BFH	Reserved	–	–	–							

Table 8-2 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	PWM Generator Flag Register	PWMFGR	R/W	–	0	–	–	–	–	0	0
C1H	Reserved	–	–	–							
C2H	Reserved	–	–	–							
C3H	PWM Generator Counter Register	PWMCNT	R	0	0	0	0	0	0	0	0
C4H	PWM Generator 0 Data Register	PWM0DR	R/W	1	1	1	1	1	1	1	1
C5H	PWM Generator 1 Data Register	PWM1DR	R/W	1	1	1	1	1	1	1	1
C6H	Reserved	–	–	–							
C7H	Reserved	–	–	–							
C8H	Oscillator Control Register	OSCCR	R/W	–	–	–	0	0	0	–	–
C9H	Reserved	–	–	–							
CAH	Reserved	–	–	–							
CBH	Reserved	–	–	–							
CCH	Reserved	–	–	–							
CDH	Reserved	–	–	–							
CEH	Reserved	–	–	–							
CFH	Reserved	–	–	–							
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–							
D2H	Reserved	–	–	–							
D3H	Reserved	–	–	–							
D4H	Reserved	–	–	–							
D5H	Reserved	–	–	–							
D6H	Reserved	–	–	–							
D7H	Reserved	–	–	–							
D8H	Low Voltage Reset Control Register	LVRCR	R/W	–	–	–	–	–	–	0	0
D9H	Reserved	–	–	–							
DAH	Reserved	–	–	–							
DBH	Reserved	–	–	–							
DCH	Reserved	–	–	–							
DDH	Reserved	–	–	–							
DEH	Reserved	–	–	–							
DFH	Reserved	–	–	–							

Table 8-2 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator A Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	Reserved	–	–	–							
E2H	Reserved	–	–	–							
E3H	Reserved	–	–	–							
E4H	Reserved	–	–	–							
E5H	Reserved	–	–	–							
E6H	Reserved	–	–	–							
E7H	Reserved	–	–	–							
E8H	Reset Flag Register	RSTFR	R/W	1	–	0	0	–	–	–	–
E9H	Reserved	–	–	–							
EAH	Reserved	–	–	–							
EBH	Reserved	–	–	–							
ECH	Reserved	–	–	–							
EDH	Reserved	–	–	–							
EEH	Reserved	–	–	–							
EFH	Reserved	–	–	–							
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Reserved	–	–	–							
F2H	Reserved	–	–	–							
F3H	Reserved	–	–	–							
F4H	Reserved	–	–	–							
F5H	Reserved	–	–	–							
F6H	Reserved	–	–	–							
F7H	Reserved	–	–	–							
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–							
FAH	Reserved	–	–	–							
FBH	Reserved	–	–	–							
FCH	Reserved	–	–	–							
FDH	Reserved	–	–	–							
FEH	Reserved	–	–	–							
FFH	Reserved	–	–	–							

8.3.3 Compiler Compatible SFR

ACC (Accumulator Register) : E0H

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ACC	Accumulator

B (B Register) : F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

B	B Register

SP (Stack Pointer) : 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 07H

SP	Stack Pointer

DPL (Data Pointer Register Low) : 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL	Data Pointer Low Byte

DPH (Data Pointer Register High) : 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH	Data Pointer High Byte

DPL1 (Data Pointer Register Low 1) : 84H

7	6	5	4	3	2	1	0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL1	Data Pointer Low 1 Byte

DPH1 (Data Pointer Register High 1) : 85H

7	6	5	4	3	2	1	0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH1	Data Pointer High 1 Byte

PSW (Program Status Word Register) : D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

CY	Carry Flag
AC	Auxiliary Carry Flag
F0	General Purpose User-Definable Flag
RS1	Register Bank Select bit 1
RS0	Register Bank Select bit 0
OV	Overflow Flag
F1	User-Definable Flag
P	Parity Flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator

EO (Extended Operation Register) : A2H

7	6	5	4	3	2	1	0
-	-	-	TRAP_EN	-	DPSEL2	DPSEL1	DPSEL0
-	-	-	R/W	-	R/W	R/W	R/W

Initial value : 00H

TRAP_EN Select the Instruction **(Keep always '0')**.

0 Select Software TRAP Instruction

1 Select MOVC @(DPTR++), A

DPSEL[2:0] Select Banked Data Pointer Register

DPSEL2	DPSEL1	SPSEL0	Description
0	0	0	DPTR0
0	0	1	DPTR1
Reserved			

9. I/O Ports

9.1 I/O Ports

The MC96P0202 has two groups of I/O ports (P0 ~ P1). Each port can be easily configured by software as I/O pin, internal pull up, internal pull down and open-drain pin to meet various system configurations and design requirements. Also P06 and P07 include function that can generate interrupt according to change of state of the pin.

9.2 Port Register

9.2.1 Data Register (Px)

Data Register is a bidirectional I/O port. If ports are configured as output ports, data can be written to the corresponding bit of the Px. If ports are configured as input ports, the data can be read from the corresponding bit of the Px.

9.2.2 Direction Register (PxIO)

Each I/O pin can be independently used as an input or an output through the PxIO register. Bits cleared in this register will make the corresponding pin of Px to input mode. Set bits of this register will make the pin to output mode. Almost bits are cleared by a system reset, but some bits are set by a system reset.

9.2.3 Pull-up Resistor Selection Register (PxPU)

The on-chip pull-up resistor can be connected to I/O ports individually with a pull-up resistor selection register (PxPU). The pull-up register selection controls the pull-up resister enable/disable of each port. When the corresponding bit is 1, the pull-up resister of the pin is enabled. When 0, the pull-up resister is disabled. All bits are cleared by a system reset.

9.2.4 Pull-down Resistor Selection Register (PxPD)

The on-chip pull-down resistor can be connected to I/O ports individually with a pull-down resistor selection register (PxPD). The pull-down register selection controls the pull-down resister enable/disable of each port. When the corresponding bit is 1, the pull-down resister of the pin is enabled. When 0, the pull-down resister is disabled. All bits are cleared by a system reset.

9.2.5 Open-drain Selection Register (PxOD)

There are internally open-drain selection registers (PxOD) for P0. The open-drain selection register controls the open-drain enable/disable of each port. Almost ports become push-pull by a system reset, but some ports become open-drain by a system reset.

9.2.6 Debounce Enable Register (PxDB)

P0[6:7] and P10 support debounce function. Debounce clocks of each ports are fx/1, fx/4, and fx/4096.

9.2.7 Port Function Selection Register (PxFSR)

These registers define alternative functions of ports. Please remember that these registers should be set properly for alternative port function. A reset clears the PxFSR register to '00H', which makes all pins to normal I/O ports.

9.2.8 Register Map

Table 9-1 Port Register Map

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	91H	R/W	00H	P0 Direction Register
P0PU	92H	R/W	00H	P0 Pull-up Resistor Selection Register
P0PD	93H	R/W	00H	P0 Pull-down Resistor Selection Register
P0OD	94H	R/W	00H	P0 Open-drain Selection Register
P01DB	95H	R/W	00H	P0/P1 Debounce Enable Register
P0FSR	96H	R/W	00H	Port 0 Function Selection Register
P1	88H	R/W	06H	P1 Data Register
P1IO	99H	R/W	06H	P1 Direction Register

9.3 P0 Port

9.3.1 P0 Port Description

P0 is 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P01DB), P0 pull-up resistor selection register (P0PU), P0 pull-down resistor selection register (P0PD), and P0 open-drain selection register (P0OD). The P01~P03 and P05 function can be selected by the P0FSR[3:0] bits of the P0FSR register. Refer to the port function selection registers.

9.3.2 Register description for P0

P0 (P0 Data Register) : 80H

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0[7:0] I/O Data

P0IO (P0 Direction Register) : 91H

7	6	5	4	3	2	1	0
P07IO	P06IO	P05IO	P04IO	P03IO	P02IO	P01IO	P00IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0IO[7:0] P0 Data I/O Direction.

0 Input

1 Output

NOTE) EINT0/EINT1 function possible when input

P0PU (P0 Pull-up Resistor Selection Register) : 92H

7	6	5	4	3	2	1	0
P07PU	P06PU	P05PU	P04PU	P03PU	P02PU	P01PU	P00PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0PU[7:0] Configure Pull-up Resistor of P0 Port

0 Disable

1 Enable

P0PD (P0 Pull-down Resistor Selection Register) : 93H

7	6	5	4	3	2	1	0
P07PD	P06PD	-	-	-	-	-	-
R/W	R/W	-	-	-	-	-	-

Initial value : 00H

P0PD[7:6] Configure Pull-down Resistor of P07/P06 Port

0 Disable

1 Enable

P0OD (P0 Open-drain Selection Register) : 94H

7	6	5	4	3	2	1	0
P07OD	P06OD	P05OD	P04OD	P03OD	P02OD	P01OD	P00OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0OD[7:0]	Configure Open-drain of P0 Port	
	0	Push-pull output
	1	Open-drain output

P01DB (P0/P1 Debounce Enable Register) : 95H

7	6	5	4	3	2	1	0
DBCLK1	DBCLK0	-	-	-	P10DB	P07DB	P06DB
R/W	R/W	-	-	-	R/W	R/W	R/W

Initial value : 00H

DBCLK[1:0]	Configure Debounce Clock of Port		
	DBCLK1	DBCLK0	Description
	0	0	fx/1
	0	1	fx/4
	1	0	fx/4096
	1	1	Reserved
P10DB	Configure Debounce of P10 Port		
	0	Disable	
	1	Enable	
P07DB	Configure Debounce of P07 Port		
	0	Disable	
	1	Enable	
P06DB	Configure Debounce of P06 Port		
	0	Disable	
	1	Enable	

NOTES) 1. If the same level is not detected on enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.

2. A pulse level should be input for the duration of 3 clock or more to be actually detected as a valid edge.

3. The port debounce is automatically disabled at stop mode and recovered after stop mode release.

9.4 P1 Port

9.4.1 P1 Port Description

P1 is 3-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P01DB).

9.4.2 Register description for P1

P1 (P1 Data Register) : 88H

7	6	5	4	3	2	1	0
-	-	-	-	-	P12	P11	P10
-	-	-	-	-	R/W	R/W	R

Initial value : 06H

P1[2:0]	I/O Data

P1IO (P1 Direction Register) : 99H

7	6	5	4	3	2	1	0
-	-	-	-	-	P12IO	P11IO	-
-	-	-	-	-	R/W	R/W	-

Initial value : 06H

P1IO[2:1]	P1 Data I/O Direction
0	Input
1	Open-drain output

NOTE) P10 is used for reading output of AMP2. So, this port should not be used for external input from VO2 pin

9.5 Port Function

9.5.1 Port Function Description

Port function control registers consist of Port function selection register 0(P0FSR).

9.5.2 Register description for P0FSR

P0FSR (Port 0 Function Selection Register) : 96H

7	6	5	4	3	2	1	0
-	-	-	-	PFSR05	PFSR03	PFSR02	PFSR01
-	-	-	-	R/W	R/W	R/W	R/W

Initial value : 00H

PFSR05	P05 Function Select	
	0	I/O Port
	1	T0OUT Function
PFSR03	P03 Function Select	
	0	I/O Port
	1	PWM1 Function
PFSR02	P02 Function Select	
	0	I/O Port
	1	PWM0 Function
PFSR01	P01 Function Select	
	0	I/O Port
	1	REM Function

10. Interrupt Controller

10.1 Overview

The MC96P0202 supports up to 8 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software. The interrupt controller has following features:

- Receive the request from 8 interrupt source
- 6 group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is served first.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency: 3~9 machine cycles in single interrupt system

The non-maskable interrupt is always enabled. The maskable interrupts are enabled through four pair of interrupt enable registers (IE, IE1, IE2, IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The MC96P0202 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Table 10-1 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

Table 10-1 Interrupt Group Priority Level

Interrupt Group	Highest → Lowest				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	Lowest

10.2 External Interrupt

The external interrupt on INT0, INT1 and INT2 pins receive various interrupt request depending on the external interrupt polarity register (EIPOL) as shown in Figure 10.1. The external interrupt flag register (EIFLAG) provides the status of external interrupts.

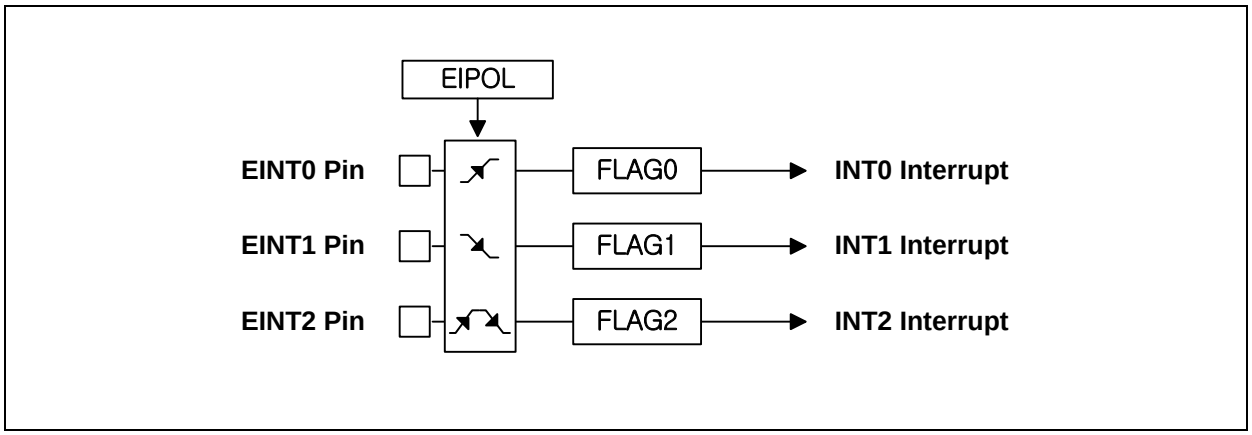


Figure 10.1 External Interrupt Description

10.3 Block Diagram

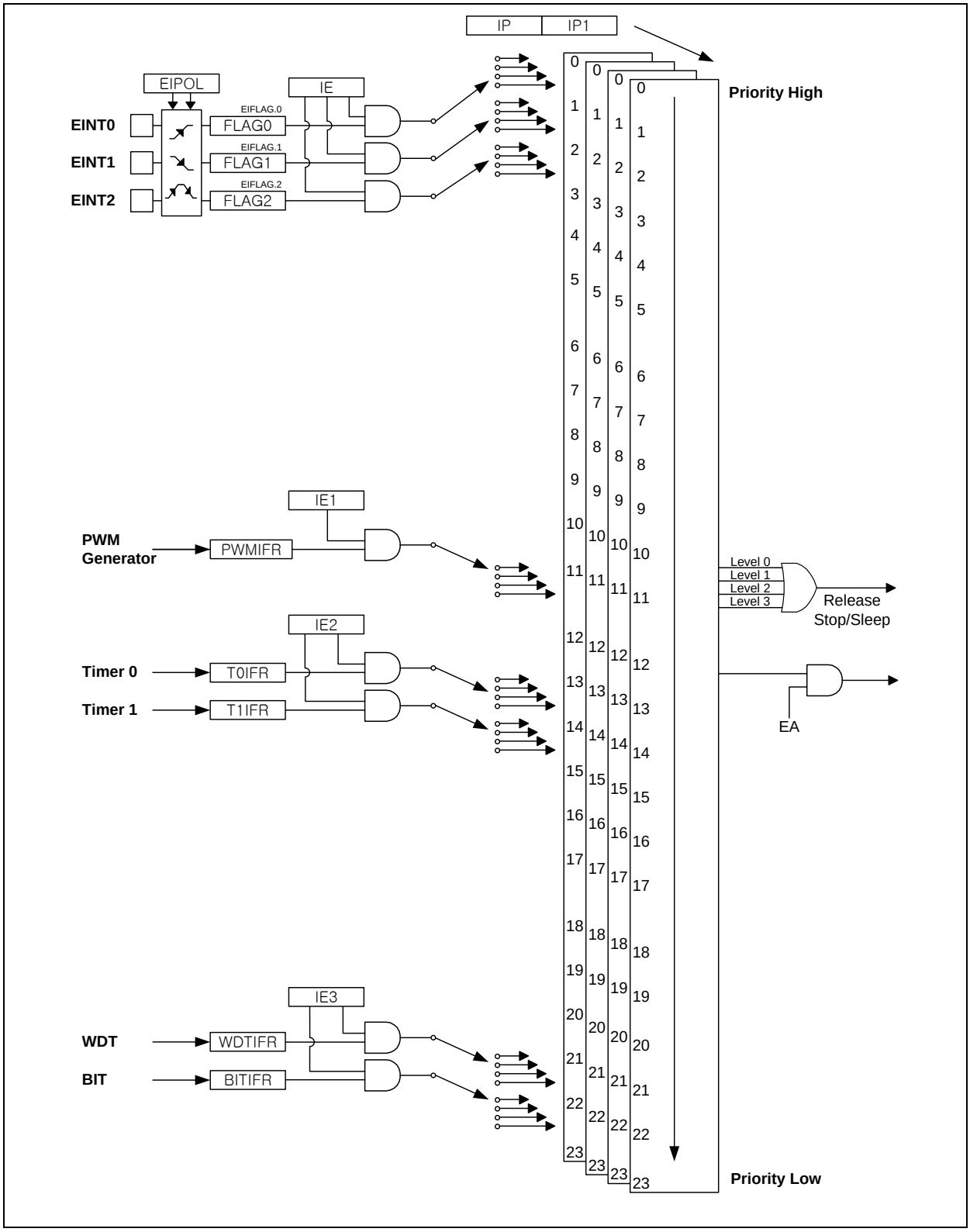


Figure 10.2 Block Diagram of Interrupt

NOTES) 1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.

2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

10.4 Interrupt Vector Table

The interrupt controller supports 24 interrupt sources as shown in the Table 10-2. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 10-2 Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Polarity	Mask	Vector Address
Hardware Reset	RESETB	0 0	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
External Interrupt 2	INT2	IE.2	3	Maskable	0013H
–	INT3	IE.3	4	Maskable	001BH
–	INT4	IE.4	5	Maskable	0023H
–	INT5	IE.5	6	Maskable	002BH
–	INT6	IE1.0	7	Maskable	0033H
–	INT7	IE1.1	8	Maskable	003BH
–	INT8	IE1.2	9	Maskable	0043H
–	INT9	IE1.3	10	Maskable	004BH
–	INT10	IE1.4	11	Maskable	0053H
PWM Generator Interrupt	INT11	IE1.5	12	Maskable	005BH
–	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
–	INT15	IE2.3	16	Maskable	007BH
–	INT16	IE2.4	17	Maskable	0083H
–	INT17	IE2.5	18	Maskable	008BH
–	INT18	IE3.0	19	Maskable	0093H
–	INT19	IE3.1	20	Maskable	009BH
–	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
–	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

10.5 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to ‘0’ by a reset or an instruction. Interrupt acceptance always generates at last cycle of the instruction. So instead of fetching the current instruction, CPU executes internally LCALL instruction and saves the PC at stack. For the interrupt service routine, the interrupt controller gives the address of LJMP instruction to CPU. Since the end of the execution of current instruction, it needs 3~9 machine cycles to go to the interrupt service routine. The interrupt service task is terminated by the interrupt return instruction [RETI]. Once an interrupt request is generated, the following process is performed.

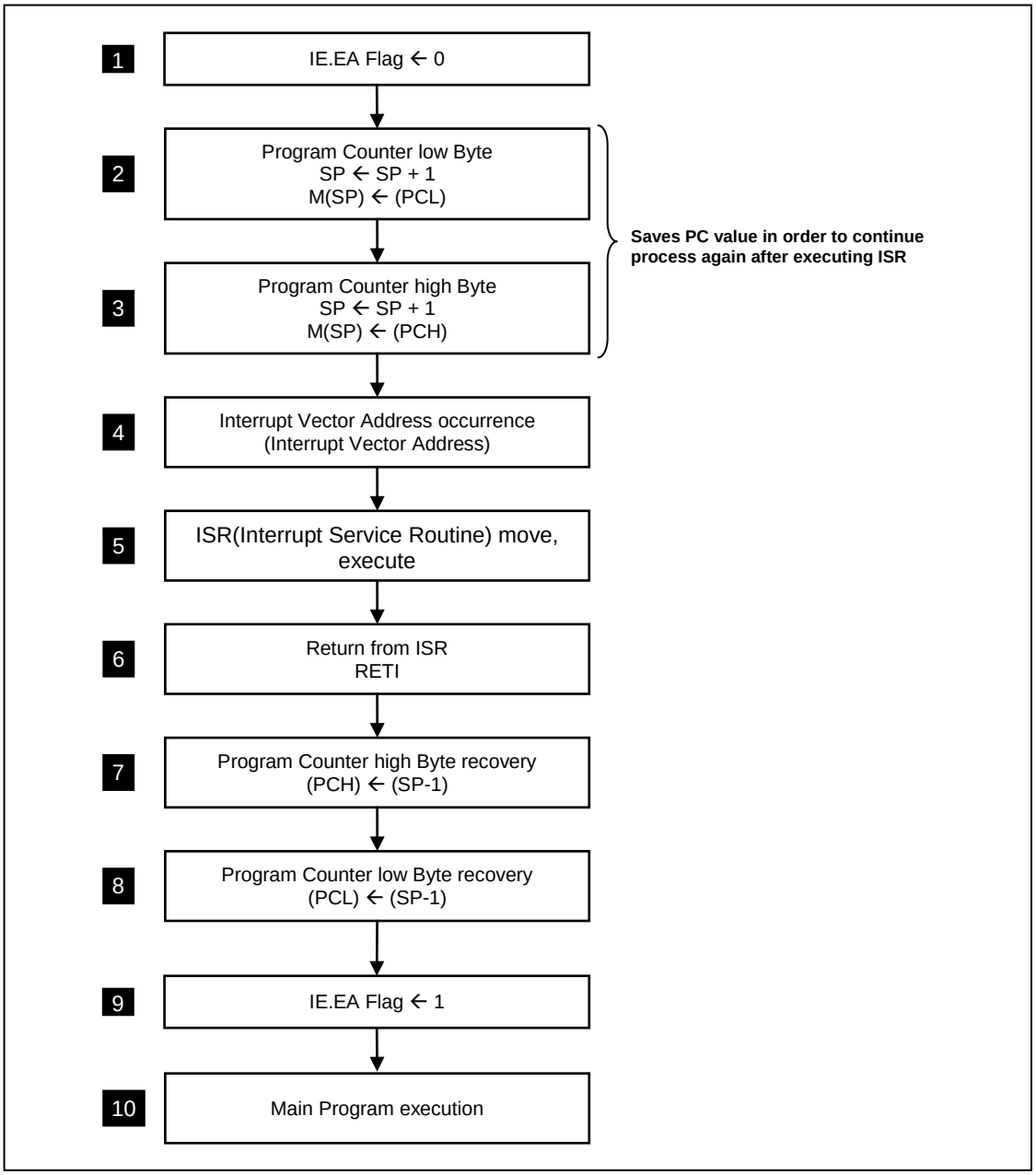


Figure 10.3 Interrupt Vector Address Table

10.6 Effective Timing after Controlling Interrupt Bit

Case a) Control Interrupt Enable Register (IE, IE1, IE2, IE3)

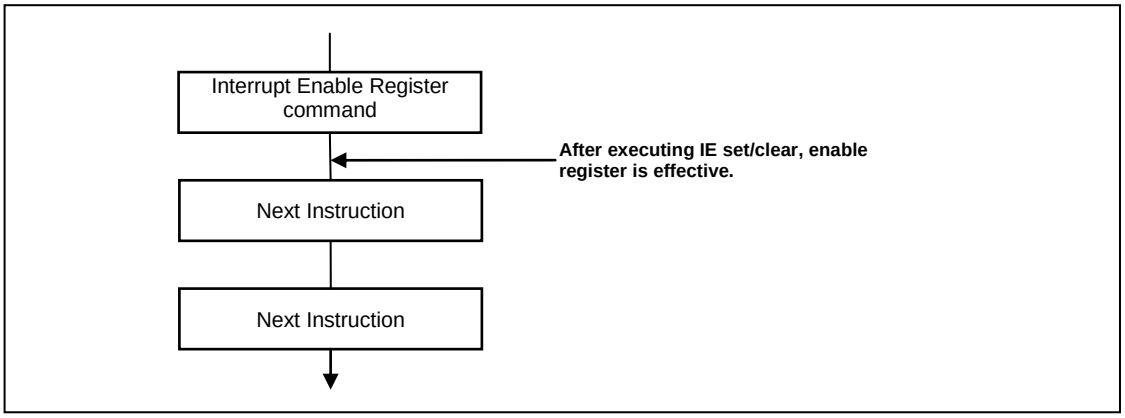


Figure 10.4 Effective Timing of Interrupt Enable Register

Case b) Interrupt flag Register

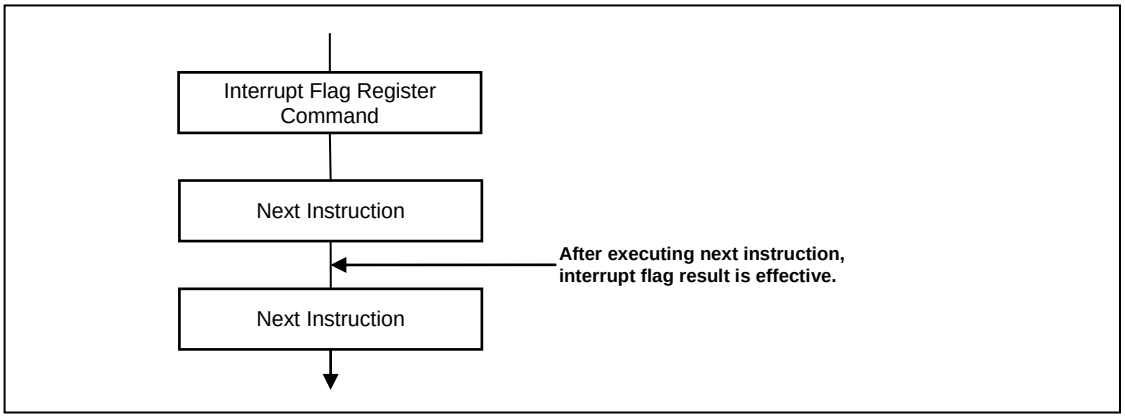


Figure 10.5 Effective Timing of Interrupt Flag Register

10.7 Multi Interrupt

If two requests of different priority levels are received simultaneously, the request of higher priority level is served first. If more than one interrupt request are received, the interrupt polling sequence determines which request is served first by hardware. However, for special features, multi-interrupt processing can be executed by software.

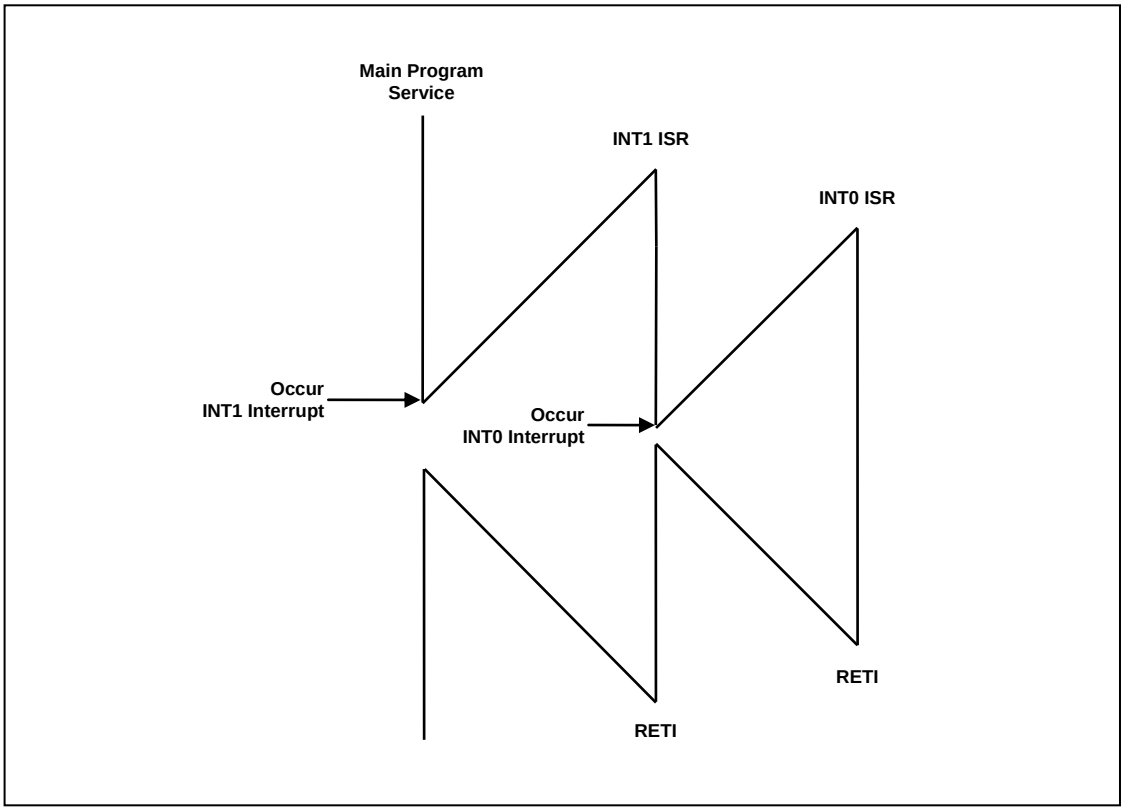


Figure 10.6 Effective Timing of Interrupt

Figure 10.6 shows an example of multi-interrupt processing. While INT1 is served, INT0 which has higher priority than INT1 is occurred. Then INT0 is served immediately and then the remain part of INT1 service routine is executed. If the priority level of INT0 is same or lower than INT1, INT0 will be served after the INT1 service has completed.

An interrupt service routine may be only interrupted by an interrupt of higher priority and, if two interrupts of different priority occur at the same time, the higher level interrupt will be served first. An interrupt cannot be interrupted by another interrupt of the same or a lower priority level. If two interrupts of the same priority level occur simultaneously, the service order for those interrupts is determined by the scan order.

10.8 Interrupt Enable Accept Timing

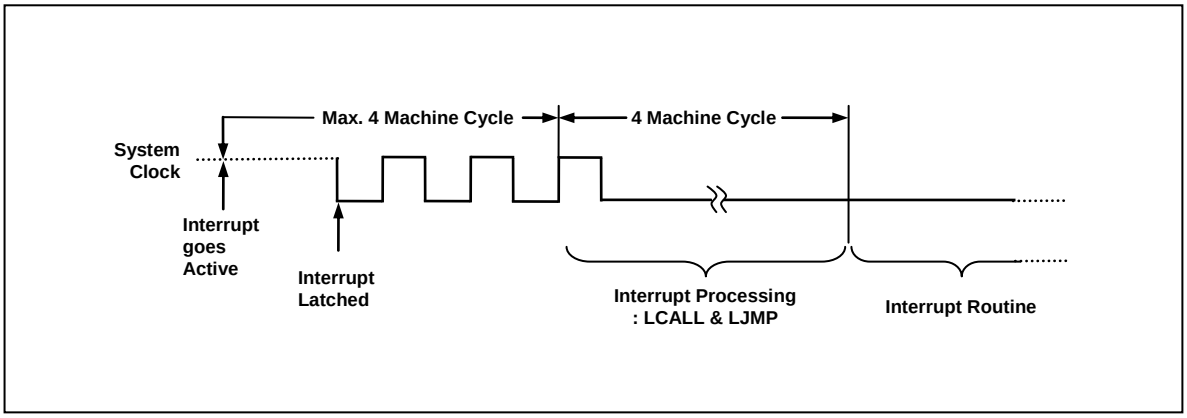


Figure 10.7 Interrupt Response Timing Diagram

10.9 Interrupt Service Routine Address

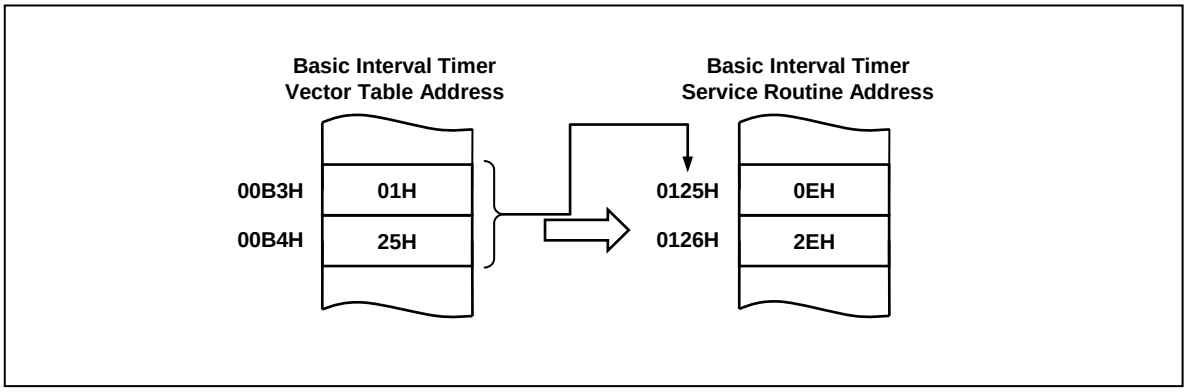


Figure 10.8 Correspondence between Vector Table Address and the Entry Address of ISP

10.10 Saving/Restore General-Purpose Registers

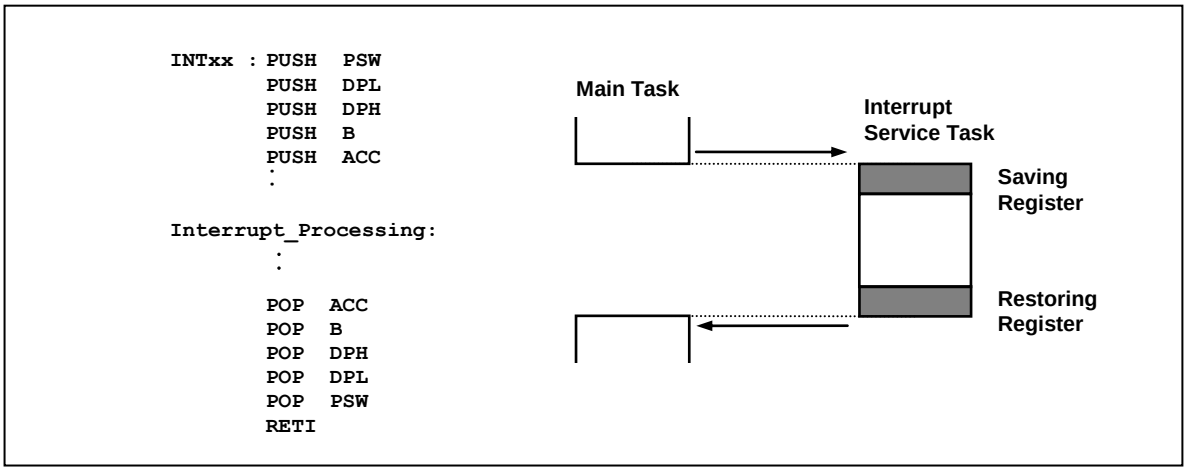


Figure 10.9 Saving/Restore Process Diagram and Sample Source

10.11 Interrupt Timing

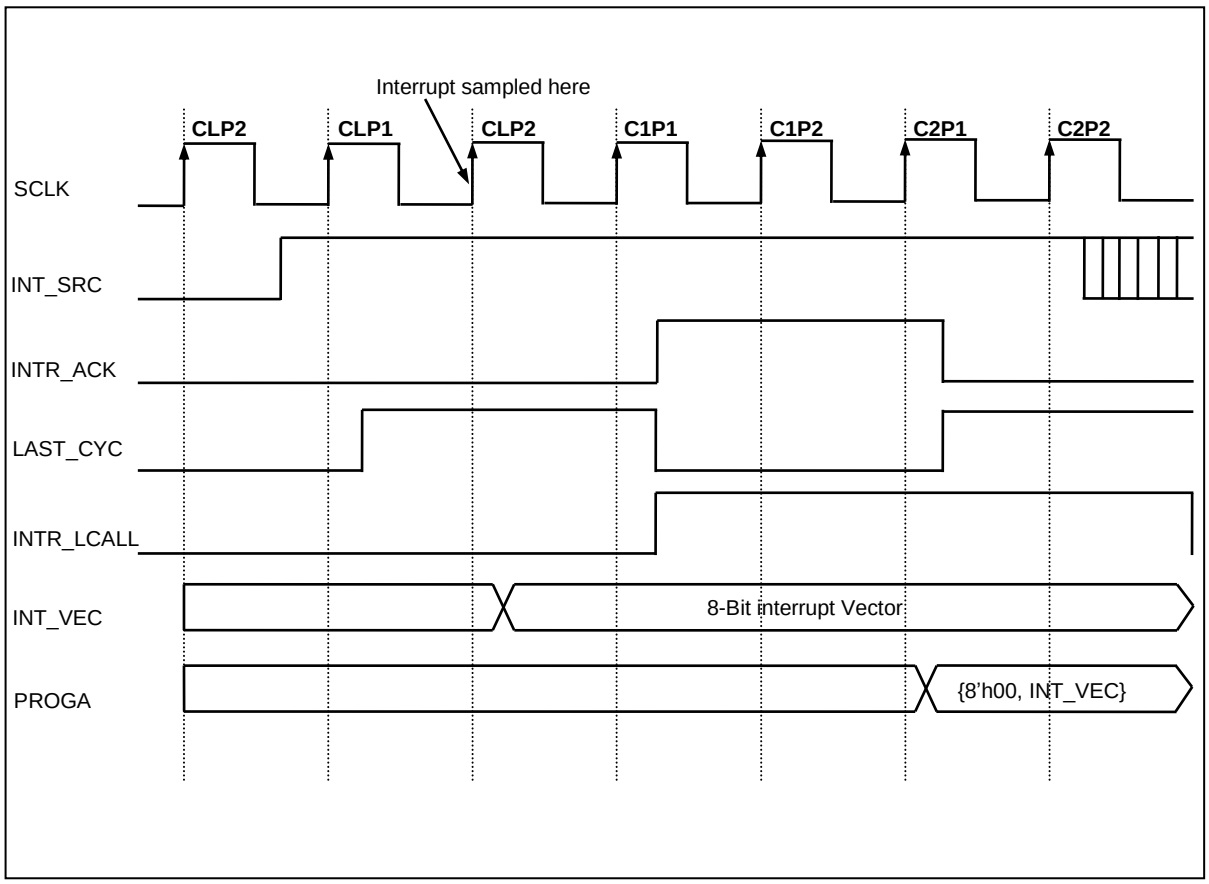


Figure 10.10 Timing Chart of Interrupt Acceptance and Interrupt Return Instruction

Interrupt sources are sampled at the last cycle of a command. If an interrupt source is detected the lower 8-bit of interrupt vector (INT_VEC) is decided. M8051W core makes interrupt acknowledge at the first cycle of a command, and executes long call to jump to interrupt service routine.

Note) command cycle CLPx: L=Last cycle, 1=1st cycle or 1st phase, 2=2nd cycle or 2nd phase

10.12 Interrupt Register Overview

10.12.1 Interrupt Enable Register (IE, IE1, IE2, IE3)

Interrupt enable register consists of global interrupt control bit (EA) and peripheral interrupt control bits. Total 24 peripherals are able to control interrupt.

10.12.2 Interrupt Priority Register (IP, IP1)

The 24 interrupts are divided into 6 groups which have each 4 interrupt sources. A group can be assigned 4 levels interrupt priority using interrupt priority register. Level 3 is the highest priority, while level 0 is the lowest priority. After a reset IP and IP1 are cleared to '00H'. If interrupts have the same priority level, lower number interrupt is served first.

10.12.3 External Interrupt Flag Register (EIFLAG)

The external interrupt flag register (EIFLAG) is set to '1' when the external interrupt generating condition is satisfied. The flag is cleared when the interrupt service routine is executed. Alternatively, the flag can be cleared by writing '0' to it.

10.12.4 External Interrupt Polarity Register (EIPOL)

The external interrupt polarity register (EIPOL) determines the edge of interrupt (rising, falling and both edge).

10.12.5 Register Map

Table 10-3 Interrupt Register Map

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IP	B8H	R/W	00H	Interrupt Polarity Register
IP1	F8H	R/W	00H	Interrupt Polarity Register 1
EIFLAG	B0H	R/W	00H	External Interrupt Flag Register
EIPOL	B1H	R/W	00H	External Interrupt Polarity Register

10.13 Interrupt Register Description

The interrupt register is used for controlling interrupt functions. Also it has external interrupt control registers. The interrupt register consists of interrupt enable register (IE), interrupt enable register 1 (IE1), interrupt enable register 2 (IE2) and interrupt enable register 3 (IE3). For external interrupt, it consists of external interrupt flag register (EIFLAG), external interrupt polarity register (EIPOL).

10.13.1 Register Description for Interrupt

IE (Interrupt Enable Register) : A8H

7	6	5	4	3	2	1	0
EA	-	-	-	-	INT2E	INT1E	INT0E
R/W	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

EA	Enable or Disable All Interrupt bits	
	0	All Interrupt disable
	1	All Interrupt enable
INT2E	Enable or Disable External Interrupt 2 (EINT2)	
	0	Disable
	1	Enable
INT1E	Enable or Disable External Interrupt 1 (EINT1)	
	0	Disable
	1	Enable
INT0E	Enable or Disable External Interrupt 0 (EINT0)	
	0	Disable
	1	Enable

IE1 (Interrupt Enable Register 1): A9H

7	6	5	4	3	2	1	0
-	-	INT11E	-	-	-	-	-
-	-	R/W	-	-	-	-	-

Initial value: 00H

INT11E	Enable or Disable PWM Generator Interrupt	
	0	Disable
	1	Enable

IE2 (Interrupt Enable Register 2) : AAH

7	6	5	4	3	2	1	0
-	-	-	-	-	INT14E	INT13E	-
-	-	-	-	-	R/W	R/W	-

Initial value : 00H

INT14E Enable or Disable Timer 1 match Interrupt
0 Disable
1 Enable

INT13E Enable or Disable Timer 0 match Interrupt
0 Disable
1 Enable

IE3 (Interrupt Enable Register 3) : ABH

7	6	5	4	3	2	1	0
-	-	-	INT22E	INT21E	-	-	-
-	-	-	R/W	R/W	-	-	-

Initial value : 00H

INT22E Enable or Disable BIT Interrupt
0 Disable
1 Enable

INT21E Enable or Disable WDT Interrupt
0 Disable
1 Enable

IP (Interrupt Priority Register) : B8H

7	6	5	4	3	2	1	0
-	-	IP5	IP4	IP3	IP2	IP1	IP0
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP1 (Interrupt Priority Register 1) : F8H

7	6	5	4	3	2	1	0
-	-	IP15	IP14	IP13	IP12	IP11	IP10
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP[5:0], IP1[5:0] Select Interrupt Group Priority

IP1x	IPx	Description
0	0	level 0 (lowest)
0	1	level 1
1	0	level 2
1	1	level 3 (highest)

EIFLAG (External Interrupt Flag Register) : B0H

7	6	5	4	3	2	1	0
-	-	-	-	-	FLAG2	FLAG1	FLAG0
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

FLAG[2:0] When an External Interrupt is occurred, the flag becomes '1'. The flag is cleared by writing '0' to the bit or automatically cleared by INT_ACK signal.

0 External Interrupt not occurred

1 External Interrupt occurred

EIPOL (External Interrupt Polarity Register): B1H

7	6	5	4	3	2	1	0
-	-	POL2		POL1		POL0	
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

EIPOL[5:0] External Interrupt (EINT2/EINT1/EINT0) Polarity Selection

POLn[1:0]		Description
0	0	No Interrupt at any edge
0	1	Interrupt on rising edge
1	0	Interrupt on falling edge
1	1	Interrupt on both of rising and falling edge

Where n = 0, 1, and 2

11. Peripheral Hardware

11.1 Clock Generator

11.1.1 Overview

As shown in Figure 11.1, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. The default system clock is 1MHz INT-RC oscillator and the default division rate is eight. In order to stabilize system internally, it is used 1MHz INT-RC oscillator on POR.

- Calibrated Internal RC Oscillator (8 MHz)
  . INT-RC OSC/1 (8 MHz)
  . INT-RC OSC/2 (4 MHz)
  . INT-RC OSC/4 (2 MHz)
  . INT-RC OSC/8 (1 MHz, Default system clock)

11.1.2 Block Diagram

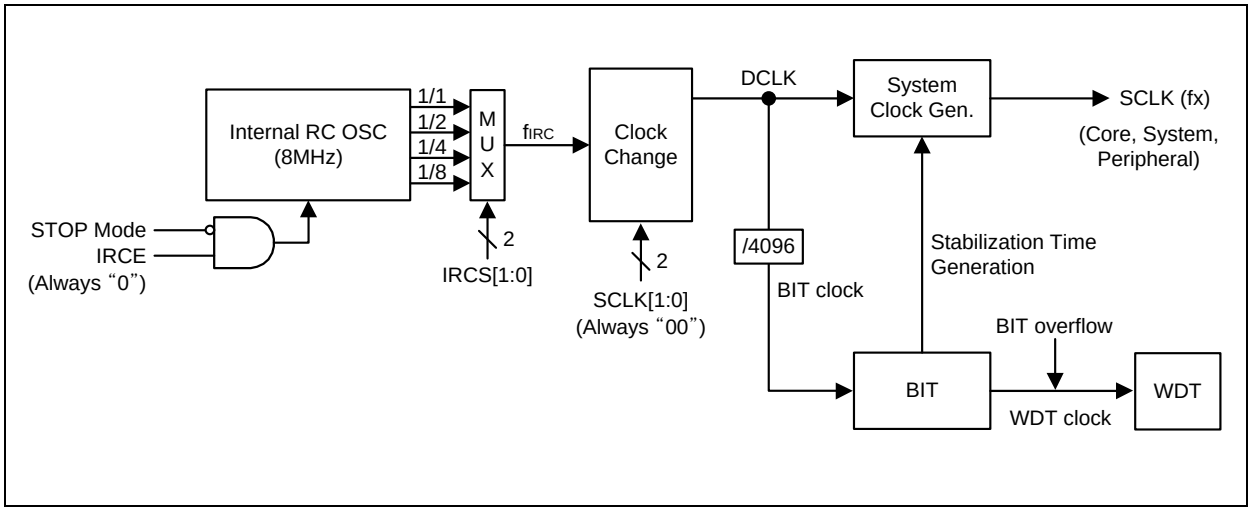


Figure 11.1 Clock Generator Block Diagram

11.1.3 Register Map

Table 11-1 Clock Generator Register Map

Name	Address	Dir	Default	Description
SCCR	8AH	R	00H	System and Clock Control Register
OSCCR	C8H	R/W	00H	Oscillator Control Register

11.1.4 Clock Generator Register Description

The clock generator register uses clock control for system operation. The clock generation consists of system and clock control register(SCCR) and oscillator control register(OSCCR).

11.1.5 Register Description for Clock Generator

SCCR (System and Clock Control Register) : 8AH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	SCLK1	SCLK0
-	-	-	-	-	-	R	R

Initial value : 00H

SCLK [1:0] System Clock Selection Bit

SCLK1	SCLK0	Description
0	0	INT RC OSC for system clock
Other value		Not available

NOTE) These bits are always “00” by hardware.

OSCCR (Oscillator Control Register) : C8H

7	6	5	4	3	2	1	0
-	-	-	IRCS1	IRCS0	IRCE	-	-
-	-	-	R/W	R/W	R	-	-

Initial value : 00H

IRCS[1:0] Internal RC Oscillator Post-divider Selection

IRCS1	IRCS0	Description
0	0	INT-RC/8 (1MHz)
0	1	INT-RC/4 (2MHz)
1	0	INT-RC/2 (4MHz)
1	1	INT-RC/1 (8MHz)

IRCE Control the Operation of the Internal RC Oscillator

0	Enable operation of INT-RC OSC
1	Not available

NOTE) This bit is always “0” by hardware.

11.2 Basic Interval Timer

11.2.1 Overview

The MC96P0202 has one 8-bit basic interval timer that is free-run and can't stop. Block diagram is shown in Figure 11.2. In addition, the basic interval timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITIFR).

The MC96P0202 has these basic interval timer (BIT) features:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As timer function, timer interrupt occurrence

11.2.2 Block Diagram

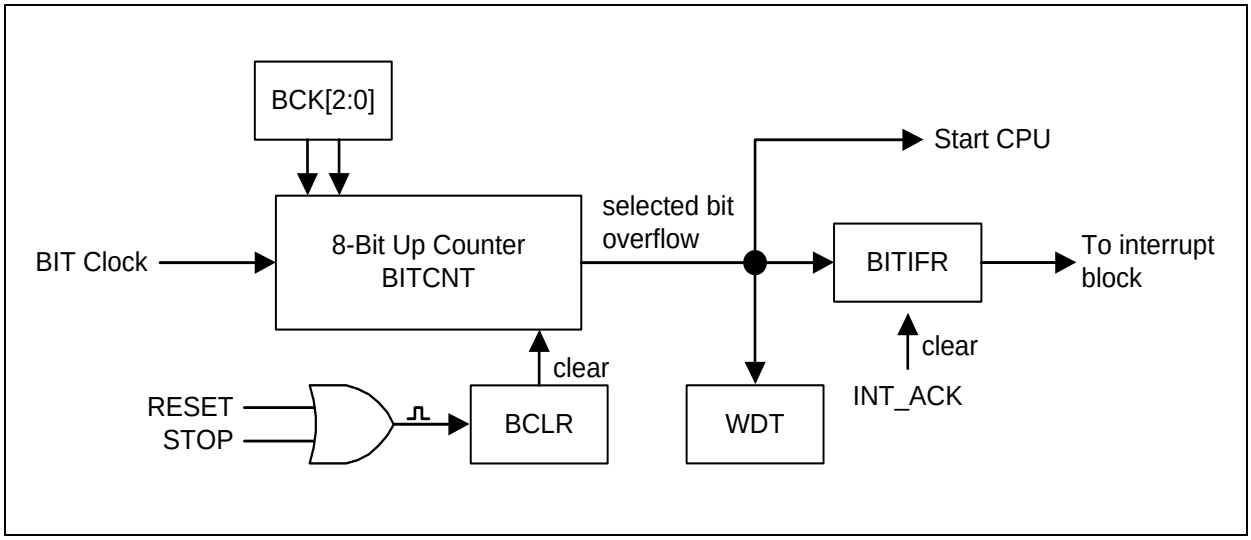


Figure 11.2 Basic Interval Timer Block Diagram

11.2.3 Register Map

Table 11-2 Basic Interval Timer Register Map

Name	Address	Dir	Default	Description
BITCNT	8CH	R	00H	Basic Interval Timer Counter Register
BITCR	8BH	R/W	03H	Basic Interval Timer Control Register

11.2.4 Basic Interval Timer Register Description

The basic interval timer register consists of basic interval timer counter register (BITCNT) and basic interval timer control register (BITCR). If BCLR bit is set to '1', BITCNT becomes '0' and then counts up. After 1 machine cycle, BCLR bit is cleared to '0' automatically.

11.2.5 Register Description for Basic Interval Timer

BITCNT (Basic Interval Timer Counter Register) : 8CH

7	6	5	4	3	2	1	0
BITCNT7	BITCNT6	BITCNT5	BITCNT4	BITCNT3	BITCNT2	BITCNT1	BITCNT0
R	R	R	R	R	R	R	R

Initial value : 00H

BITCNT[7:0] BIT Counter

BITCR (Basic Interval Timer Control Register) : 8BH

7	6	5	4	3	2	1	0
BITIFR	-	-	-	BCLR	BCK2	BCK1	BCK0
R/W	-	-	-	R/W	R/W	R/W	R/W

Initial value : 03H

BITIFR When BIT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 BIT interrupt no generation

1 BIT interrupt generation

BCLR If this bit is written to '1', BIT Counter is cleared to '0'

0 Free Running

1 Clear Counter

BCK[2:0] Select BIT overflow period

BCK2	BCK1	BCK0	Description
0	0	0	Bit 0 overflow (BIT Clock * 2)
0	0	1	Bit 1 overflow (BIT Clock * 4)
0	1	0	Bit 2 overflow (BIT Clock * 8)
0	1	1	Bit 3 overflow (BIT Clock * 16) (default)
1	0	0	Bit 4 overflow (BIT Clock * 32)
1	0	1	Bit 5 overflow (BIT Clock * 64)
1	1	0	Bit 6 overflow (BIT Clock * 128)
1	1	1	Bit 7 overflow (BIT Clock * 256)

11.3 Watch Dog Timer

11.3.1 Overview

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTCR[6] bit. If WDTCR[5] is written to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDTCNT, the interrupt request flag is generated. This can be used as watchdog timer interrupt or reset of CPU in accordance with the bit WDTRSON.

The input clock source of watch dog timer is the BIT overflow. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTDR set value. The equation can be described as

WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)

11.3.2 WDT Interrupt Timing Waveform

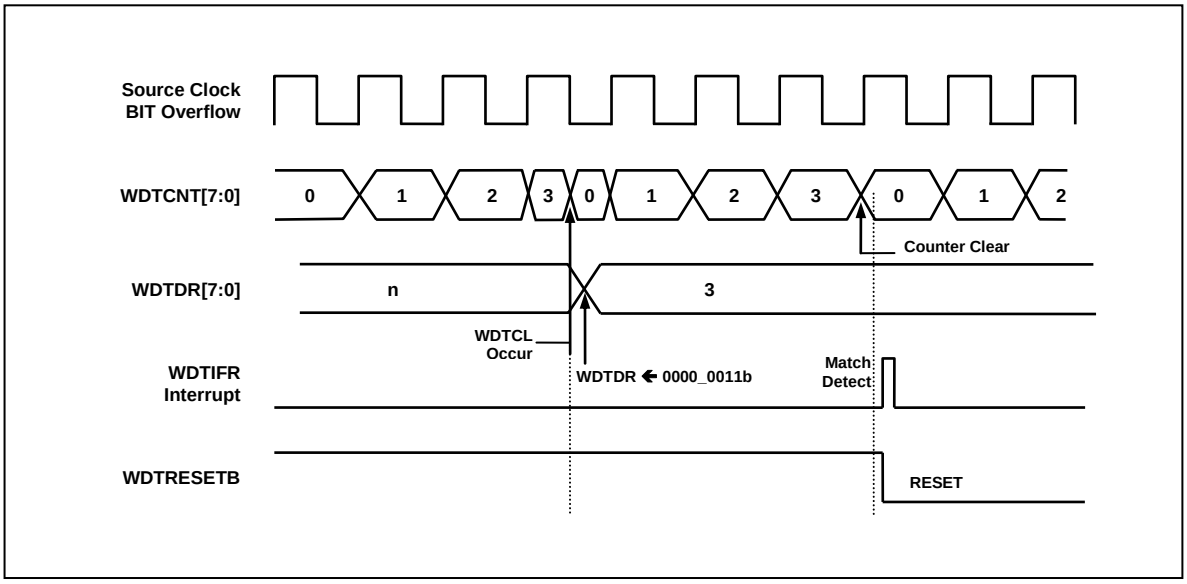


Figure 11.3 Watch Dog Timer Interrupt Timing Waveform

11.3.3 Block Diagram

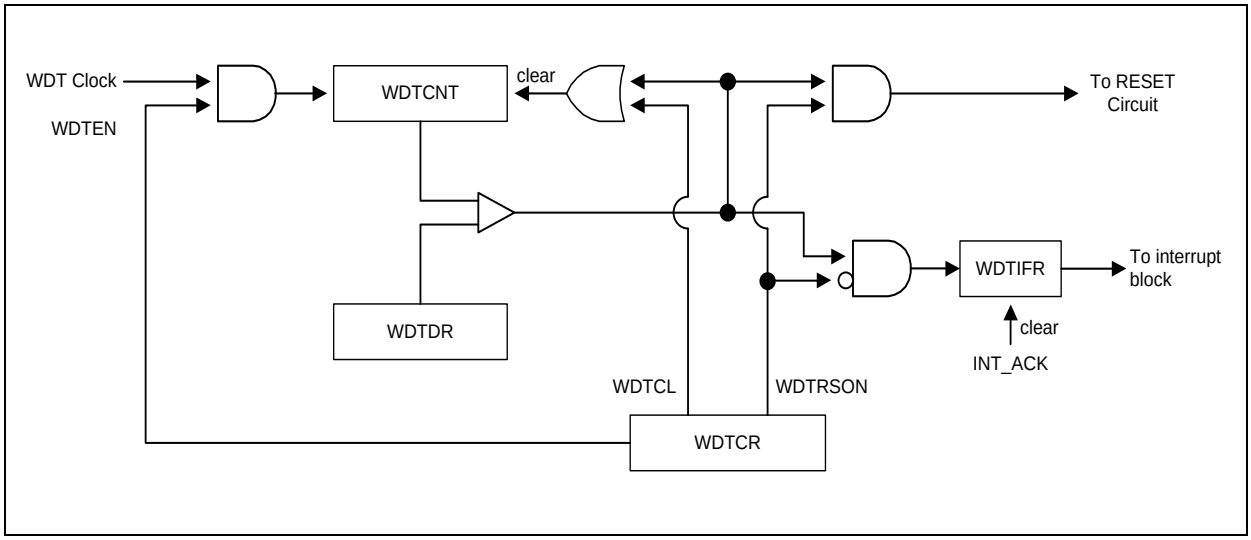


Figure 11.4 Watch Dog Timer Block Diagram

11.3.4 Register Map

Table 11-3 Watch Dog Timer Register Map

Name	Address	Dir	Default	Description
WDTCNT	8EH	R	00H	Watch Dog Timer Counter Register
WDTDR	8EH	W	FFH	Watch Dog Timer Data Register
WDTCR	8DH	R/W	00H	Watch Dog Timer Control Register

11.3.5 Watch Dog Timer Register Description

The watch dog timer register consists of watch dog timer counter register (WDTCNT), watch dog timer data register (WDTDR), and watch dog timer control register (WDTCR).

11.3.6 Register Description for Watch Dog Timer

WDTCNT (Watch Dog Timer Counter Register: Read Case) : 8EH

7	6	5	4	3	2	1	0
WDTCNT7	WDTCNT6	WDTCNT5	WDTCNT4	WDTCNT3	WDTCNT2	WDTCNT1	WDTCNT0
R	R	R	R	R	R	R	R

Initial value : 00H

WDTCNT[7:0] WDT Counter

WDTDR (Watch Dog Timer Data Register: Write Case) : 8EH

7	6	5	4	3	2	1	0
WDTDR7	WDTDR6	WDTDR5	WDTDR4	WDTDR3	WDTDR2	WDTDR1	WDTDR0
W	W	W	W	W	W	W	W

Initial value : FFH

WDTDR[7:0] Set a period
WDT Interrupt Interval=(BIT Interrupt Interval) x(WDTDR Value+1)
Note) Do not write “0” in the WDTDR register.

WDTCR (Watch Dog Timer Control Register) : 8DH

7	6	5	4	3	2	1	0
WDTEN	WDTRSON	WDTCL	-	-	-	-	WDTIFR
R/W	R/W	R/W	-	-	-	-	R/W

Initial value : 00H

WDTEN Control WDT Operation
0 Disable
1 Enable

WDTRSON Control WDT RESET Operation
0 Free Running 8-bit timer
1 Watch Dog Timer RESET ON

WDTCL Clear WDT Counter
0 Free Run
1 Clear WDT Counter (auto clear after 1 Cycle)

WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.
0 WDT Interrupt no generation
1 WDT Interrupt generation

11.4 Timer 0

11.4.1.1 Overview

The 8-bit Timer 0 consists of multiplexer, Timer 0 counter register, Timer 0 data register, and Timer 0 control register (T0CNT, T0DR, T0CR). It can be used as an internal 8-bit timer/counter 0.

The 8-bit Timer 0 is able to use the divided clock of the system clock selected from prescaler output. T1M (timer 1 match signal) can be also used as the clock source of Timer 0.

11.4.2 Block Diagram

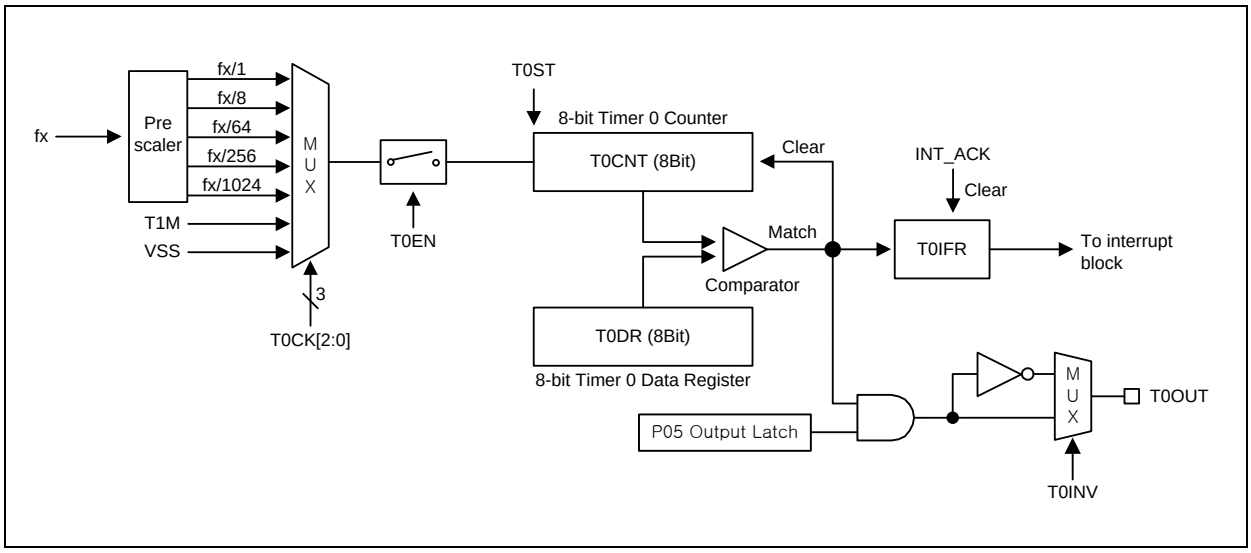


Figure 11.5 8-Bit Timer 0 Block Diagram

11.4.3 Register Map

Table 11-4 Timer 0 Register Map

Name	Address	Dir	Default	Description
T0CNT	B3H	R	00H	Timer 0 Counter Register
T0DR	B4H	R/W	FFH	Timer 0 Data Register
T0CR	90H	R/W	00H	Timer 0 Control Register

11.4.3.1 Timer/Counter 0 Register Description

The timer/counter 0 register consists of Timer 0 counter register (T0CNT), Timer 0 data register (T0DR), and Timer 0 control register (T0CR).

11.4.3.2 Register Description for Timer/Counter 0

T0CNT (Timer 0 Counter Register) : B3H

7	6	5	4	3	2	1	0
T0CNT7	T0CNT6	T0CNT5	T0CNT4	T0CNT3	T0CNT2	T0CNT1	T0CNT0
R	R	R	R	R	R	R	R

Initial value : 00H

T0CNT[7:0] T0 Counter

T0DR (Timer 0 Data Register) : B4H

7	6	5	4	3	2	1	0
T0DR7	T0DR6	T0DR5	T0DR4	T0DR3	T0DR2	T0DR1	T0DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T0DR[7:0] T0 Data

T0CR (Timer 0 Control Register) : 90H

7	6	5	4	3	2	1	0
T0EN	T0IFR	T0INV	T0CK2	T0CK1	T0CK0	T0CN	T0ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T0EN Control Timer 0

0 Timer 0 disable

1 Timer 0 enable

T0IFR When T0 Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 T0 Interrupt no generation

1 T0 Interrupt generation

T0INV Timer 0 Output Inversion Control

0 Timer 0 output not inverted

1 Timer 0 output inverted

T0CK[2:0] Select Timer 0 clock source. fx is system clock frequency

T0CK2	T0CK1	T0CK0	Description
0	0	0	Counter stop
0	0	1	fx/1
0	1	0	fx/8
0	1	1	fx/64
1	0	0	fx/256
1	0	1	fx/1024
1	1	0	T1M (Timer 1 Match signal)
1	1	1	Not available

T0CN Control Timer 0 Counter pause/continue

0 Temporary count stop

1 Continue count

T0ST Control Timer 0 start/stop

0 Counter stop

1 Clear counter and start

11.5 Timer 1

11.5.1 Overview

The 8-bit timer 1 consists of multiplexer, timer 1 counter register, timer 1 data high/low register, and timer 1 control register (T1CNT, T1DRH, T1DRL, T1CR) . For carrier mode, it has the carrier control register (CARCR).

It has two operating modes:

- 8-bit timer/counter mode
- 8-bit carrier mode

The timer/counter 1 can be clocked by an internal clock source. The clock source is selected by clock selection logic which is controlled by the clock selection bits (T1CK[2:0]).

- TIMER1 clock source: fx/1, fx/2, fx/8, fx/16, fx/32, fx/64, fx/256, fx/512

In the carrier mode, Timer 1 can be used to generate the carrier frequency or a remote controller signal. Timer 1 can output the comparison result between T1CNT & T1DRH/L and carrier frequency through REM port. T1CNT value is cleared by hardware.

Table 11-5 Timer 1 Operating Modes

T1EN	PFSR01	CAR1	T1CK[2:0]	CMOD	Timer 1
1	1	0	XXX	0	8 Bit Timer/Counter
1	1	1	XXX	0	8 Bit Carrier (One-shot)
1	1	1	XXX	1	8 Bit Carrier (Repeat)

11.5.2 8-Bit Timer/Counter 1 Mode

The 8-bit timer/counter mode is selected by control register as shown in Figure 11.6.

The 8-bit timer have counter and data register. The counter register is increased by internal clock source. Timer 1 can use the input clock with one of 1, 2, 8, 16, 32, 64, 256, and 512 prescaler division rates (T1CK[2:0]). When the value of T1CNT and the T1DRH is identical in Timer 1, a match signal is generated and the interrupt of Timer 1 occurs. The match signal generates a timer 1 interrupt and clear the counter. The timer 1 interval can be output through REM port.

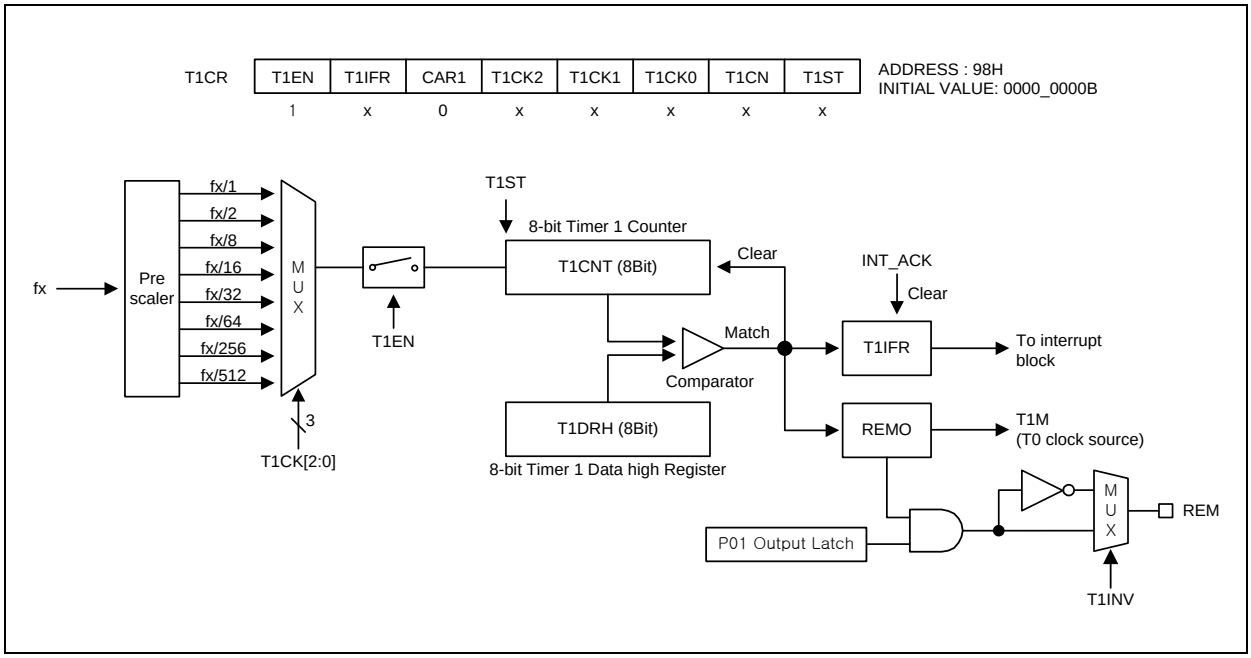


Figure 11.6 8-Bit Timer/Counter Mode for Timer 1

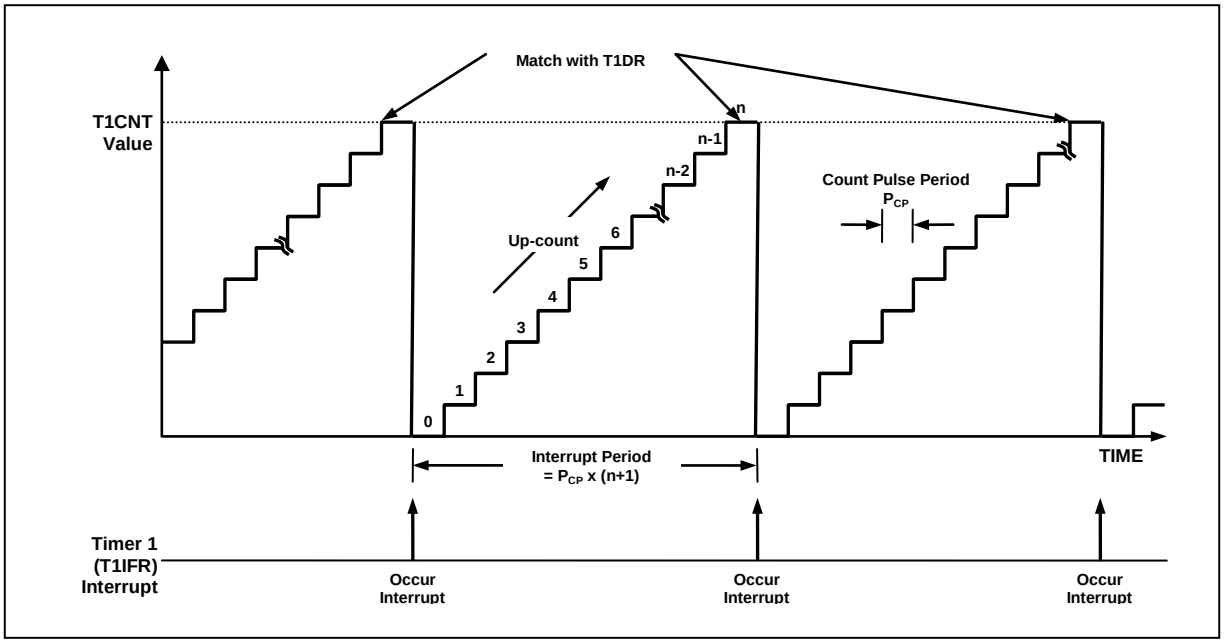


Figure 11.7 8-Bit Timer/Counter 1 Example

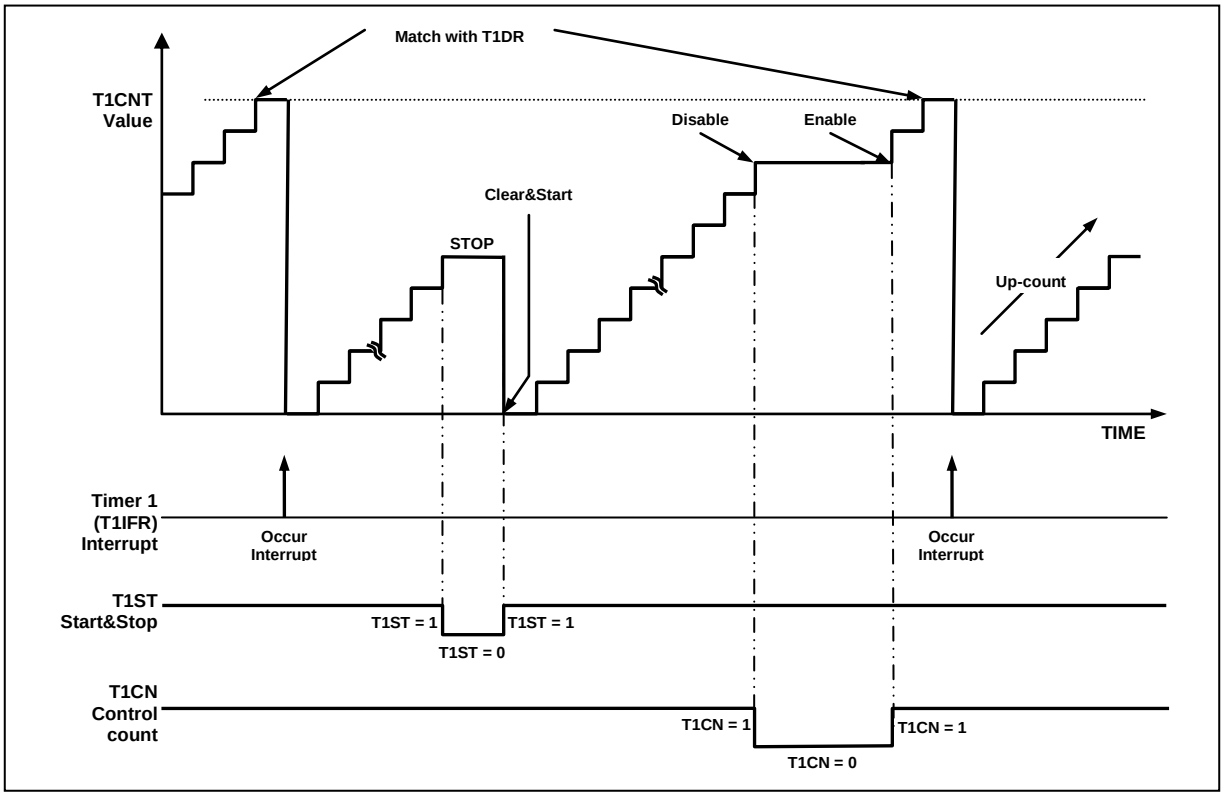


Figure 11.8 8-Bit Timer/Counter 1 Counter Operation

11.5.3 8-Bit Timer 1 Carrier Frequency Mode.

The carrier frequency and the pulse of data are calculated by the formula in the following sheet .The Figure 11.9 shows the block diagram of Timer 1 for carrier frequency mode.

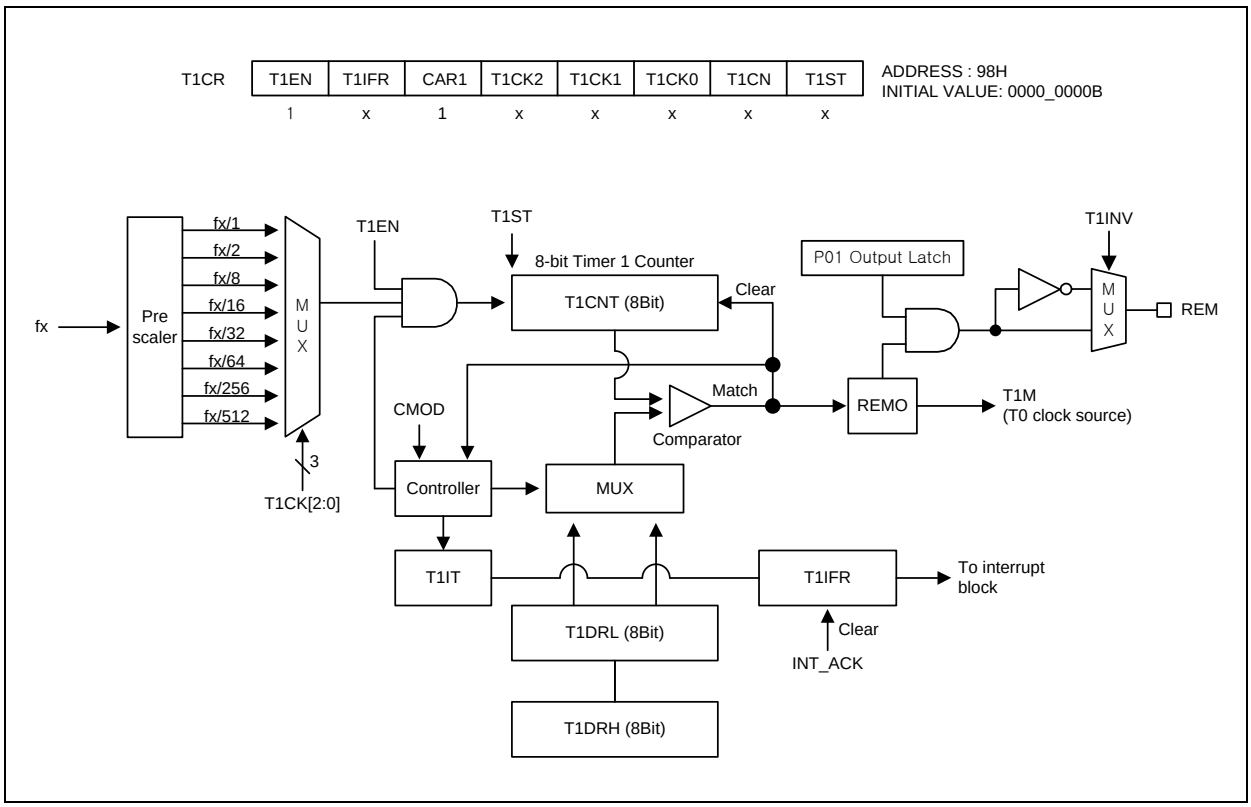
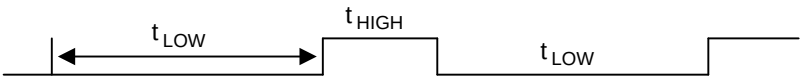


Figure 11.9 8-Bit Carrier Frequency Mode for Timer 1

Note) When one of T1DRH and T1DRL values is “00H”, the carrier frequency generator (REM) output always becomes a “High” or “Low”. At that time, Timer 1 Interrupt Flag Bit (T1IFR) is not set.

11.5.4 Carrier Output Pulse Width Calculatins



To generate the above repeated waveform consisted of low period time (t_{LOW}), and high period time (t_{HIGH}).

When REMO = 0,

t_{LOW} = (T1DRL + 1) x 1/f_{T1}, 0H < T1DRL < 100H, where f_{T1} = The selected clock.

t_{HIGH} = (T1DRH + 1) x 1/f_{T1}, 0H < T1DRH < 100H, where f_{T1} = The selected clock.

When REMO = 1,

t_{LOW} = (T1DRH + 1) x 1/f_{T1}, 0H < T1DRH < 100H, where f_{T1} = The selected clock.

t_{HIGH} = (T1DRL + 1) x 1/f_{T1}, 0H < T1DRL < 100H, where f_{T1} = The selected clock.

To make t_{LOW} = 24 us and t_{HIGH} = 15 us. f_X = 4 MHz, f_{T1} = 4 MHz/4 = 1 MHz

When REMO = 0,

t_{LOW} = 24 us = (T1DRL + 1) /f_{T1} = (T1DRL + 1) x 1us, T1DRL = 22.

t_{HIGH} = 15 us = (T1DRH + 1) /f_{T1} = (T1DRH + 1) x 1us, T1DRH = 13.

When REMO = 1,

t_{LOW} = 24 us = (T1DRH + 1) / f_{T1} = (T1DRH + 1) x 1us, T1DRH = 22.

t_{HIGH} = 15 us = (T1DRL + 1) / f_{T1} = (T1DRL + 1) x 1us, T1DRL = 13.

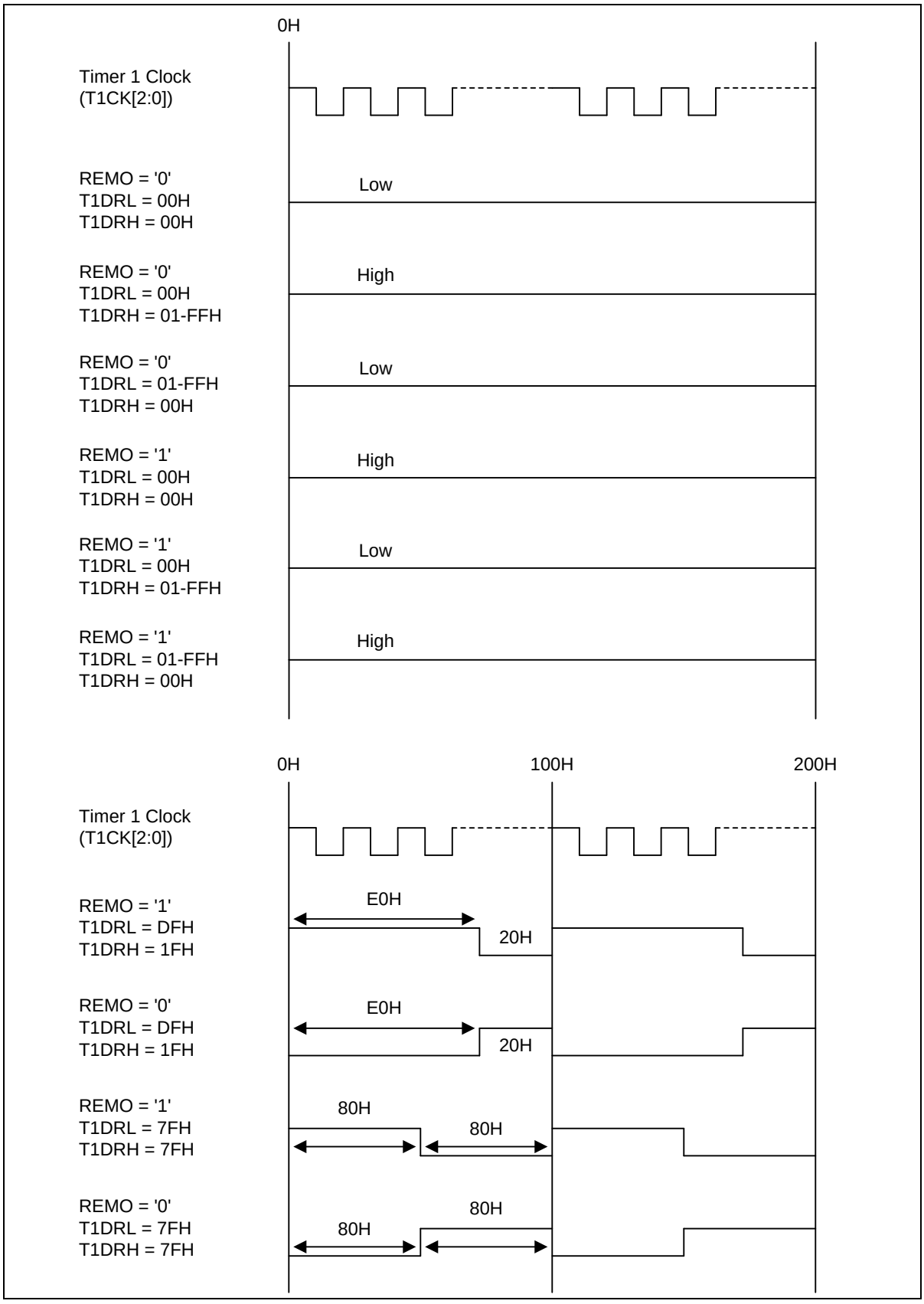


Figure 11.10 Carrier Output Waveforms in Repeat Mode for Timer 1

11.5.5 Block Diagram

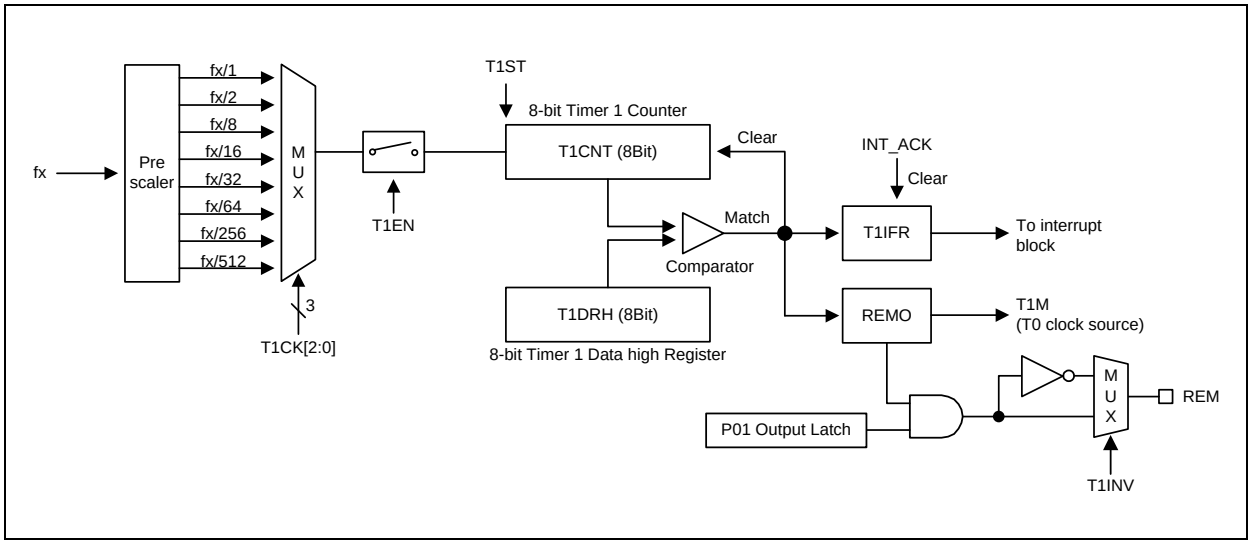


Figure 11.11 8-Bit Timer 1 Block Diagram

11.5.6 Register Map

Table 11-6 Timer 1 Register Map

Name	Address	Dir	Default	Description
T1CNT	BBH	R	00H	Timer 1 Counter Register
T1DRH	BDH	R/W	FFH	Timer 1 Data High Register
T1DRL	BCH	R/W	FFH	Timer 1 Data Low Register
T1CR	98H	R/W	00H	Timer 1 Control Register
CARCR	BEH	R/W	00H	Carrier Control Register

11.5.6.1 Timer/Counter 1 Register Description

The timer/counter 1 register consists of timer 1 counter register (T1CNT), timer 1 data high register (T1DRH), timer 1 data low register (T1DRL), timer 1 control register (T1CR) and carrier control register (CARCR).

11.5.6.2 Register description for Timer/Counter 1

T1CNT (Timer 1 Counter Register) : BBH

7	6	5	4	3	2	1	0
T1CNT7	T1CNT6	T1CNT5	T1CNT4	T1CNT3	T1CNT2	T1CNT1	T1CNT0
R	R	R	R	R	R	R	R

Initial value : 00H

T1CNT[7:0] T1 Counter

T1DRH (Timer 1 Data High Register) : BDH

7	6	5	4	3	2	1	0
T1DRH7	T1DRH6	T1DRH5	T1DRH4	T1DRH3	T1DRH2	T1DRH1	T1DRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T1DRH[7:0] T1 Data High

T1DRL (Timer 1 Data Low Register: Carrier mode only) : BCH

7	6	5	4	3	2	1	0
T1DRL7	T1DRL6	T1DRL5	T1DRL4	T1DRL3	T1DRL2	T1DRL1	T1DRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

T1DRL[7:0] T1 Data Low

T1CR (Timer 1 Control Register) : 98H

7	6	5	4	3	2	1	0
T1EN	T1IFR-	CAR1	T1CK2	T1CK1	T1CK0	T1CN	T1ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T1EN Control Timer 1

0 Timer 1 disable

1 Timer 1 enable

T1IFR When T1 Match Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT_ACK signal.

0 T1 match interrupt no generation

1 T1 match interrupt generation

CAR1 Control Timer 1 Operation mode

0 Timer/counter mode

1 Carrier mode

T1CK[2:0] Select Timer 1 Clock Source. fx is system clock frequency

T1CK2	T1CK1	T1CK0	Description
0	0	0	fx/1
0	0	1	fx/2
0	1	0	fx/8
0	1	1	fx/16
1	0	0	fx/32
1	0	1	fx/64
1	1	0	fx/256
1	1	1	fx/512

T1CN Control Timer 1 Counter pause/continue

0 Temporary count stop

1 Continue count

T1ST Control Timer 1 start/stop

0 Counter stop

1 Clear counter and start

CARCR (Carrier Control Register: Carrier mode only) : BEH

7	6	5	4	3	2	1	0
T1INV	-	T1IT1	T1IT0	-	-	CMOD	REMO
R/W	-	R/W	R/W	-	-	R/W	R/W

Initial value : 00H

T1INV Timer 1 Output Inversion Control.
This bit is effective at the timer mode, too.

0 Timer 1 output not inverted

1 Timer 1 output inverted

T1IT[1:0] T1 Interrupt Time Select

T1IT1	T1IT0	Description
0	0	Elapsed time for low data value
0	1	Elapsed time for high data value
1	0	Elapsed time for low and high data value
1	1	Not available

CMOD Carrier Frequency Mode Select

0 One-shot mode

1 Repeating mode

REMO REM Output Control

0 T1DRL→ Low width, T1DRH→ High width

1 T1DRL→ High width, T1DRH→ Low width

11.6 PWM Generator

11.6.1 Overview

The MC96P0202 has a high speed 8-bit PWM (Pulse Width Modulation) generator. The PWM generator has PWM0 and PWM1 pins with 8-bit resolution PWM output. These pins should be configured as a PWM output by set P0FSR[1] and P0FSR[2] to '1'. The PWMCNT runs up to "FFH" and then continues incrementing from "00H". It is the period of PWM. The duty of the PWM0 and PWM1 output is determined by the PWM0DR(PWM generator data register 0) and PWM1DR (PWM generator data register 1). The PWM interrupt is generated whenever a counter overflow occurs. PWMCNT value is cleared by software (PWMCC) bit or overflow.

11.6.2 Block Diagram

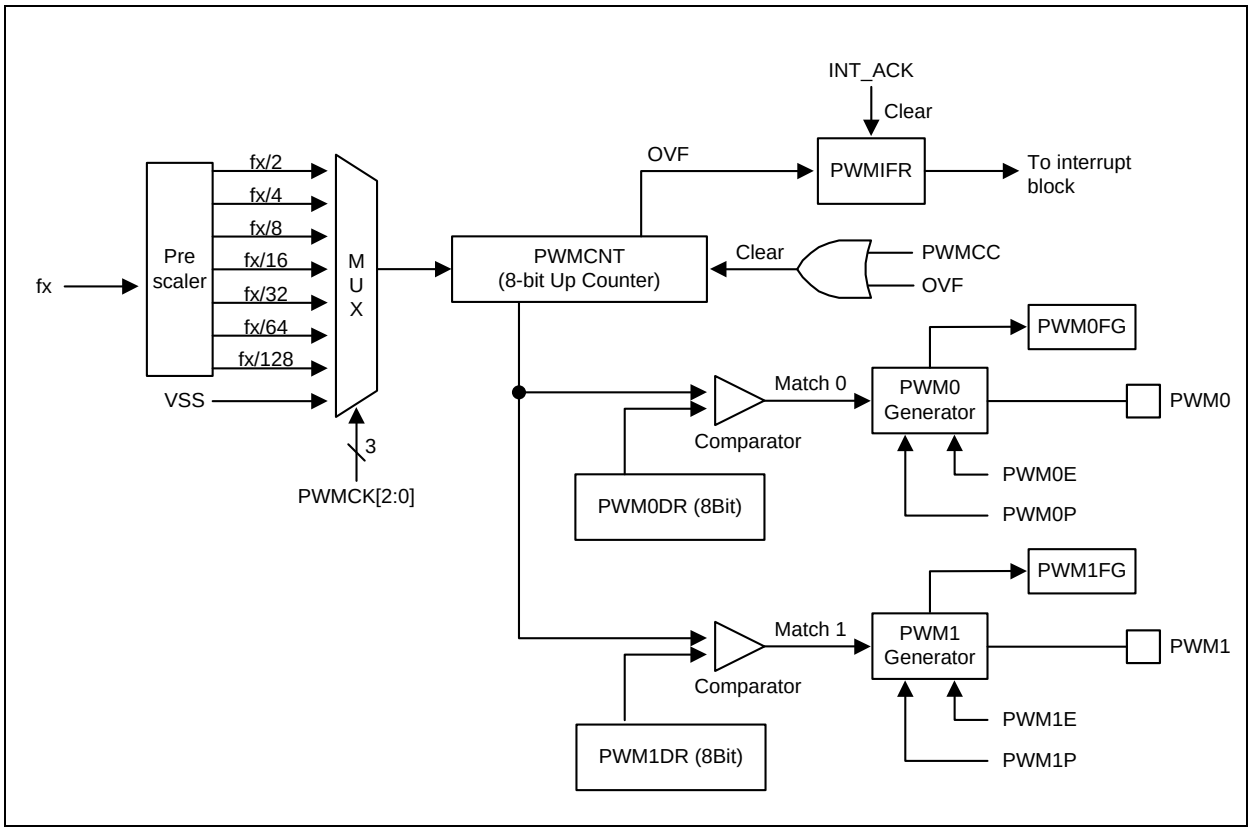


Figure 11.12 8-Bit PWM Generator Block Diagram

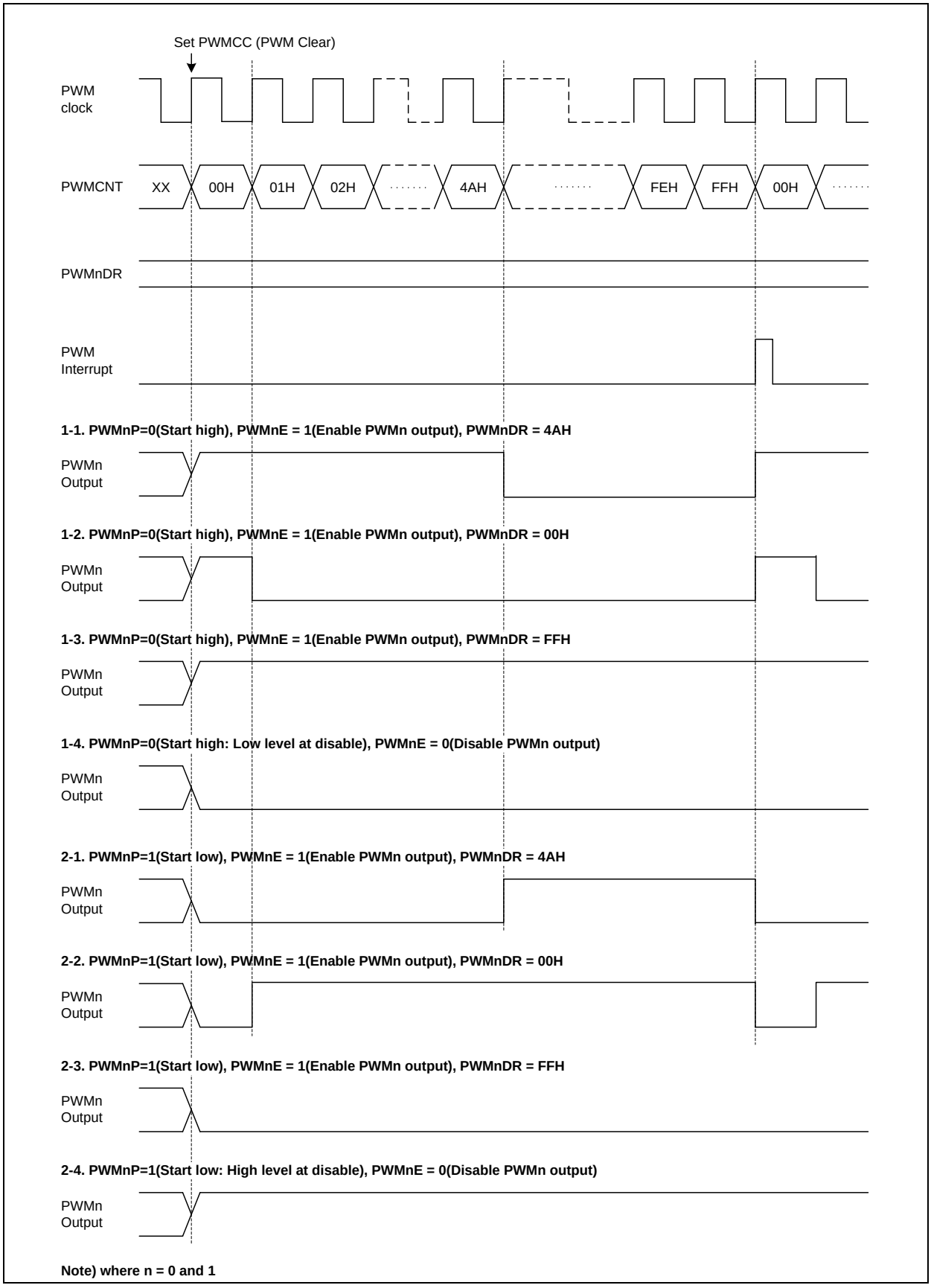


Figure 11.13 PWM Output Waveforms for PWM generator

11.6.3 Register Map

Table 11-7 PWM generator Register Map

Name	Address	Dir	Default	Description
PWMCNT	C3H	R	00H	PWM Generator Counter Register
PWM0DR	C4H	R/W	FFH	PWM Generator Data Register 0
PWM1DR	C5H	R/W	FFH	PWM Generator Data Register 1
PWMCR	A0H	R/W	00H	PWM Generator Control Register
PWMFGR	C0H	R/W	00H	PWM Generator Flag Register

11.6.3.1 PWM Generator Register Description

The PWM generator register consists of PWM generator counter register (PWMCNT), PWM generator data register 0(PWM0DR), PWM generator data register 1(PWM1DR), PWM generator control register (PWMCR), and PWM generator flag register(PWMFGR).

11.6.3.2 Register Description for PWM Generator

PWMCNT (PWM Generator Counter Register) : C3H

7	6	5	4	3	2	1	0
PWMCNT7	PWMCNT6	PWMCNT5	PWMCNT4	PWMCNT3	PWMCNT2	PWMCNT1	PWMCNT0
R	R	R	R	R	R	R	R

Initial value : 00H

PWMCNT[7:0] PWM Generator Counter

PWM0DR (PWM Generator Data Register 0) : C4H

7	6	5	4	3	2	1	0
PWM0DR7	PWM0DR6	PWM0DR5	PWM0DR4	PWM0DR3	PWM0DR2	PWM0DR1	PWM0DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

PWM0DR[7:0] PWM Generator 0 Data

PWM1DR (PWM Generator Data Register 1) : C5H

7	6	5	4	3	2	1	0
PWM1DR7	PWM1DR6	PWM1DR5	PWM1DR4	PWM1DR3	PWM1DR2	PWM1DR1	PWM1DR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

PWM1DR[7:0] PWM Generator 1 Data

PWMCR (PWM Generator Control Register) : A0H

7	6	5	4	3	2	1	0
PWM1E	PWM1P	PWM0E	PWM0P	PWMCC	PWMCK2	PWMCK1	PWMCK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PWM1E PWM1 Output Control
- 0 Disable PWM1 output
- 1 Enable PWM1 output

PWM1P PWM1 Polarity Selection
- 0 Start high (PWM1 is low level at disable)
- 1 Start low (PWM1 is high level at disable)

PWM0E PWM0 Output Control
- 0 Disable PWM0 output
- 1 Enable PWM0 output

PWM0P PWM0 Polarity Selection
- 0 Start high (PWM0 is low level at disable)
- 1 Start low (PWM0 is high level at disable)

PWMCC Clear PWM Generator Counter
- 0 No effect
- 1 Clear the PWM generator counter (When write, automatically cleared “0” after being cleared counter)

PWMCK[2:0] Select PWM generator clock source. fx is a system clock frequency

PWMCK2	PWMCK1	PWMCK0	Description
0	0	0	Counter stop
0	0	1	fx/2
0	1	0	fx/4
0	1	1	fx/8
1	0	0	fx/16
1	0	1	fx/32
1	1	0	fx/64
1	1	1	fx/128

PWMFGR (PWM Generator Flag Register) : C0H

7	6	5	4	3	2	1	0
-	PWMIFR	-	-	-	-	PWM1FG	PWM0FG
-	RW	-	-	-	-	R	R

Initial value : 00H

PWMIFR	When PWM Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.	
	0	PWM Interrupt no generation
	1	PWM Interrupt generation
PWM1FG	PWM1 Output Status Flag	
	0	PWM1 output is ‘0’
	1	PWM1 output is ‘1’
PWM0FG	PWM0 Output Status Flag	
	0	PWM0 output is ‘0’
	1	PWM0 output is ‘1’

11.7 Inverter Amplifier

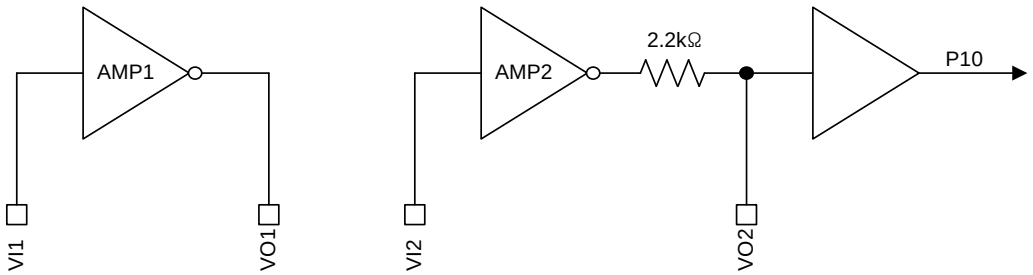
11.7.1 Overview

The MC96P0202 has two inverter amplifiers. These are used for amplifying input signals.

The amplifiers consist of the following components:

- Inverter Amplifier 1(VI1, VO1)
- Inverter Amplifier 2(VI2, VO2)

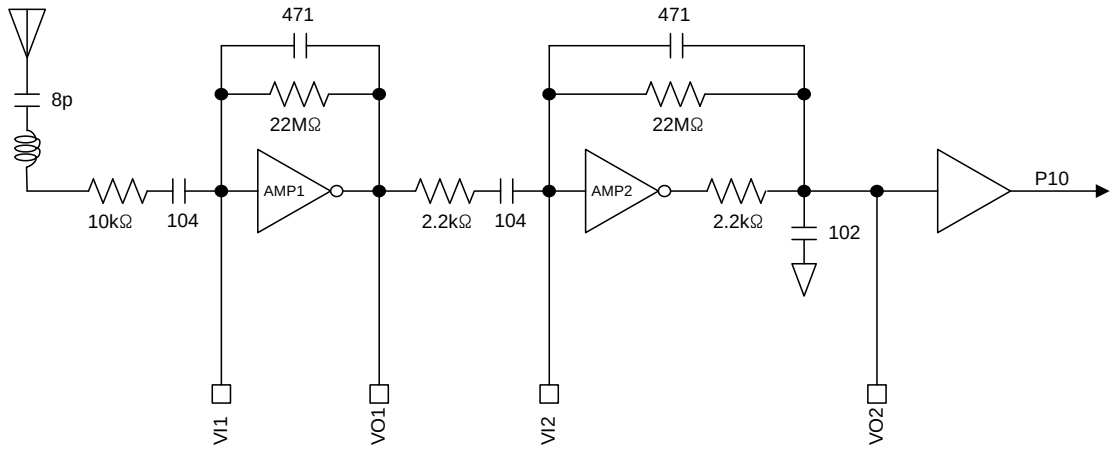
11.7.2 Block Diagram



Note) P10 is used for reading output of AMP2. So, this port should not be used for external input from VO2 pin.

Figure 11.14 Inverter Amplifier 1, 2 Block Diagram

11.7.3 Application Circuit



Note) P10 is used for reading output of AMP2. So, this port should not be used for external input from VO2 pin

Figure 11.15 Example Application Circuit for Inverter Amplifier 1, 2

12. Power Down Operation

12.1 Overview

The MC96P0202 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides two kinds of power saving functions, IDLE and STOP mode. In two modes, program is stopped.

12.2 Peripheral Operation in IDLE/STOP Mode

Table 12-1 Peripheral Operation during Power Down Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Stop
Timer0~1	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
PWM Generator	Operates Continuously	Stop
Internal OSC (8MHz)	Oscillation	Stop
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, External Interrupt

12.3 IDLE Mode

The power control register is set to '01h' to enter the IDLE Mode. In this mode, the internal oscillation circuits remain active. Oscillation continues and peripherals are operated normally but CPU stops. It is released by reset or interrupt. To be released by interrupt, interrupt should be enabled before IDLE mode. If using reset, because the device becomes initialized state, the registers have reset value.

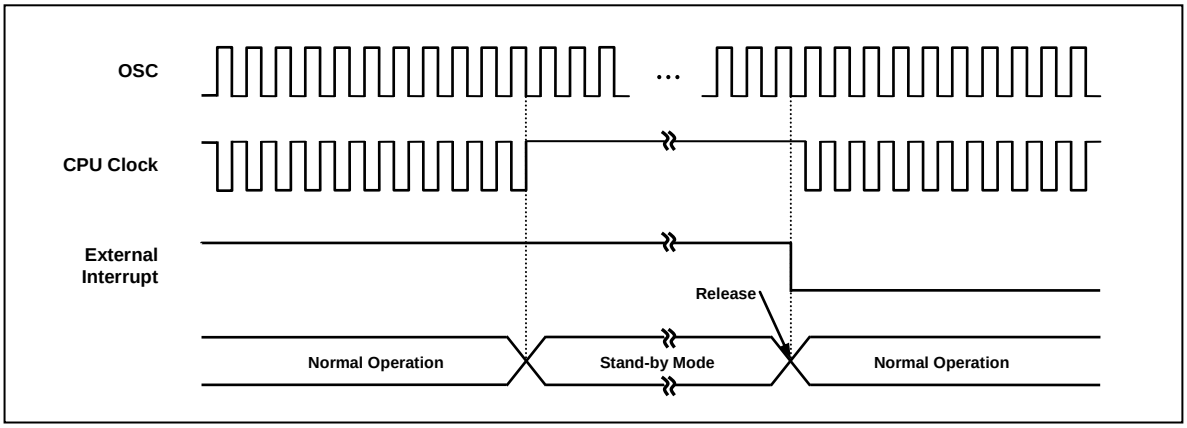


Figure 12.1 IDLE Mode Release Timing by External Interrupt

12.4 STOP Mode

The power control register is set to '03H' to enter the STOP Mode. In the stop mode, system clock(the internal RC oscillator) and peripheral clock is stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and control registers are held.

The source for exit from STOP mode is hardware reset and interrupts. The reset re-defines all the control registers.

When exit from STOP mode, enough oscillation stabilization time is required to normal operation. Figure 12.2 shows the timing diagram. When released from STOP mode, the Basic interval timer is activated on wake-up. Therefore, before STOP instruction, user must be set its relevant prescale divide ratio to have long enough time. This guarantees that oscillator has started and stabilized.

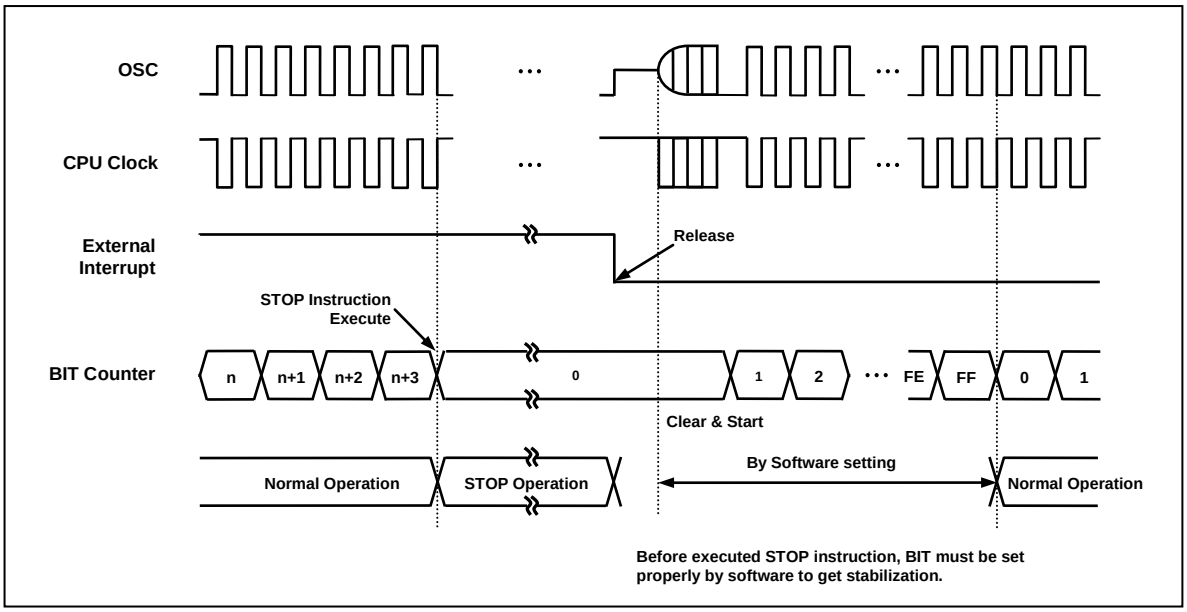


Figure 12.2 STOP Mode Release Timing by External Interrupt

12.5 Release Operation of STOP Mode

After STOP mode is released, the operation begins according to content of related interrupt register just before STOP mode start (Figure 12.3). If the global interrupt Enable Flag (IE.EA) is set to `1`, the STOP mode is released by the interrupt which each interrupt enable flag = `1` and the CPU jumps to the relevant interrupt service routine. Even if the IE.EA bit is cleared to '0', the STOP mode is released by the interrupt of which the interrupt enable flag is set to '1'.

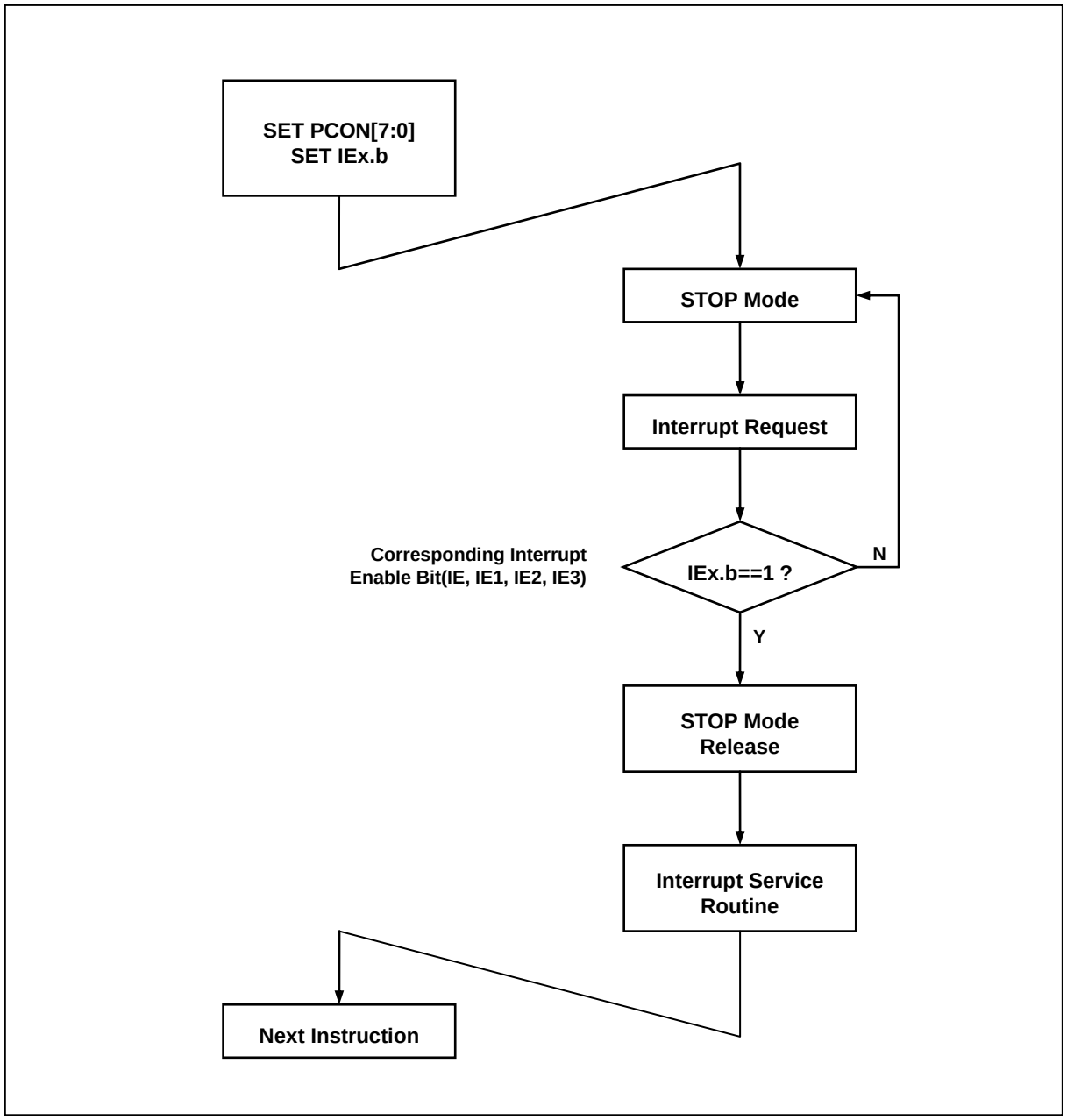


Figure 12.3 STOP Mode Release Flow

12.5.1 Register Map

Table 12-2 Power Down Operation Register Map

Name	Address	Dir	Default	Description
PCON	87H	R/W	00H	Power Control Register

12.5.2 Power Down Operation Register Description

The power down operation register consists of the power control register (PCON).

12.5.3 Register Description for Power Down Operation

PCON (Power Control Register) : 87H

7	6	5	4	3	2	1	0
PCON7	-	-	-	PCON3	PCON2	PCON1	PCON0
R/W	-	-	-	R/W	R/W	R/W	R/W

Initial value : 00H

PCON[7:0]	Power Control
01H	IDLE mode enable
03H	STOP mode enable

Notes) 1. To enter IDLE mode, PCON must be set to ‘01H’.

2. To enter STOP mode, PCON must be set to ‘03H’.
3. The PCON register is automatically cleared by a release signal in STOP/IDLE mode.
4. Three or more NOP instructions must immediately follow the instruction that make the device enter STOP/IDLE mode. Refer to the following examples.

```
Ex1)  MOV   PCON, #01H    ; IDLE mode
      NOP
      NOP
      NOP
       •
       •
       •
```

```
Ex2)  MOV   PCON, #03H    ; STOP mode
      NOP
      NOP
      NOP
       •
       •
       •
```

13. RESET

13.1 Overview

The The following is the hardware setting value.

Table 13-1 Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

13.2 Reset Source

The MC96P0202 has four types of reset sources. The following is the reset sources.

- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset
- OCD Reset

13.3 RESET Block Diagram

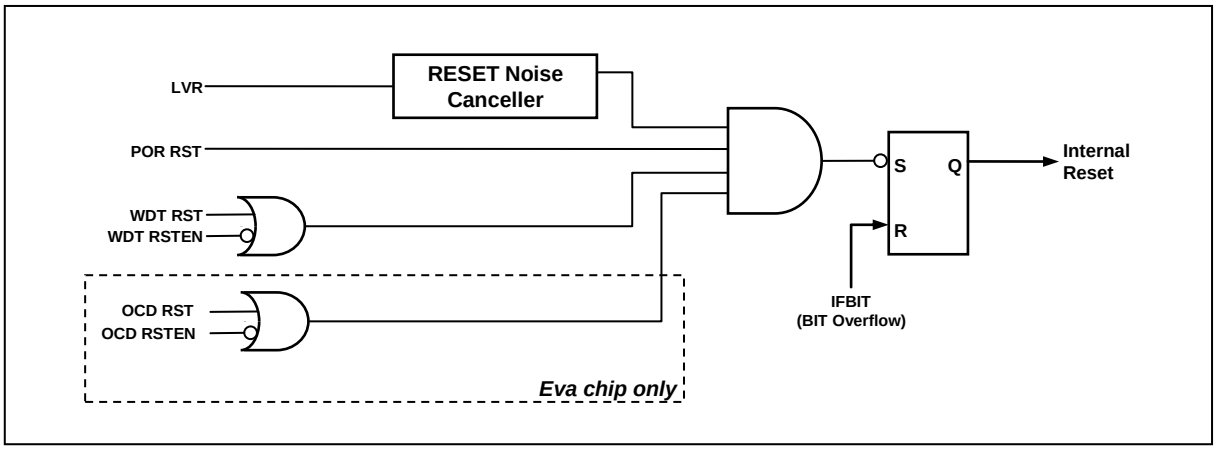


Figure 13.1 RESET Block Diagram

13.4 RESET Noise Canceller

The Figure 13.2 is the noise canceller diagram for noise cancellation of RESET. It has the noise cancellation value of about 2us (@V_{DD}=5V) to the low input of system reset.

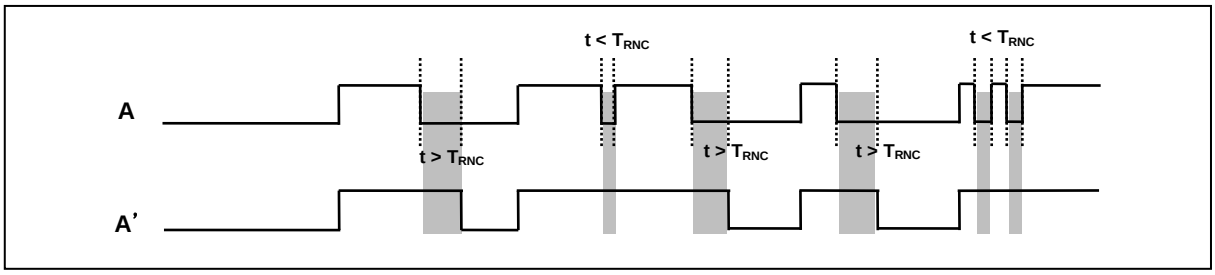


Figure 13.2 Reset noise canceller timer diagram

13.5 Power On RESET

When rising device power, the POR (Power On Reset) has a function to reset the device. If POR is used, it executes the device RESET function instead of the RESET IC or the RESET circuits.

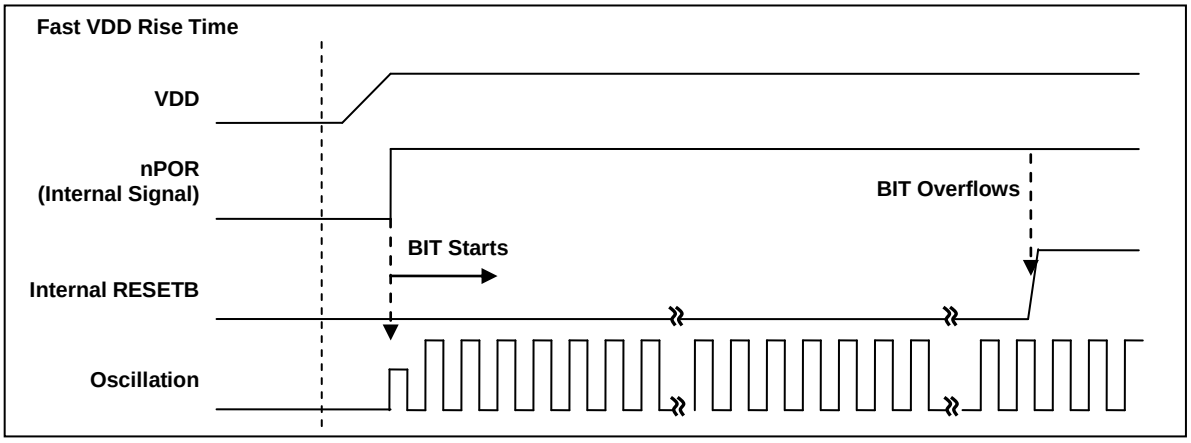


Figure 13.3 Fast VDD Rising Time

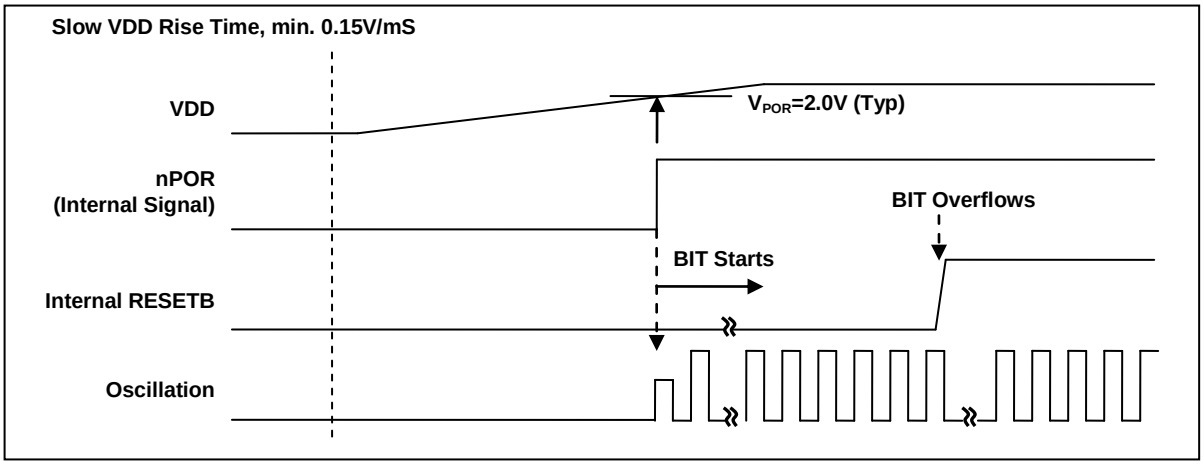


Figure 13.4 Internal RESET Release Timing On Power-Up

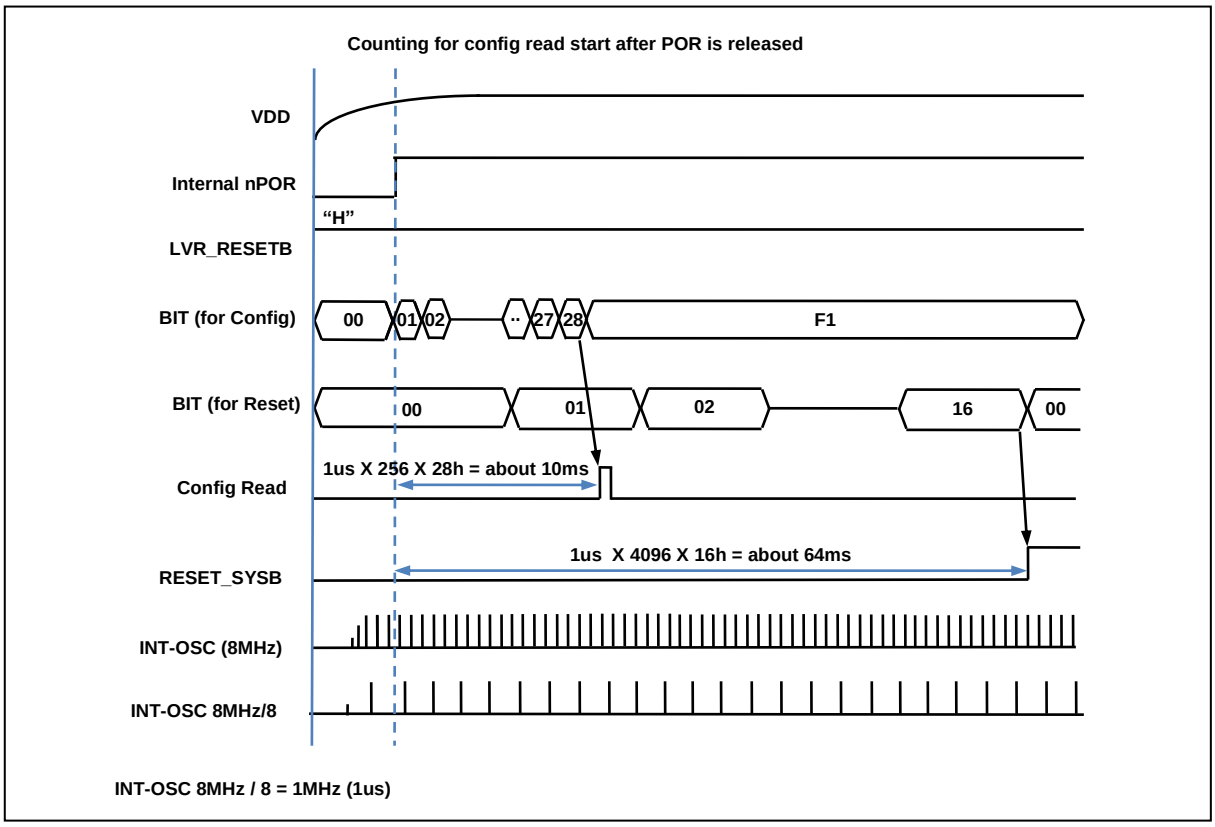


Figure 13.5 Configuration Timing when Power-on

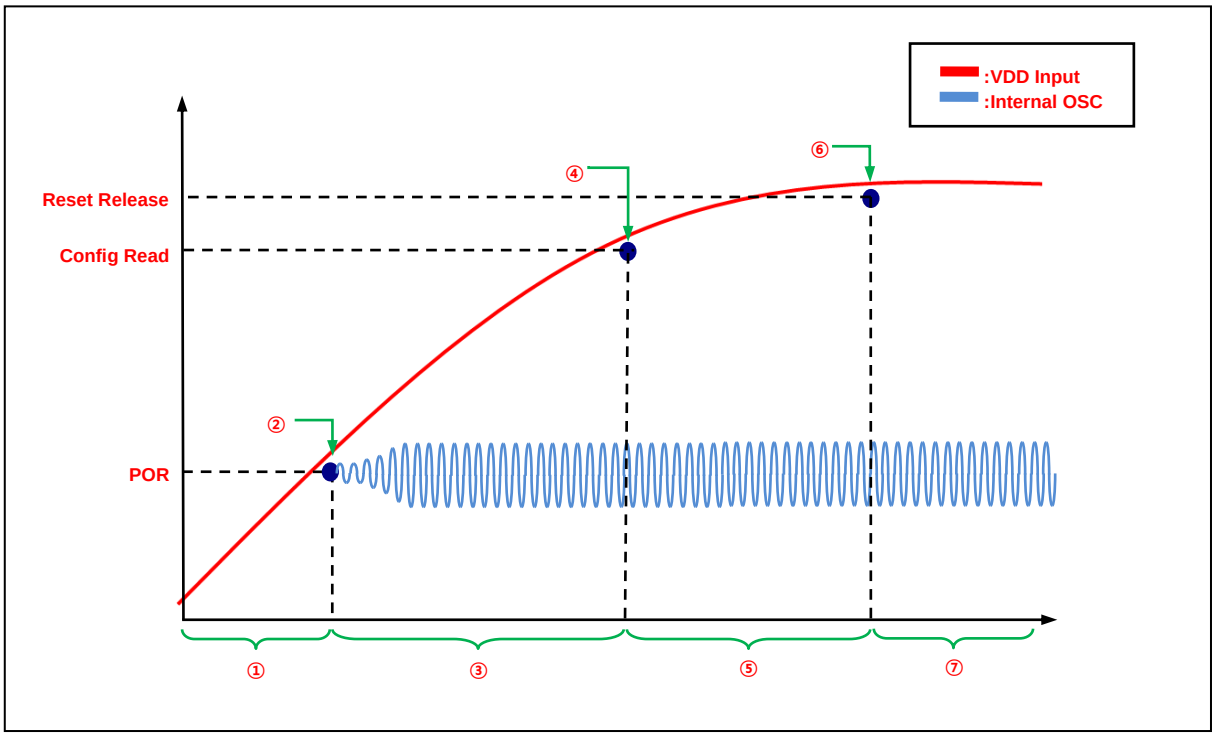


Figure 13.6 Boot Process Wave Form

Table 13-2 Boot Process Description

Process	Description	Remarks
①	-No Operation	
②	-1st POR level Detection	-about 2.0V
③	- (INT-OSC 8MHz/8)x256x28h Delay section (=10ms) -VDD input voltage must rise over than operating voltage for Config read	-Slew Rate >= 0.15V/ms
④	- Config read point	-over 2.2V -Config Value is determined by Writing Option
⑤	- Rising section to Reset Release Level	-16ms point after POR
⑥	- Reset Release section (BIT overflow) i) after16ms, after External Reset Release (External reset) ii) 16ms point after POR (POR only)	- BIT is used for Peripheral stability
⑦	-Normal operation	

13.6 Brown Out Detector Processor

The MC96P0202 has an On-chip brown-out detection circuit (BOD) for monitoring the VDD level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by LVRVS[1:0] bit to be 2.20V, 2.30V, 2.50V. The LVR block is always on.

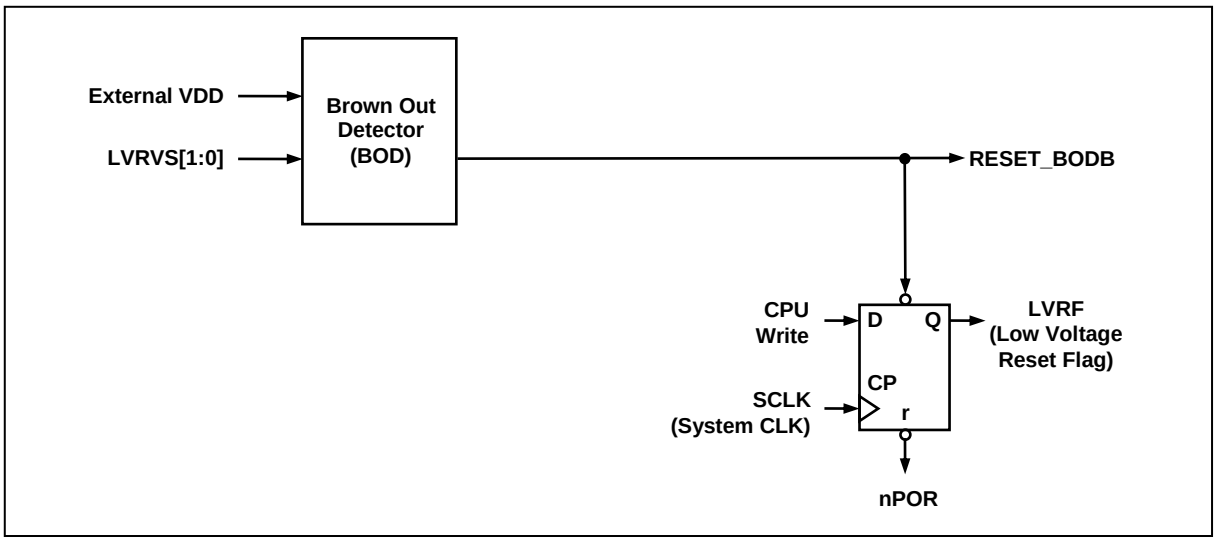


Figure 13.7 Block Diagram of BOD

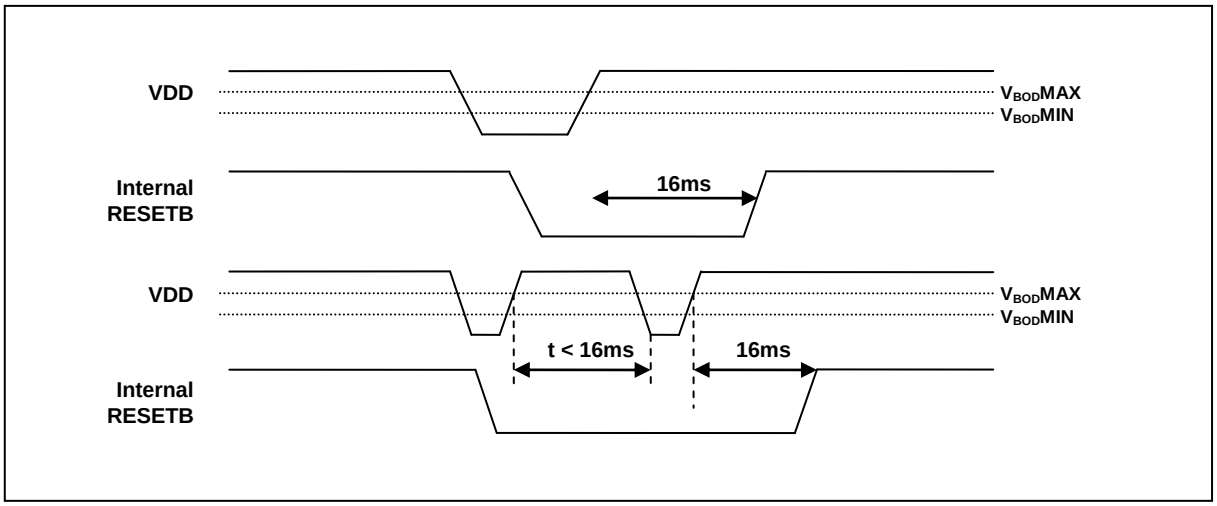


Figure 13.8 Internal Reset at the power fail situation

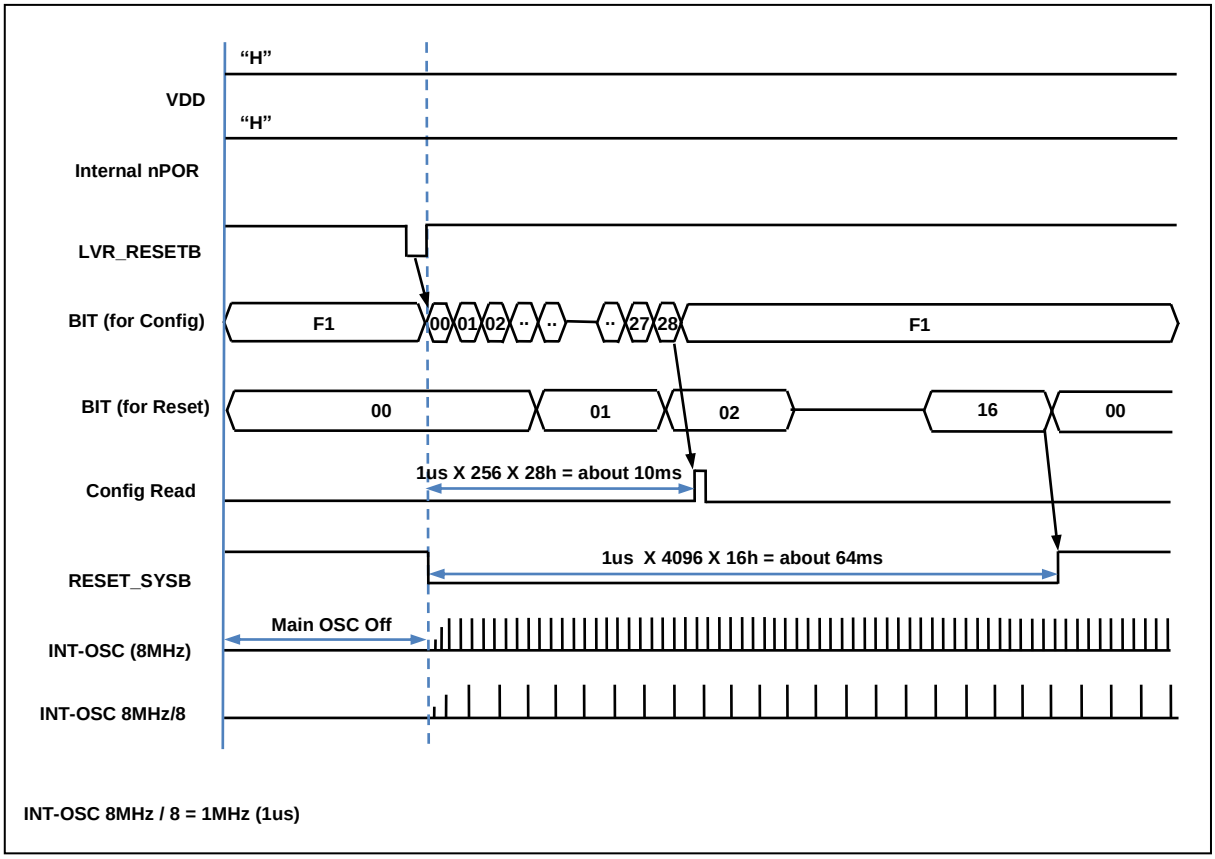


Figure 13.9 Configuration timing when BOD RESET

13.6.1 Register Map

Table 13-3 Reset Operation Register Map

Name	Address	Dir	Default	Description
RSTFR	E8H	R/W	80H	Reset Flag Register
LVRCR	D8H	R/W	00H	Low Voltage Reset Control Register

13.6.2 Reset Operation Register Description

The reset control register consists of the reset flag register (RSTFR) and low voltage reset control register (LVRCR).

13.6.3 Register Description for Reset Operation

RSTFR (Reset Flag Register) : E8H

7	6	5	4	3	2	1	0
LVRF	-	WDTRF	OCDRF	-	-	-	-
R/W	-	R/W	R/W	-	-	-	-

Initial value : 80H

LVRF Low Voltage Reset flag bit. This bit is reset by writing '0' to this bit and set by POR.

0 No detection

1 Detection

WDTRF Watch Dog Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

OCDRF On-Chip Debug Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.

0 No detection

1 Detection

Notes) 1. When the Power-On Reset occurs, the LVRF bit is set to "1", the other flag (WDTRF and OCSRF) bits are all cleared to "0".

2. When a reset except the POR occurs, the corresponding flag bit is only set to "1", the other flag bits are kept in the previous.

LVRCR (Low Voltage Reset Control Register) : D8H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	LVRVS1	LVRVS0
-	-	-	-	-	-	R/W	R/W

Initial value : 00H

LVRVS[1:0] LVR Level Select

LVRVS1	LVRVS0	Description
0	0	Not used
0	1	2.2V
1	0	2.3V
1	1	2.5V

Note) The LVR block is always on.

14. On-chip Debug System (EVA Chip Only)

14.1 Overview

14.1.1 Description

The program memory of MC96P0202 is OTP type, and MC96P0202 isn't equipped with on-chip debugger (OCD). It is not recommended to develop and debug program with MC96P0202.

MC96P0202D-EVA is the evaluation chip(EVA chip) for MC96P0202. OCD is embedded in MC96P0202D-EVA and the program memory of MC96P0202D-EVA is designed with SRAM. So, it is possible to develop and debug program for MC96P0202 with MC96P0202D-EVA. Because SRAM is the program memory of MC96P0202D-EVA, it is required to control power carefully. If the power is off, the contents of the program memory are vanished.

The on-chip debugger system of MC96P0202 doesn't support ROM writing function. So, it is necessary to equip additional ROM writer("PGM Plus") to write program to MC96P0202. It is possible to get "PGM Plus" through our web-site(www.abov.co.kr).

Detail descriptions for programming via the OCD interface can be found in the following chapter. Figure 14.3 shows a block diagram of the OCD interface and the On-chip Debug system.

14.1.2 EVA Chip Pin Assignment

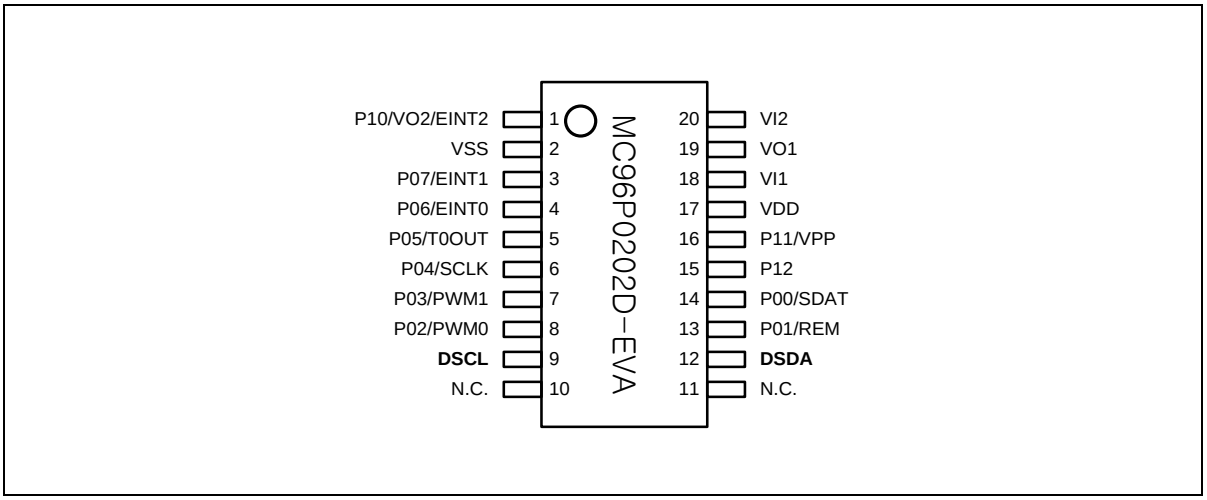


Figure 14.1 MC96P0202D-EVA 20SOP Pin Assignment

14.1.3 EVA Chip Package Diagram

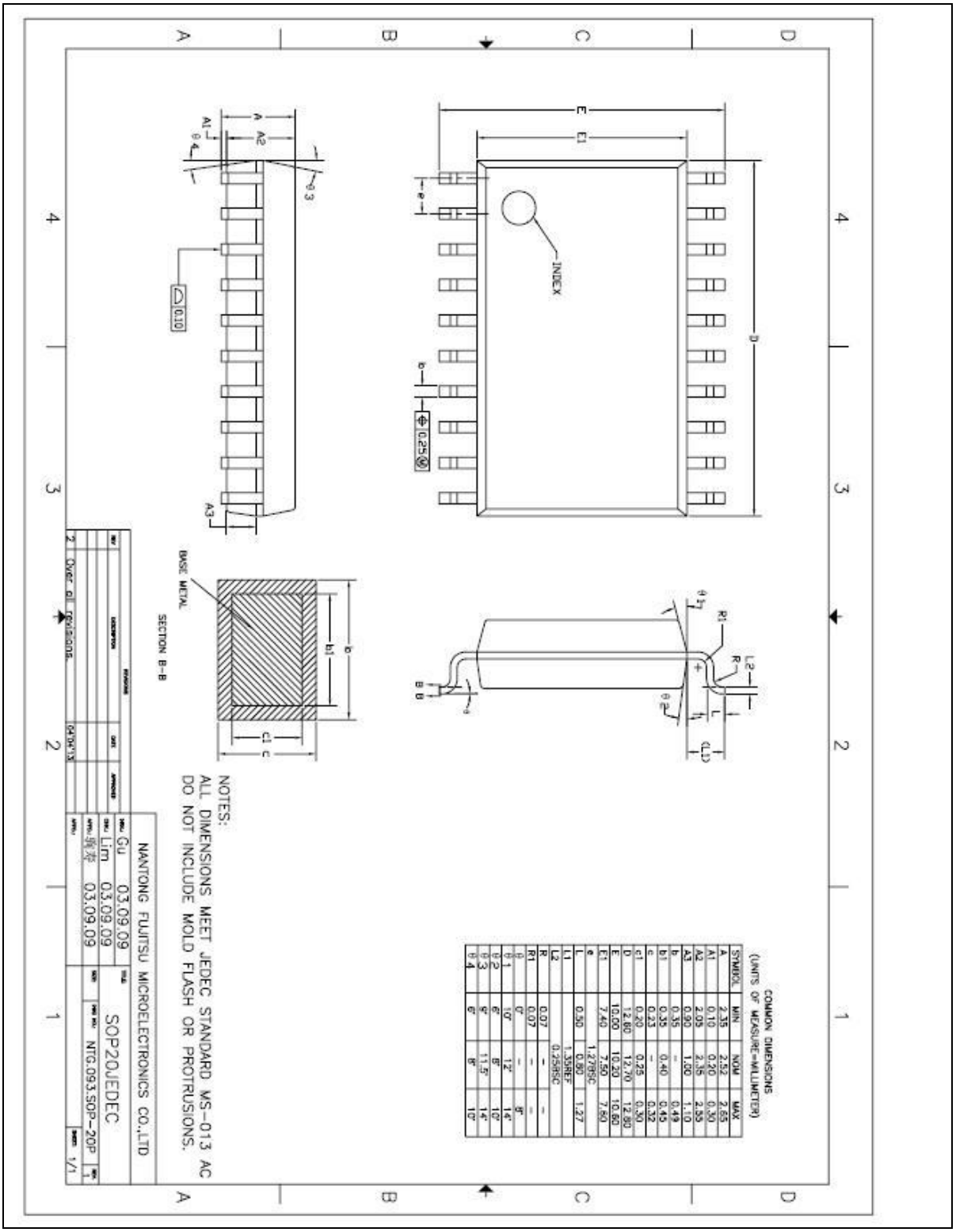


Figure 14.2 MC96P0202D-EVA 20SOP Package

14.1.4 Feature

- Two-wire external interface: 1-wire serial clock input, 1-wire bi-directional serial data bus
- Debugger Access to:
  - All Internal Peripheral Units
  - Internal data RAM
  - Program Counter
  - Program Memory (SRAM in cace of EVA chip)
- Extensive On-chip Debug Support for Break Conditions, Including
  - Break Instruction
  - Single Step Break
  - Program Memory Break Points on Single Address
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the two-wire Interface (not support for OTP chip)
  - On-chip Debugging Supported by Dr.Choice®
- Operating frequency

  Supports the maximum frequency of the target MCU

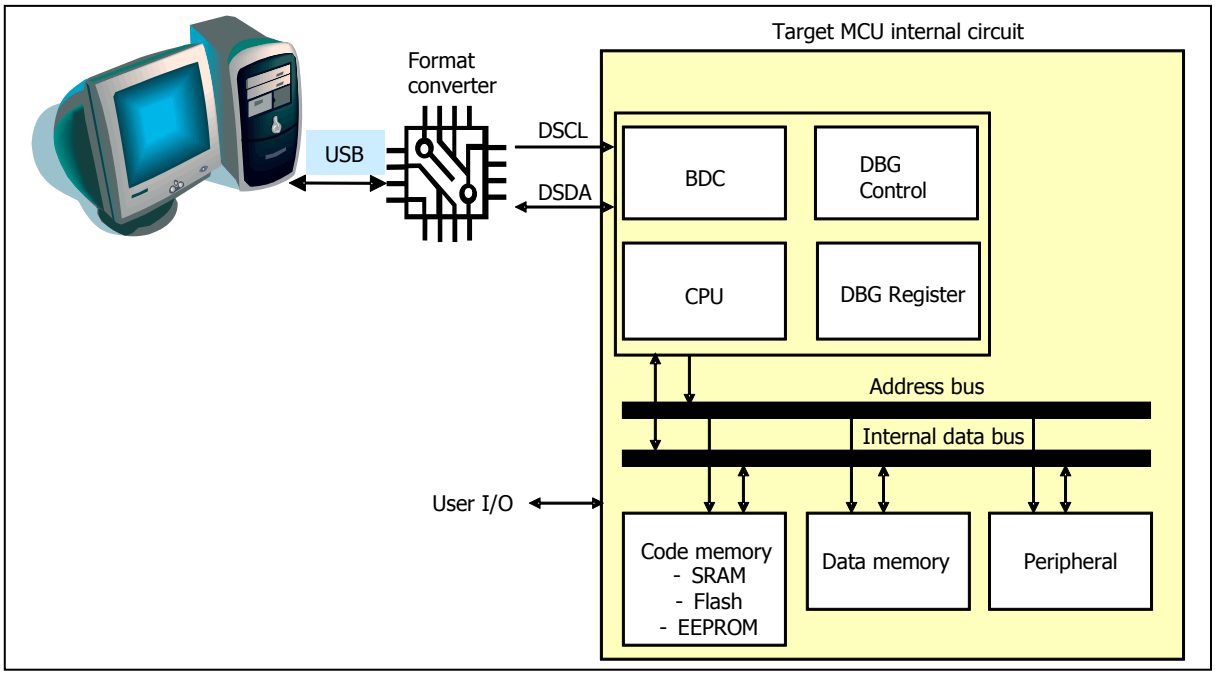


Figure 14.3 Block Diagram of On-Chip Debug System

14.2 EVA Chip OCD Interface

14.2.1 EVA Chip OCD Connection of Transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

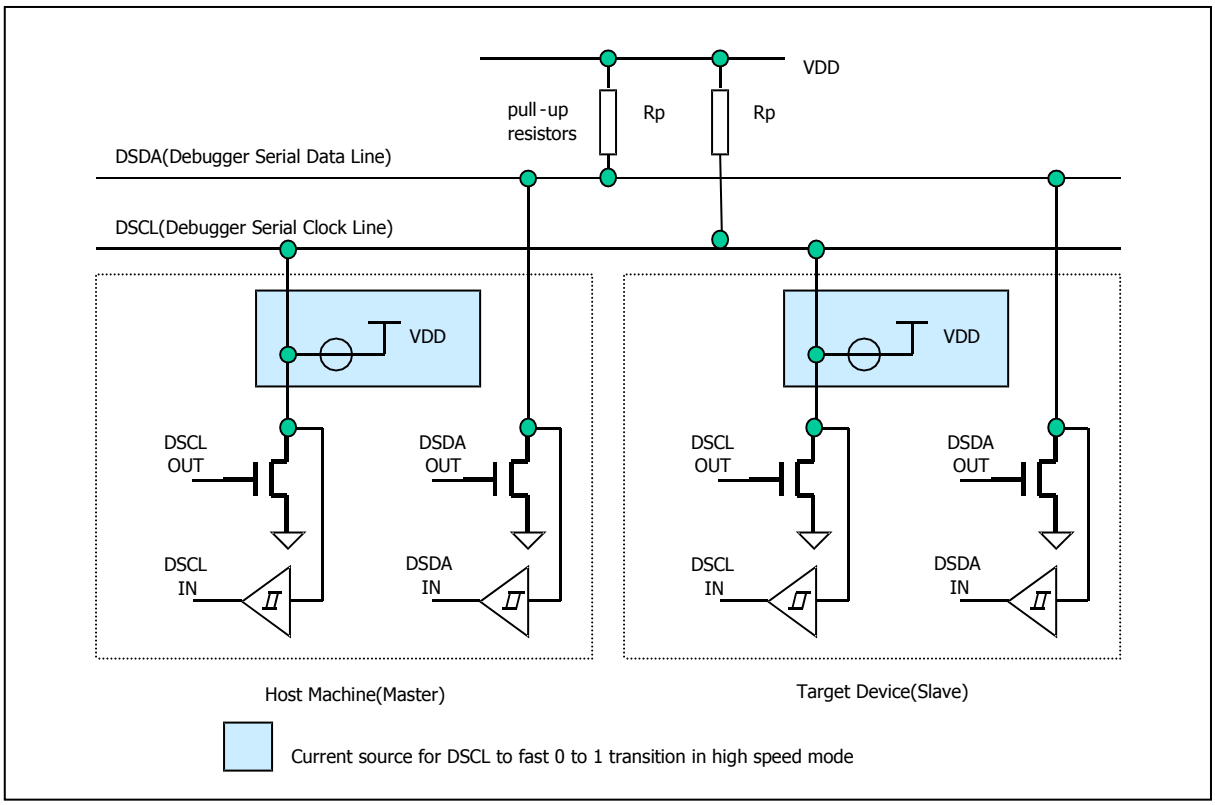


Figure 14.4 Connection of Transmission

15. Configure Option

The data for configure option should be written in the configure option area (001FH) by programmer (Writer tools).

15.1 Configure Option Control Register

CONFIGURE OPTION 1 : ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	-	-	-	-	-	-	-

Initial value : 00H

R_P	Read Protection	
	0	Disable “Read protection”
	1	Enable “Read protection”

16. APPENDIX

A. Instruction Table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below.
Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65

XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2

ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠ 0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	3	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.