

QUAD 2-INPUT "NAND" POWER GATE

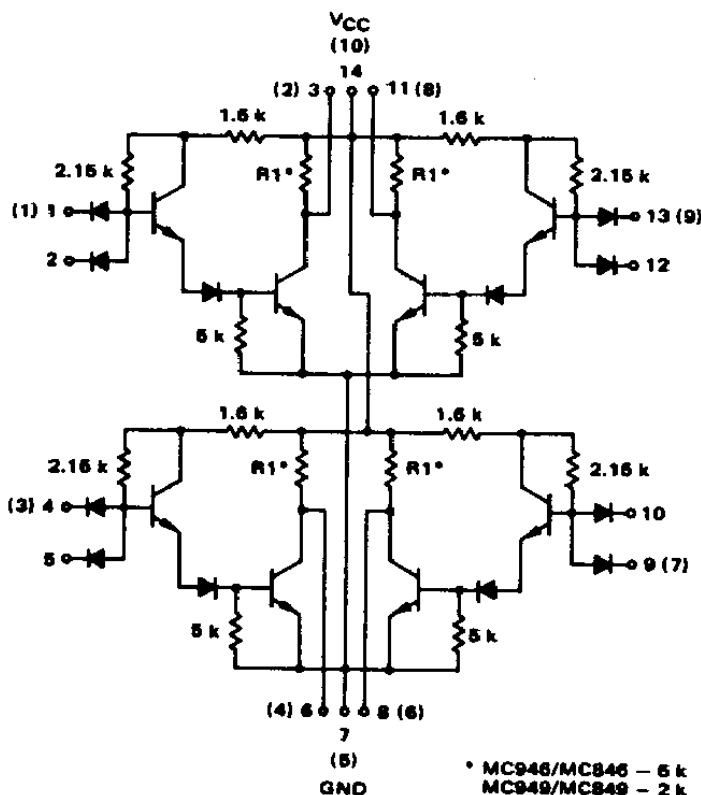
MDTL MC930/830 series

MC946F · MC846F, P
MC949F · MC849F, P

QUAD INVERTER

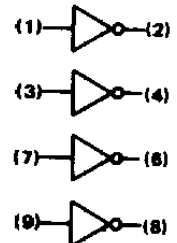
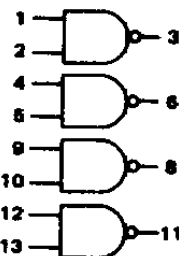
MC946G · MC846G
MC949G · MC849G

This gate element, in the 14-pin flat and dual in-line packages, consists of four 2-input NAND gate circuits. This circuit can be used as a dual 2-input non-inverting gate, or as two bistable circuits when two dual 2-input gates are cross-coupled. Since the metal can (G suffix) has only 10 pins, that circuit consists of four inverters.



MC946F/MC846F, P
 MC949F/MC849F, P

MC946G/MC846G
 MC949G/MC849G



Positive Logic: $3 = \overline{1 \cdot 2}$

Negative Logic: $3 = \overline{1 + 2}$

Positive Logic: $2 = \overline{1}$

Negative Logic: $2 = \overline{1}$

Input Loading Factor = 1

Output Loading Factor:

MC946/MC846 = 8

MC949/MC849 = 7

Total Power Dissipation:

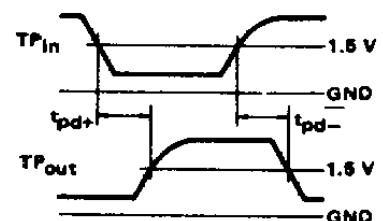
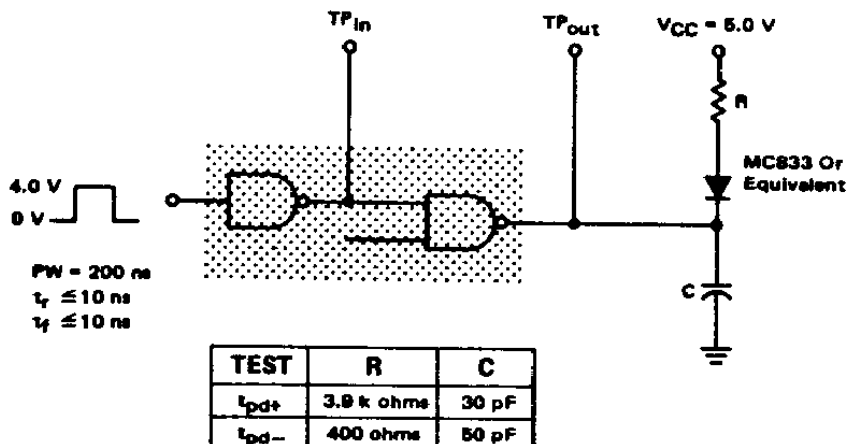
	MC946 MC846	MC949 MC849
Inputs Low	24 mW	24 mW
Inputs High	52 mW	54 mW
50% Duty Cycle	38 mW	54 mW

Propagation Delay Time:

MC946/MC846 = 30 ns typ

MC949/MC849 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

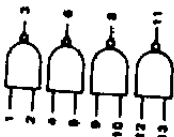


MC946F/MC846F, P, MC949F/MC849F, P (continued)
MC946G/MC846G, MC949G/MC849G (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.



PACKAGE	PIN NUMBER													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	2	3	4	5	6	7	8	9	10	11	12	13	14

Characteristic	Symbol	Pin Under Test	MC946, MC949 TEST LIMITS													
			-55°C							+25°C						
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
			Unit	Unit	Unit	Unit	Unit	Unit	Unit	Unit	Unit	Unit	Unit	Unit	Unit	Unit
Output Voltage	V _{OL} V _{OH}	3 3 3	0.40 2.50 2.50	- - -	0.40 2.90 2.90	- - -	0.45 2.60 2.60	- - -	0.45 2.60 2.60	- - -	0.45 2.60 2.60	- - -	0.45 2.60 2.60	- - -	0.50 2.50 2.50	Vdc ↑ ↑
Short-Circuit Current	I _{SC}	3	-1.34 -4.00	- -	-1.34 -4.00	- -	-1.30 -3.90	- -	-1.30 -3.90	- -	-1.30 -3.90	- -	-1.30 -3.90	- -	-1.25 -3.75	mAdc mAdc
Reverse Current	I _R	1 2	2.0 2.0	- -	2.0 2.0	- -	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	5.0 5.0	- -	10 10	μAdc μAdc
Output Leakage Current	I _{CEX}	3	-	-	50	-	-	-	-	-	-	-	-	-	-	μAdc
Forward Current	I _F	1 2	-1.60 -1.60	- -	-1.60 -1.60	- -	-1.40 -1.40	- -	-1.40 -1.40	- -	-1.40 -1.40	- -	-1.40 -1.40	- -	-1.33 -1.33	mAdc mAdc
Power Drain Current (Total Device)	I _{PDH} I _{PDH} I _{max}	14 14 14	- - -	- - -	13 21.4 11	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	- - -	mAdc mAdc mAdc
Switching Times	t _{pd} t _{pd} t _{pd} t _{pd}	1,3 1,3 1,3 1,3	- - - -	- - - -	25 10 15 10	80 30 60 30	- - - -	- - - -	- - - -	- - - -	- - - -	- - - -	- - - -	- - - -	- - - -	ns ns ns ns

Pins not listed are left open.

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D