MC74LVXC3245

Configurable Dual Supply Octal Transceiver

with 3−State Outputs for 3 V Systems

The 74LVXC3245 is a 24−pin dual−supply, octal configurable voltage interface transceiver especially well suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 3.0 V supply level; the A port is a dedicated 3.0 V port. The V_{CCB} pin accepts a 3.0 V−to−5.0 V supply level. The B port is configured to track the V_{CCB} supply level. A 5.0 V level on the V_{CCB} pin will configure the I/O pins at a 5.0 V level and a 3.0 V V_{CCB} will configure the I/O pins at a 3.0 V level. The A port interfaces with a 3.0 V host system and the B port to the card slots. This device will allow the V_{CCB} voltage source pin and I/O pins on the B port to float when $\overline{OE}$ is High. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow. Transmit (active−High) enables data from the A port to B port. Receive (active−Low) enables data from the B port to the A port.

Features

- Bidirectional Interface Between 3.0 V and 3.0 V/5.0 V Buses
- Control Inputs Compatible with TTL Level
- Outputs Source/Sink Up to 24 mA
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Available in SOIC and TSSOP Packages
- Flexible V_{CCB} Operating Range
- Allows B Port and V_{CCB} to Float Simultaneously When $\overline{OE}$ is High
- Functionally Compatible With the 74 Series 245
- These Devices are Pb−Free and are RoHS Compliant

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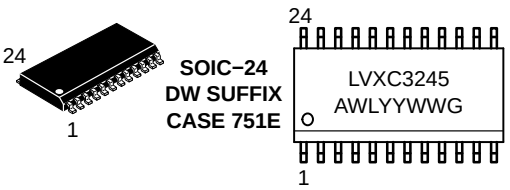
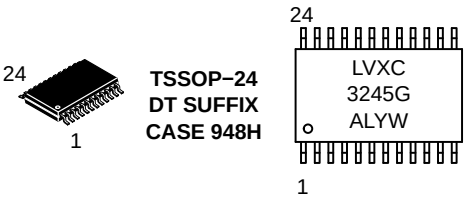
MARKING DIAGRAMS





LVXC3245	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

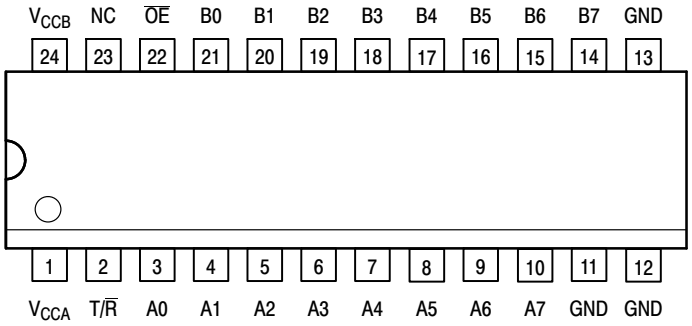


Figure 1. 24−Lead Pinout (Top View)

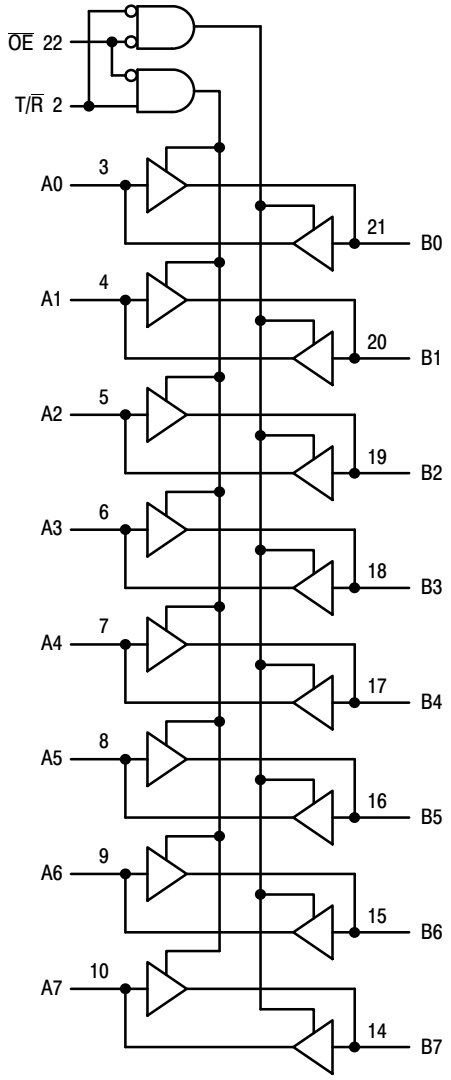


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A0−A7	Side A 3−State Inputs or 3−State Outputs
B0−B7	Side B 3−State Inputs or 3−State Outputs

INPUTS		OPERATING MODE Non−Inverting
$\overline{OE}$	T/$\overline{R}$	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; for I_{CC} reasons, Do Not Float Inputs

MAXIMUM RATINGS

Symbol	Parameter		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		−0.5 to +7.0		V
V_I	DC Input Voltage	$\overline{OE}$, T/$\overline{R}$	−0.5 to V_{CCA} +0.5		V
$V_{I/O}$	DC Input/Output Voltage	An	−0.5 to V_{CCA} +0.5		V
		Bn	−0.5 to V_{CCB} +0.5		V
I_{IK}	DC Input Diode Current	$\overline{OE}$, T/$\overline{R}$	±20	V_I < GND	mA
I_{OK}	DC Output Diode Current		±50	V_O < GND; V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}, I_{GND}	DC Supply Current	Per Output Pin Maximum Current	±50 ±200		mA
T_{STG}	Storage Temperature Range		−65 to +150		°C
	DC Latchup Source/Sink Current		±300		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Supply Voltage ($V_{CCA} \le V_{CCB}$)	V_{CCA} V_{CCB}	2.3 3.0	3.6 5.5	V
V_I	Input Voltage	$\overline{OE}$, T/$\overline{R}$	0	V_{CCA}	V
$V_{I/O}$	Input/Output Voltage	An Bn	0 0	V_{CCA} V_{CCB}	V
T_A	Operating Free−Air Temperature		−40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate V_{IN} from 30% to 70% of V_{CC}; V_{CC} at 3.0 V, 4.5 V, 5.5 V		0	8	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	T_A = 25°C	T_A = −40 to +85°C		Unit
						Typ	Guaranteed Limits		
V_{IHA}	Minimum HIGH Level Input Voltage	An $\overline{OE}$ T/$\overline{R}$	V_{OUT} ≤ 0.1 V or ≥ V_{CC} − 0.1 V	2.3 3.0 3.6	3.0 3.6 5.5		2.0 2.0 2.0	2.0 2.0 2.0	V
V_{IHB}		Bn		2.3 3.0 3.6	3.0 3.6 5.5		2.00 2.00 3.85	2.00 2.00 3.85	V
V_{ILA}	Maximum LOW Level Input Voltage	An $\overline{OE}$ T/$\overline{R}$	V_{OUT} ≤ 0.1 V or ≥ V_{CC} − 0.1 V	2.3 3.0 3.6	3.0 3.6 5.5		0.8 0.8 0.8	0.8 0.8 0.8	V
V_{ILB}		Bn		2.3 3.0 3.6	3.0 3.6 5.5		0.80 0.80 1.65	0.80 0.80 1.65	V
V_{OHA}	Minimum HIGH Level Output Voltage		I_{OUT} = −100 μA I_{OH} = −12 mA I_{OH} = −24 mA I_{OH} = −12 mA I_{OH} = −24 mA	3.0 3.0 3.0 2.3 2.3	3.0 3.0 3.0 3.0 4.5	2.99 2.85 2.65 2.50 2.30	2.90 2.56 2.35 2.30 2.10	2.90 2.46 2.25 2.20 2.00	V
V_{OHB}			I_{OUT} = −100 μA I_{OH} = −12 mA I_{OH} = −24 mA I_{OH} = −24 mA	3.0 3.0 3.0 3.0	3.0 3.0 3.0 4.5	2.99 2.85 2.65 4.25	2.90 2.56 2.35 3.86	2.90 2.46 2.25 3.76	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition	V_{CCA}	V_{CCB}	T_A = 25°C	T_A = −40 to +85°C		Unit
						Typ	Guaranteed Limits		
V_{OLA}	Maximum LOW Level Output Voltage		I_{OUT} = 100 μA I_{OL} = 24 mA I_{OL} = 12 mA I_{OL} = 24 mA	3.0 3.0 2.7 2.7	3.0 3.0 3.0 4.5	0.002 0.21 0.11 0.22	0.10 0.36 0.36 0.42	0.10 0.44 0.44 0.50	V
V_{OLB}			I_{OUT} = 100 μA I_{OL} = 24 mA I_{OL} = 24 mA	3.0 3.0 3.0	3.0 3.0 4.5	0.002 0.21 0.18	0.10 0.36 0.36	0.10 0.44 0.44	V
I_{IN}	Max Input Leakage Current	$\overline{OE}$, T/$\overline{R}$	V_I = V_{CCA}, GND	3.6 3.6	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0	μA
I_{OZA}	Max 3−State Output Leakage	An	V_I = V_{IH}, V_{IL} $\overline{OE}$ = V_{CCA} V_O = V_{CCA}, GND	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA
I_{OZB}	Max 3−State Output Leakage	Bn	V_I = V_{IH}, V_{IL} $\overline{OE}$ = V_{CCA} V_O = V_{CCB}, GND	3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA
ΔI_{CC}	Maximum I_{CC}/Input	Bn	V_I = V_{CCB}−2.1 V	3.6	5.5	1.0	1.35	1.5	mA
		All Inputs	V_I = V_{CC}−0.6 V	3.6	3.6		0.35	0.5	mA
I_{CCA1}	Quiescent V_{CCA} Supply Current as B Port Floats		An = V_{CCA} or GND Bn = Open, $\overline{OE}$ = V_{CCA}, T/$\overline{R}$ = V_{CCA}, V_{CCB} = Open	3.6	Open		5	50	μA
I_{CCA2}	Quiescent V_{CCA} Supply Current		An = V_{CCA} or GND Bn = V_{CCB} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = GND	3.6 3.6	3.6 5.5		5 5	50 50	μA
I_{CCB}	Quiescent V_{CCB} Supply Current		An = V_{CCA} or GND Bn = V_{CCB} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = V_{CCA}	3.6 3.6	3.6 5.5		5 8	50 80	μA
V_{OLPA}	Quiet Output Max Dynamic V_{OL}		Notes 1, 2	3.3 3.3	3.3 5.0		0.8 0.8		V
V_{OLPB}			Notes 1, 2	3.3 3.3	3.3 5.0		0.8 1.5		V
V_{OLVA}	Quiet Output Min Dynamic V_{OL}		Notes 1, 2	3.3 3.3	3.3 5.0		−0.8 −0.8		V
V_{OLVB}			Notes 1, 2	3.3 3.3	3.3 5.0		−0.8 −1.2		V
V_{IHDA}	Min HIGH Level Dynamic Input Voltage		Notes 1, 3	3.3 3.3	3.3 5.0		2.0 2.0		V
V_{IHDB}			Notes 1, 3	3.3 3.3	3.3 5.0		2.0 3.5		V
V_{ILDA}	Max LOW Level Dynamic Input Voltage		Notes 1, 3	3.3 3.3	3.3 5.0		0.8 0.8		V
V_{ILDB}			Notes 1, 3	3.3 3.3	3.3 5.0		0.8 1.5		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Worst case package.
2. Max number of outputs defined as (n). Data inputs are driven 0 V to V_{CC} level; one output at GND.
3. Max number of data inputs (n) switching. (n−1) inputs switching 0 V to V_{CC} level. Input under test switching: V_{CC} level to threshold (V_{IHD}), 0 V to threshold (V_{ILD}), f = 1 MHz.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = −40 to +85°C; C_L = 50 pF						Unit
		V_{CCA} = 2.7−3.6 V V_{CCB} = 4.5−5.5 V			V_{CCA} = 2.7−3.6 V V_{CCB} = 3.0−3.6 V			
		Min	Typ (Note 4)	Max	Min	Typ (Note 5)	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B	1.0 1.0	4.8 3.9	8.5 7.0	1.0 1.0	5.5 5.2	9.0 8.5	ns
t_{PHL} t_{PLH}	Propagation Delay B to A	1.0 1.0	3.8 4.3	7.0 8.0	1.0 1.0	4.4 5.1	7.5 8.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to B	1.0 1.0	4.7 4.8	8.5 9.0	1.0 1.0	6.0 6.1	9.5 10.0	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to A	1.0 1.0	5.9 5.4	10.0 9.5	1.0 1.0	6.4 5.8	10.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to B	1.0 1.0	4.0 3.8	8.5 8.0	1.0 1.0	6.3 4.5	10.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A	1.0 1.0	4.6 3.1	10.0 7.0	1.0 1.0	5.2 3.4	10.0 7.0	ns
t_{OSHL} t_{OSLH}	Output to Output Skew, Data to Output (Note 6)		1.0	1.5		1.0	1.5	ns

4. Typical values at V_{CCA} = 3.3 V, V_{CCB} = 5.0 V at 25°C.
5. Typical values at V_{CCA} = 3.3 V, V_{CCB} = 3.3 V at 25°C.
6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter		Condition	Typical	Unit
C_{IN}	Input Capacitance		V_{CCA} = 3.3 V; V_{CCB} = 5.0 V	4.5	pF
$C_{I/O}$	Input/Output Capacitance		V_{CCA} = 3.3 V; V_{CCB} = 5.0 V	10	pF
C_{PD}	Power Dissipation Capacitance (Measured at 10 MHz)	A→B B→A	V_{CCB} = 5.0 V V_{CCA} = 3.3 V	50 40	pF

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVXC3245DWRG	SOIC−24 (Pb−Free)	1000 Tape & Reel
MC74LVXC3245DTG	TSSOP−24* (Pb−Free)	62 Units / Rail
MC74LVXC3245DTR2G	TSSOP−24* (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

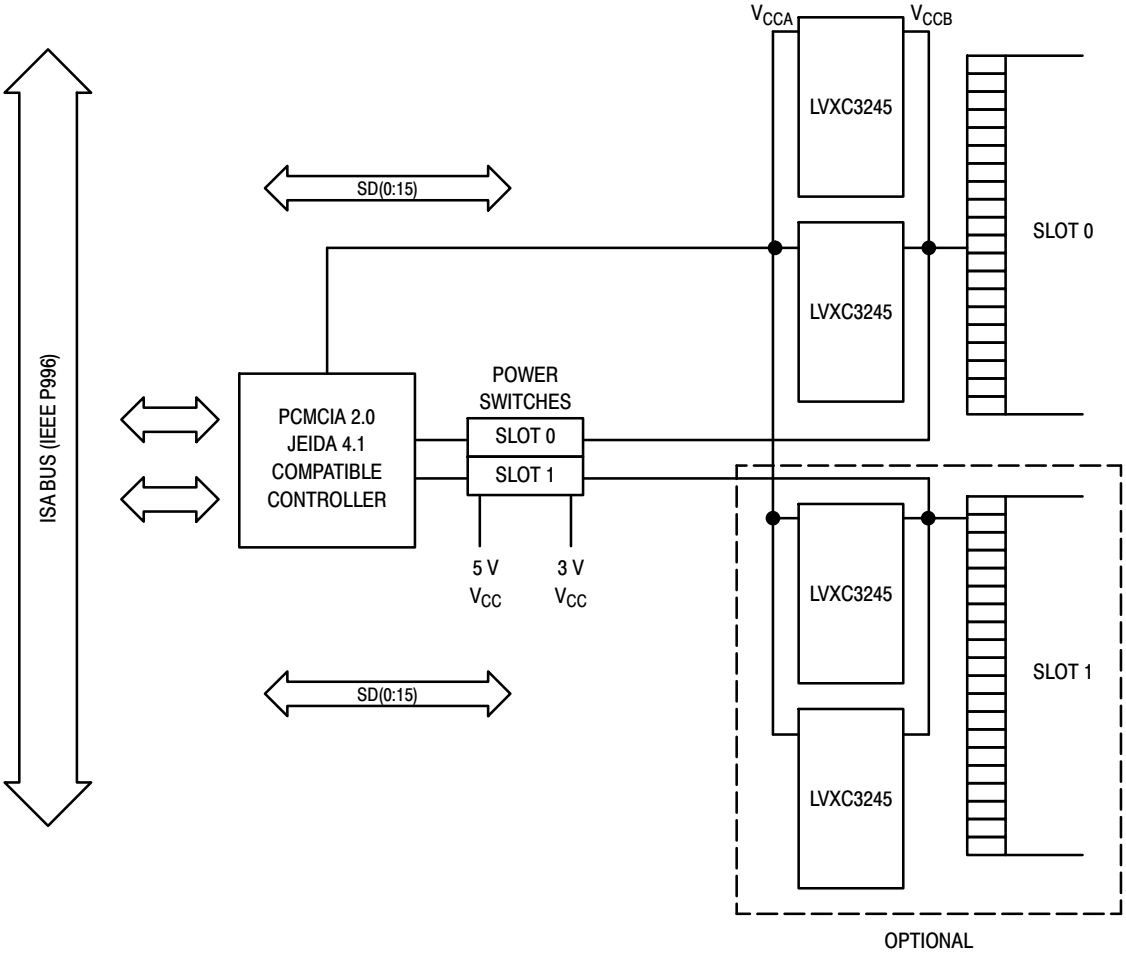
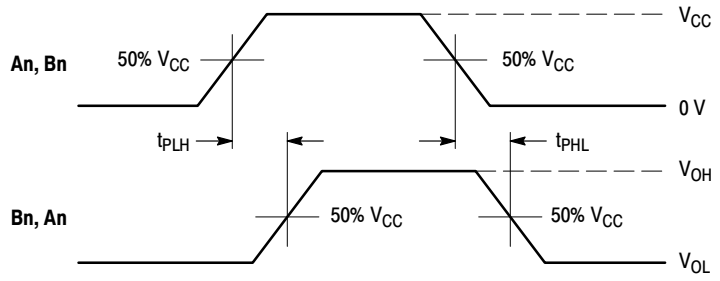


Figure 3. Block Diagram

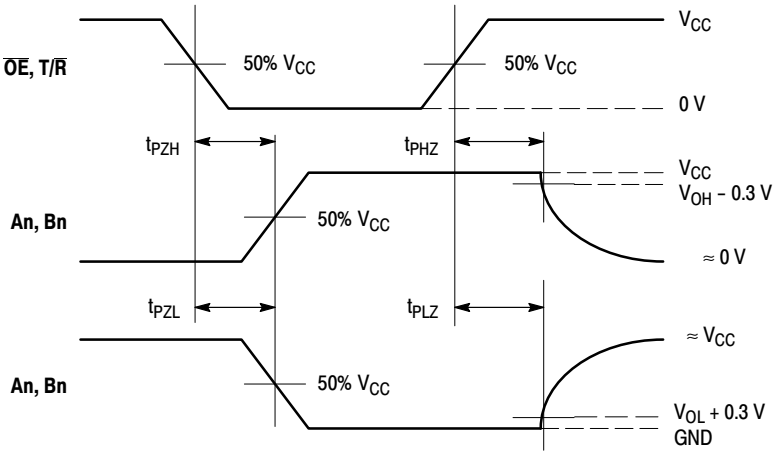
Configurable I/O Application for PCMCIA Cards

The 74LVXC3245 is a dual−supply device well suited for PCMCIA configurable I/O applications. The LVXC3245 consumes less than 1mW of quiescent power in all modes of operation, making it ideal for low power notebook designs. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5.0 V and 3.3 V operation. By tying the V_{CCB} pin to the card voltage supply, the PCMCIA card will always have rail−to−rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin must always be tied to a 3.3 V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).

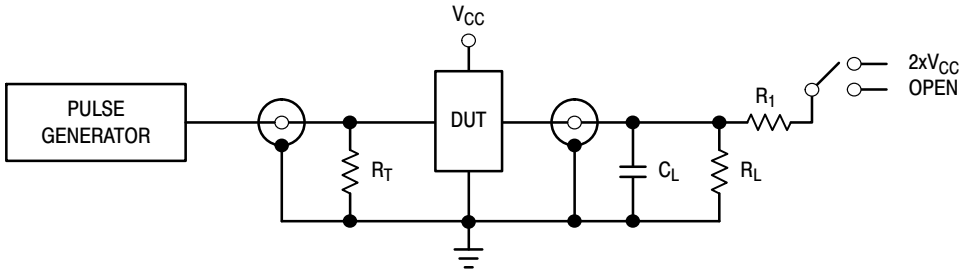


WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 4. AC Waveforms



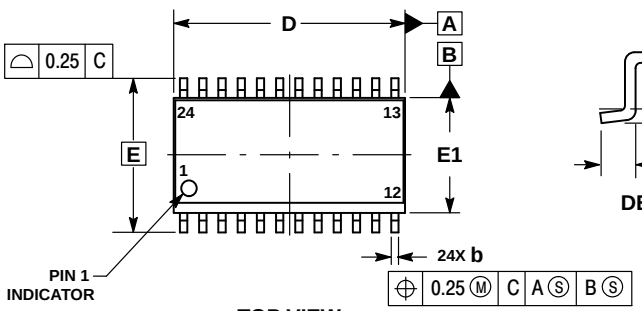
TEST	SWITCH
t_{PLH}, t_{PHL}, t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2xV_{CC}

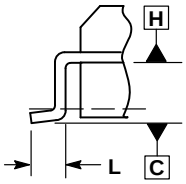
C_L = 50 pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500 Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

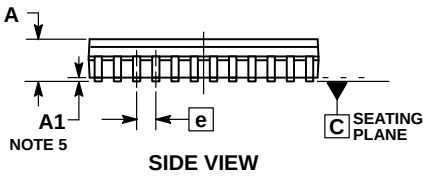
Figure 5. Test Circuit

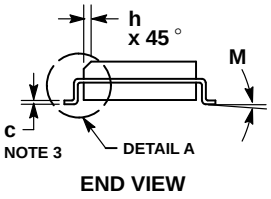
PACKAGE DIMENSIONS

SOIC−24
DW SUFFIX
CASE 751E−04
ISSUE F





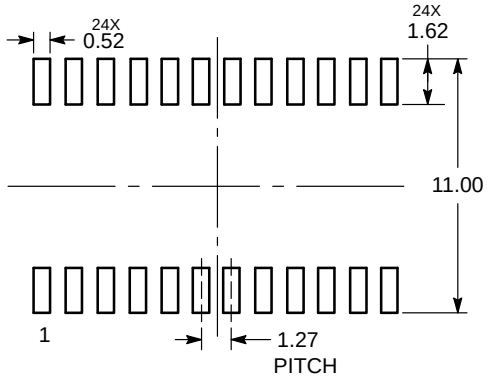




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
b	0.35	0.49
c	0.23	0.32
D	15.25	15.54
E	10.30 BSC	
E1	7.40	7.60
e	1.27 BSC	
h	0.25	0.75
L	0.41	0.90
M	0 °	8 °

RECOMMENDED
SOLDERING FOOTPRINT*

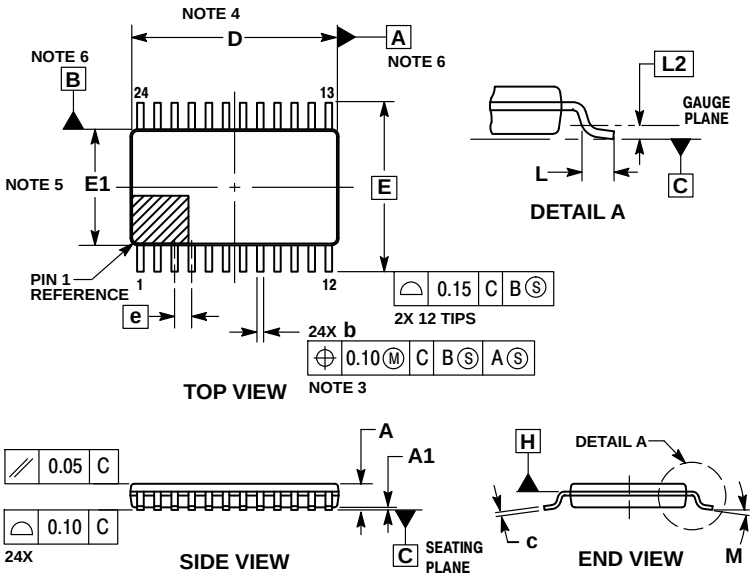


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

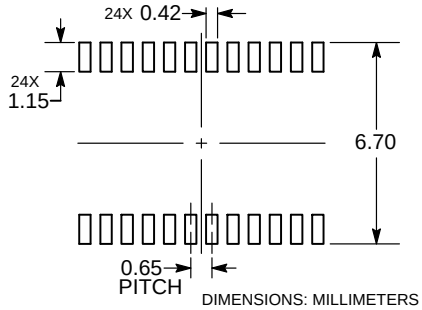
TSSOP−24, 7.8x4.4, 0.65P
DT SUFFIX
CASE 948H
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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