NEC

MOS INTEGRATED CIRCUIT
MC-458DA727

8 M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE
REGISTERED TYPE

Description

The MC-458DA727 is a 8,388,608 words by 72 bits synchronous dynamic RAM module on which 9 pieces of 64M SDRAM: μPD4564841 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 72 bits organization (ECC type)
- Clock frequency and access time from CLK

Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)
MC-458DA727-A75	CL = 3	133 MHz	5.4 ns

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All DQs have 10 Ω ±10 % of series resistor
- Single 3.3 V ±0.3 V power supply
- LVTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Registered type
- Serial PD

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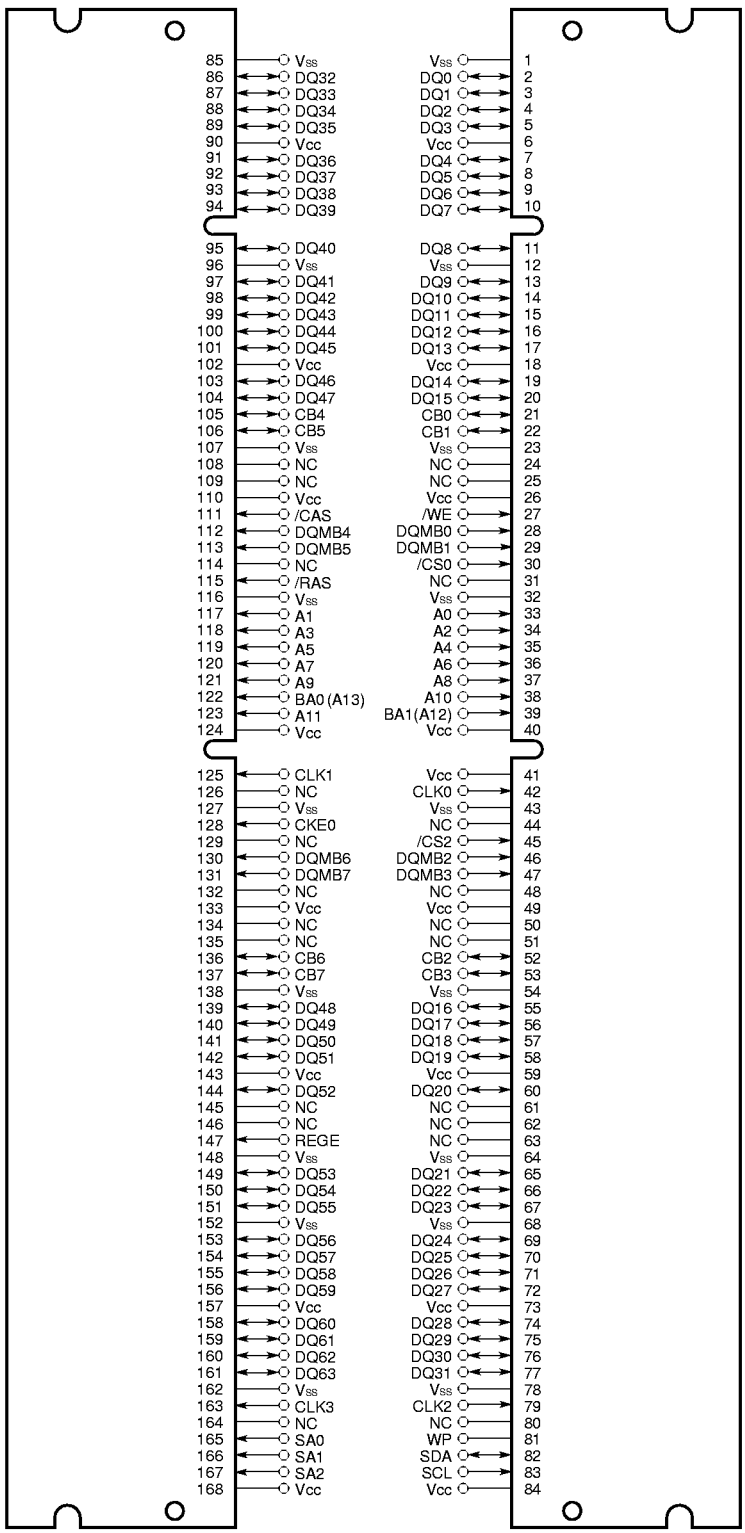
Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-458DA727LF-A75	133 MHz	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plated 38.1 mm (1.5 inch) height	9 pieces of μPD4564841G5 (Rev. L) (400 mil TSOP (II))

Pin Configuration

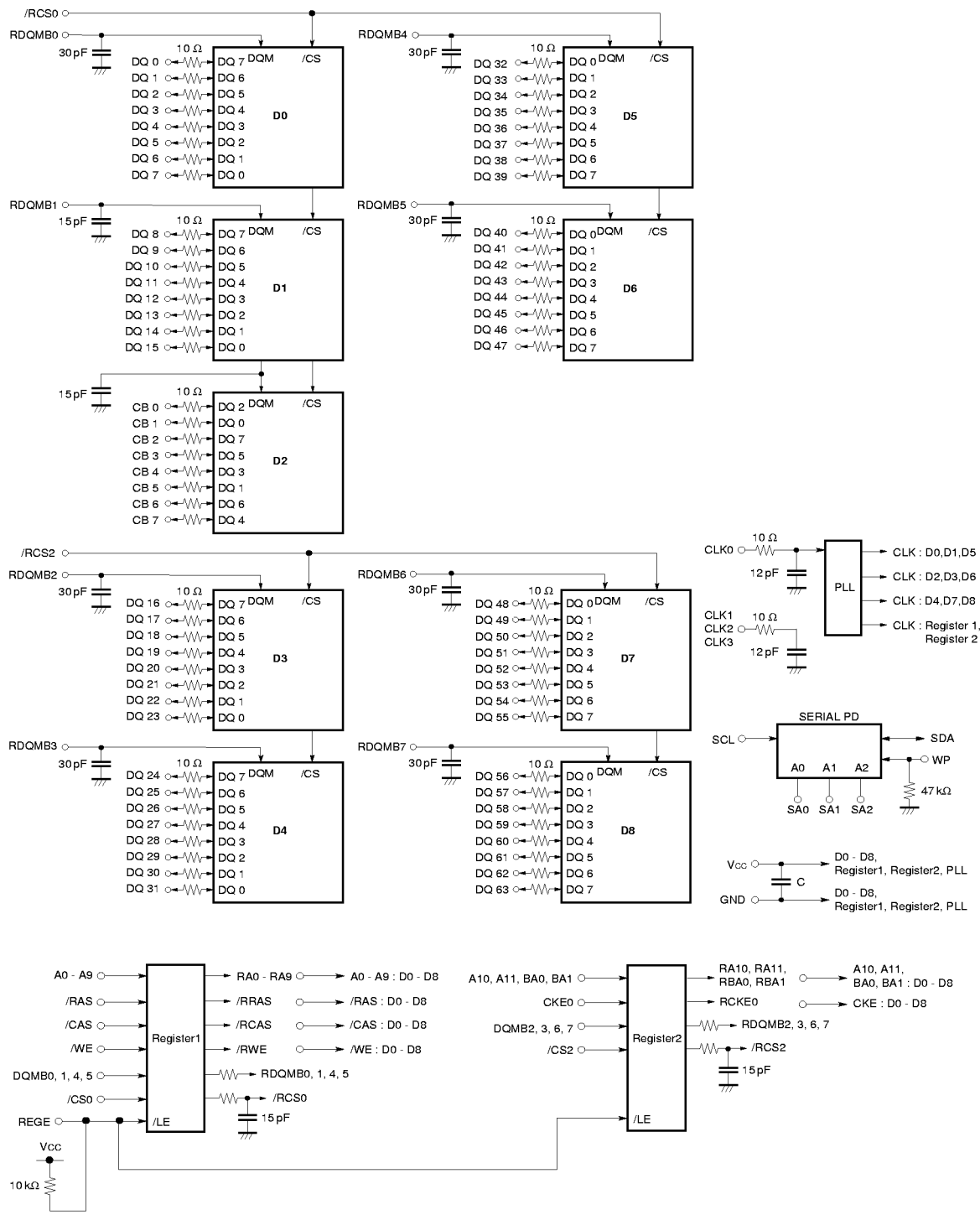
168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

A0 - A11	: Address Inputs
[Row: A0 - A11, Column: A0 - A8]	
BA0(A13), BA1(A12)	: SDRAM Bank Select
DQ0 - DQ63, CB0 - CB7	: Data Inputs/Outputs
CLK0 - CLK3	: Clock Input
CKE0	: Clock Enable Input
WP	: Write Protect
/CS0, /CS2	: Chip Select Input
/RAS	: Row Address Strobe
/CAS	: Column Address Strobe
/WE	: Write Enable
DQMB0 - DQMB7	: DQ Mask Enable
SA0 - SA2	: Address Input for EEPROM
SDA	: Serial Data I/O for PD
SCL	: Clock Input for PD
Vcc	: Power Supply
Vss	: Ground
REGE	: Register / Buffer Enable
NC	: No Connection

Block Diagram



Remarks 1. The series register values of DQs are 10 Ω.

2. D0 - D8: μPD4564841 (2M words × 8 bits × 4 banks)

3. REGE ≤ V_{IL}: Buffer mode
REGE ≥ V_{IH}: Register mode

4. Register: HD74ALVCF162834
PLL: HD74CDCF2509B

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 1 ms and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		12	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC}+0.3$	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, BA0(A13), BA1(A12), /RAS, /CAS, /WE	T.B.D.		T.B.D.	pF
	C_{I2}	CLK0 - CLK3	T.B.D.		T.B.D.	
	C_{I3}	CKE0	T.B.D.		T.B.D.	
	C_{I4}	/CS0, /CS2	T.B.D.		T.B.D.	
	C_{I5}	DQMB0 -DQMB7	T.B.D.		T.B.D.	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63, CB0 - CB7	T.B.D.		T.B.D.	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC(MIN.)}$, I_O = 0 mA		1,210	mA	1
Precharge standby current in power down mode	I_{CC2P}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns		259	mA	
	I_{CC2PS}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞		80		
Precharge standby current in non power down mode	I_{CC2N}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.		430	mA	
	I_{CC2NS}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞, Input signals are stable.		134		
Active standby current in power down mode	I_{CC3P}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns		295	mA	
	I_{CC3PS}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞		96		
Active standby current in non power down mode	I_{CC3N}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.		475	mA	
	I_{CC3NS}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞, Input signals are stable.		170		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA		1,615	mA	2
CBR (Auto) refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$		1,660	mA	3
Self refresh current	I_{CC6}	CKE ≤ 0.2 V		259	mA	
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V	−10	+10	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V	−1.5	+1.5	μA	
High level output voltage	V_{OH}	I_O = −4.0 mA	2.4		V	
Low level output voltage	V_{OL}	I_O = +4. 0 mA		0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

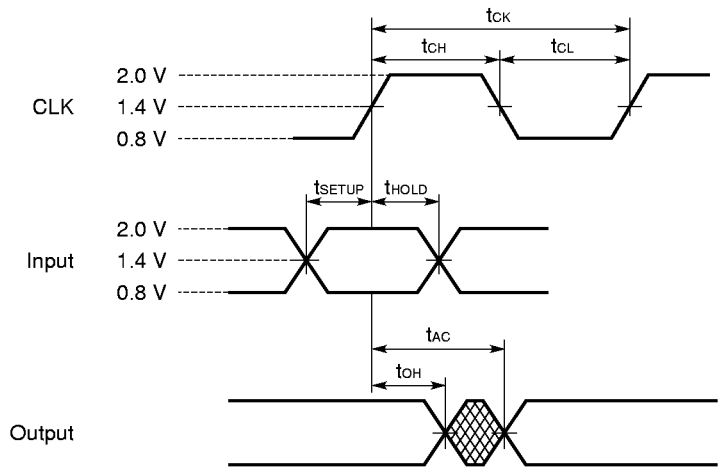
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

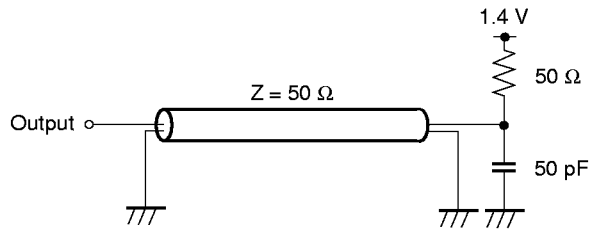
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics (Registered Mode)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
Clock cycle time	t_{CK}	7.5	(133 MHz)	ns	
Access time from CLK	t_{AC}		5.4	ns	1
Input clock frequency		50	133	MHz	
Input CLK duty cycle		45	55	%	
Data-out hold time	t_{OH}	2.7		ns	1
Data-out low-impedance time	t_{LZ}	0		ns	
Data-out high- impedance time	t_{HZ}	3	6	ns	
Data-in setup time	t_{DS}	1.5		ns	
Data-in hold time	t_{DH}	0.8		ns	
Address setup time	t_{AS}	1.5		ns	
Address hold time	t_{AH}	0.8		ns	
CKE setup time	t_{CKS}	1.5		ns	
CKE hold time	t_{CKH}	0.8		ns	
CKE setup time (Power down exit)	t_{CKSP}	1.5		ns	
Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time	t_{CMS}	1.5		ns	
Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time	t_{CMH}	0.8		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

Asynchronous Characteristics (Registered Mode)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
REF to REF/ACT command period	t_{RC}	9		CLK	
ACT to PRE command period	t_{RAS}	6	16,000	CLK	
PRE to ACT command period	t_{RP}	3		CLK	
Delay time ACT to READ/WRITE command	t_{RCD}	3		CLK	
ACT(0) to ACT(1) command period	t_{RRD}	2		CLK	
Data-in to PRE command period	t_{DPL}	1		CLK	
Data-in to ACT(REF) command period(Auto precharge)	t_{DAL}	20		ns	
Mode register set cycle time	t_{RSC}	2		CLK	
Transition time	t_T	0.5	30	ns	
Refresh time (4,096 refresh cycles)	t_{REF}		64	ms	

Serial PD (1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows		0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns		09H	0	0	0	0	1	0	0	1	9 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTL
9	CL = 3 Cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
10	CL = 3 Access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
11	DIMM configuration type		02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate/type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		08H	0	0	0	0	1	0	0	0	×8
14	Error checking SDRAM width		08H	0	0	0	0	1	0	0	0	×8
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM		04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported		04H	0	0	0	0	0	1	0	0	3
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes		1FH	0	0	0	1	1	1	1	1	Registered
22	SDRAM device attributes : General		0EH	0	0	0	0	1	1	1	0	
23-26			00H	0	0	0	0	0	0	0	0	
27	$t_{RP(MIN.)}$	-A75	17H	0	0	0	1	0	1	1	1	23 ns(22.5ns)
28	$t_{RRD(MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
29	$t_{RCD(MIN.)}$	-A75	17H	0	0	0	1	0	1	1	1	23 ns(22.5ns)
30	$t_{RAS(MIN.)}$	-A75	2DH	0	0	1	0	1	1	0	1	45 ns
31	Module bank density		10H	0	0	0	1	0	0	0	0	64M bytes

(2/2)

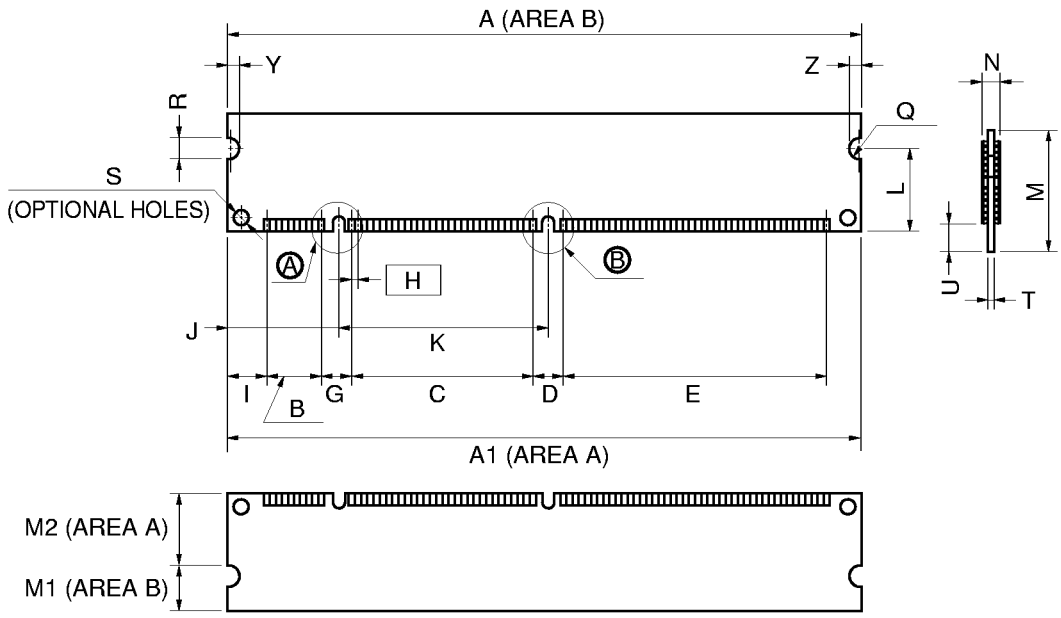
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32	Command and address signal input setup time		15H	0	0	0	1	0	1	0	1	1.5 ns
33	Command and address signal input hold time		08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time		15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time		08H	0	0	0	0	1	0	0	0	0.8 ns
36-61			00H	0	0	0	0	0	0	0	0	
62	SPD revision		02H	0	0	0	0	0	0	1	0	JEDEC 2
63	Checksum for bytes 0 - 62	-A75	C3H	1	1	0	0	0	0	1	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency		64H	0	1	1	0	0	1	0	0	100 MHz
127	Intel specification /CAS latency support	-A75	85H	1	0	0	0	0	1	0	1	

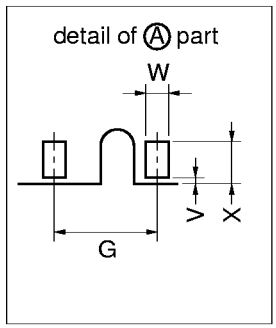
Timing Chart

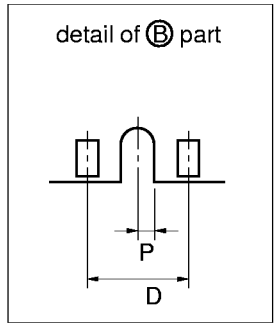
Refer to the **SYNCHRONOUS DRAM MODULE TIMING CHART Information (M13348X)**.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS
A	133.35
A1	133.35±0.13
B	11.43
C	36.83
D	6.35
E	54.61
G	6.35
H	1.27 (T.P.)
I	8.89
J	24.495
K	42.18
L	17.78
M	38.1
M1	18.32
M2	19.78
N	4.0 MAX.
P	1.0
Q	R2.0
R	4.0±0.1
S	ϕ3.0
T	1.27±0.1
U	4.0 MIN.
V	0.2±0.15
W	1.0±0.05
X	2.54 MIN.
Y	3.0 MIN.
Z	3.0 MIN.