

MC4558V

Dual Wide Bandwidth Operational Amplifiers

The MC4558V combine all the outstanding features of the MC1458 and, in addition offer three times the unity gain bandwidth of the industry standard.

- 2.0 MHz Unity Gain Bandwidth Guaranteed
- Internally Compensated
- Short Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
	V_{EE}	-18	
Input Differential Voltage	V_{ID}	± 30	V
Input Common Mode Voltage (Note 1.)	V_{ICM}	± 15	V
Output Short Circuit Duration (Note 2.)	t_{SC}	Continuous	
Ambient Temperature Range	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$

1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply.

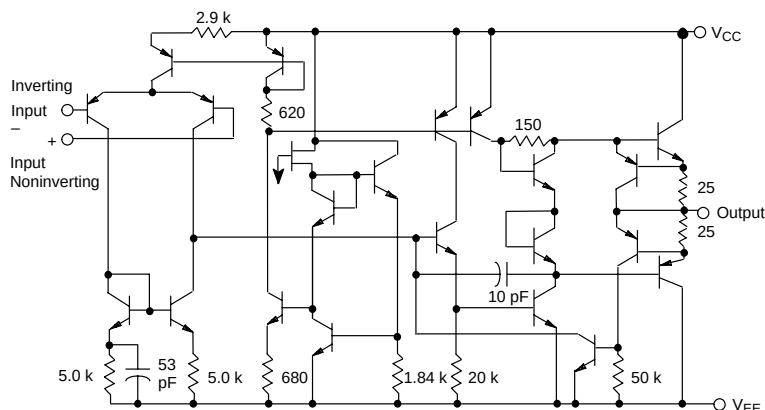


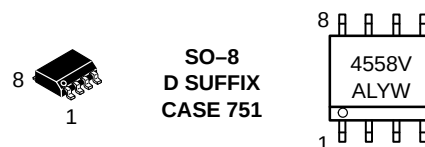
Figure 1. Representative Schematic Diagram
(1/2 of Circuit Shown)



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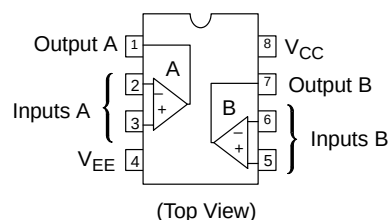
<http://onsemi.com>

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
MC4558VD	SO-8	98 Units/Rail
MC4558VDR2	SO-8	2500 Tape & Reel

MC4558V

FREQUENCY CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Unity Gain Bandwidth	BW	2.0	2.8	–	MHz

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	nA
Input Bias Current (Note 1.)	I_{IB}	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	M Ω
Input Capacitance	C_i	–	1.4	–	pF
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	–	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	A_{VOL}	20	200	–	V/mV
Output Resistance	r_o	–	75	–	Ω
Common Mode Rejection ($R_S \leq 10\text{ k}\Omega$)	CMR	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	PSRR	–	30	150	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}\Omega$) ($R_L \geq 2.0\text{ k}\Omega$)	V_O	± 12 ± 10	± 14 ± 13	– –	V
Output Short Circuit Current	I_{SC}	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	–	70	170	mW
Transient Response (Unity Gain) ($V_i = 20\text{ mV}$, $R_L \geq 2.0\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Rise Time ($V_i = 20\text{ mV}$, $R_L \geq 2.0\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Overshoot ($V_i = 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Slew Rate	t_{TLH} os SR	– – 1.0	0.3 15 1.6	– – –	μs % V/ μs

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{high}$ to T_{low} , unless otherwise noted. See Note 2.)

Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	–	–	7.5	mV
Input Offset Current ($T_A = T_{high}$) ($T_A = T_{low}$) ($T_A = -40^\circ$ to $+85^\circ\text{C}$)	I_{IO}	– – –	– – –	– – 300	nA
Input Bias Current ($T_A = T_{high}$) ($T_A = T_{low}$) ($T_A = -40^\circ$ to $+85^\circ\text{C}$)	I_{IB}	– – –	– – –	– – 800	nA
Common Mode Input Voltage Range	V_{ICR}	–	–	–	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$)	A_{VOL}	15	–	–	V/mV
Common Mode Rejection ($R_S \leq 10\text{ k}\Omega$)	CMR	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}\Omega$)	PSRR	–	–	–	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}\Omega$) ($R_L \geq 2.0\text{ k}\Omega$)	V_O	± 12 ± 10	± 14 ± 13	– –	V
Supply Currents (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	I_D	– –	– –	5.0 6.7	mA
Power Consumption (Both Amplifiers) ($T_A = T_{high}$) ($T_A = T_{low}$)	P_C	– –	– –	150 200	mW

- I_{IB} is out of the amplifier due to PNP input transistors.
- $T_{high} = +85^\circ\text{C}$, $T_{low} = -40^\circ\text{C}$.

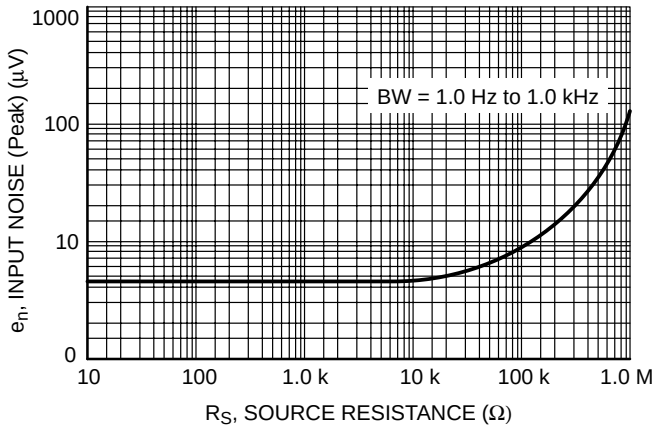


Figure 2. Burst Noise vs. Source Resistance

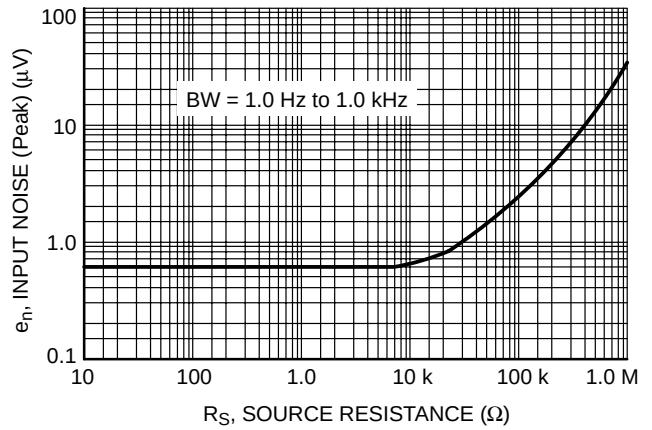


Figure 3. RMS Noise vs. Source Resistance

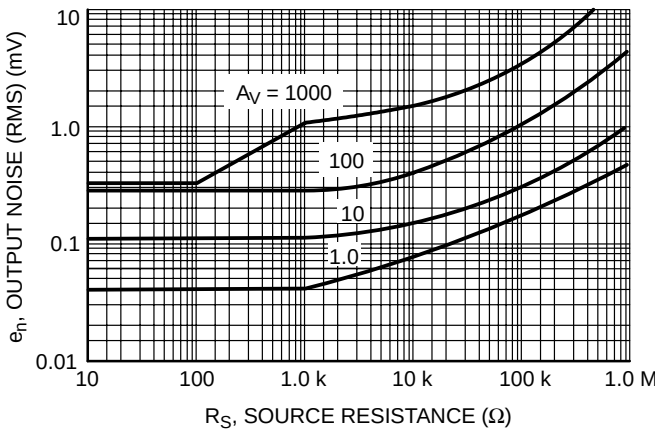


Figure 4. Output Noise vs. Source Resistance

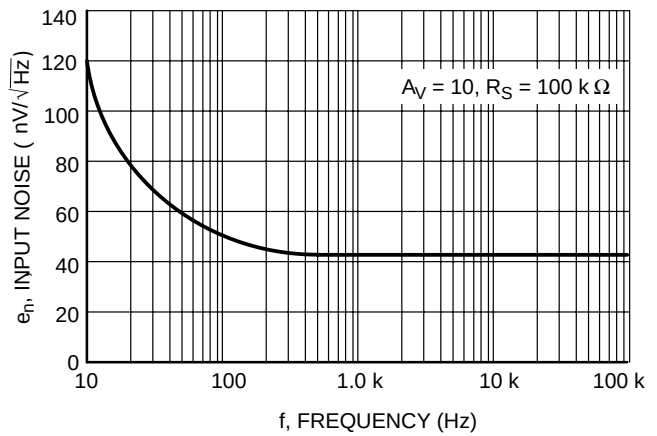
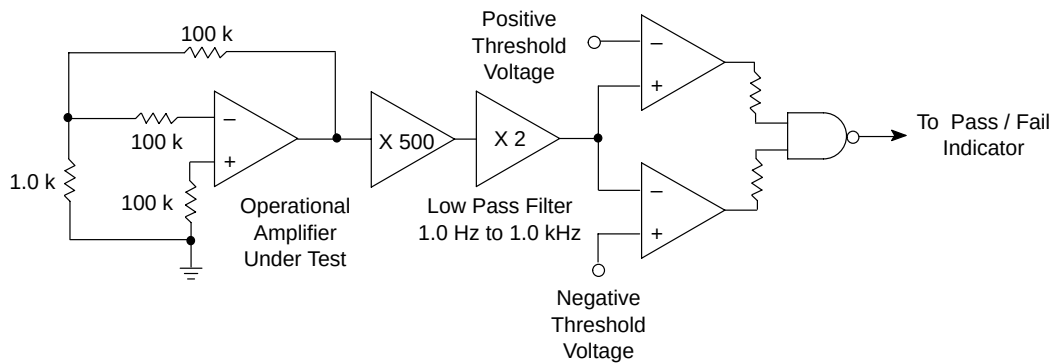


Figure 5. Spectral Noise Density



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier.

Figure 6. Burst Noise Test Circuit

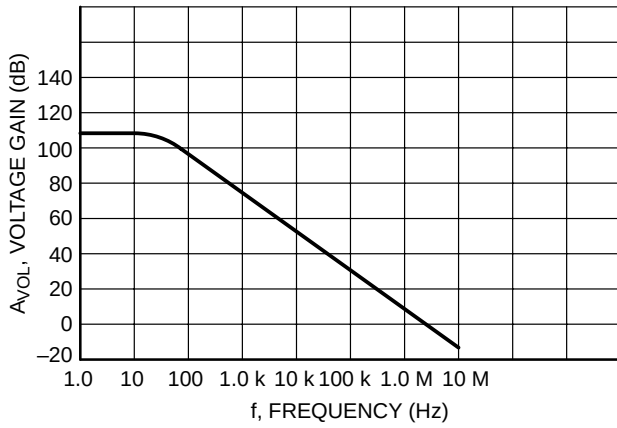


Figure 7. Open Loop Frequency Response

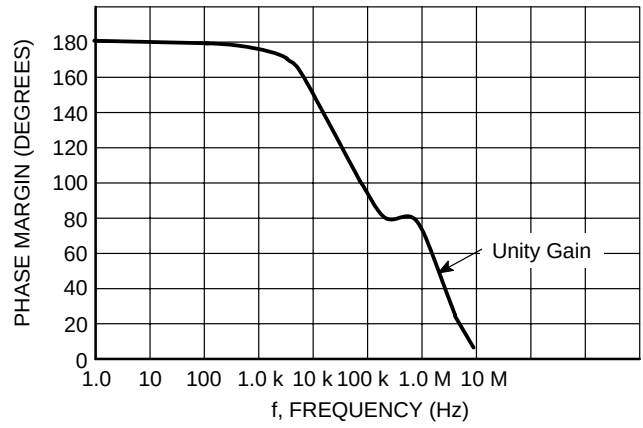


Figure 8. Phase Margin versus Frequency

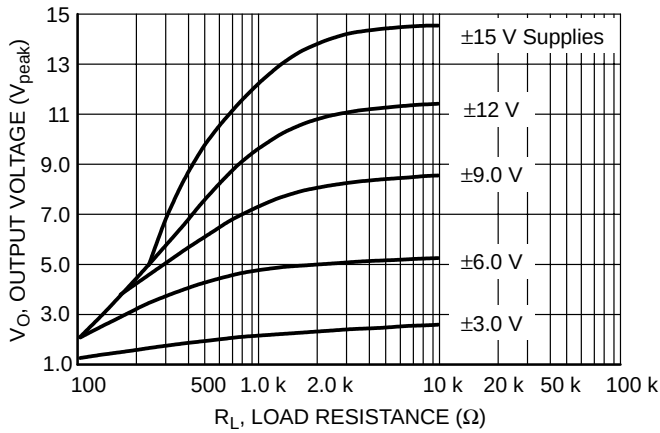


Figure 9. Positive Output Voltage Swing versus Load Resistance

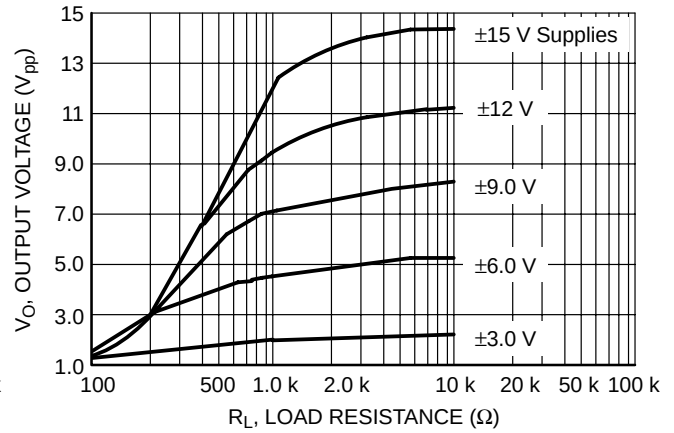


Figure 10. Negative Output Voltage Swing versus Load Resistance

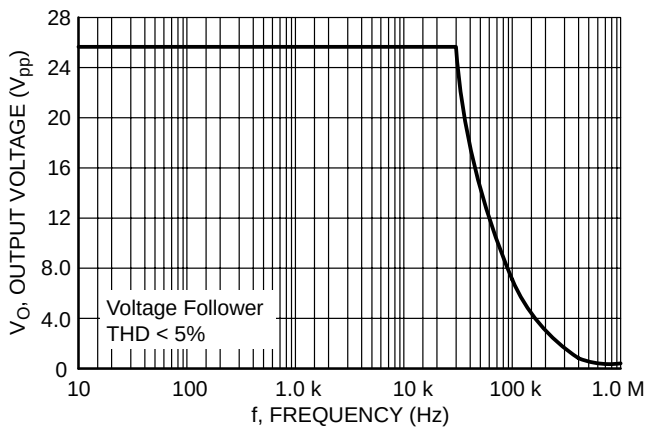


Figure 11. Power Bandwidth (Large Signal Swing versus Frequency)

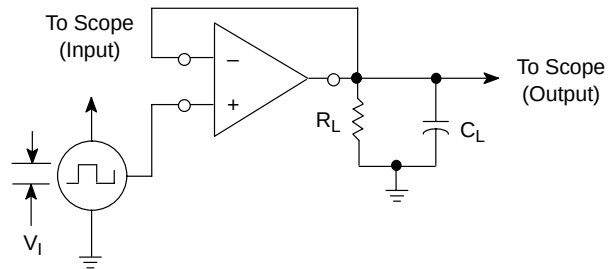
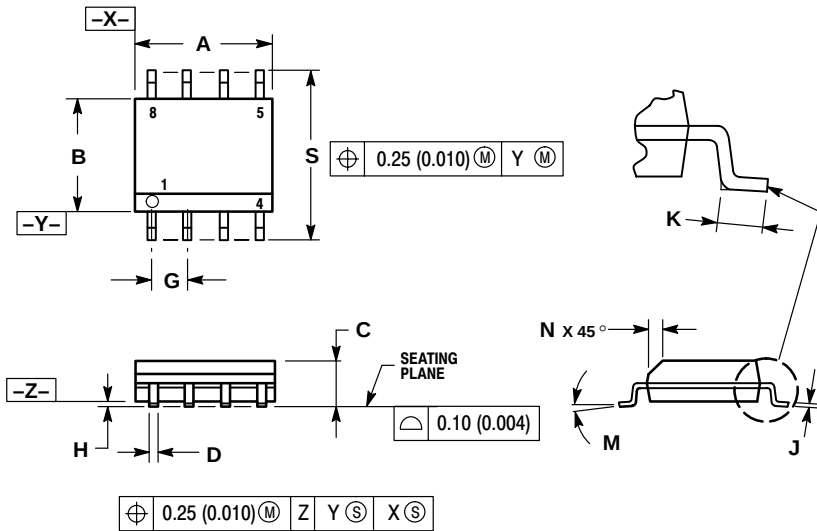


Figure 12. Transient Response Test Circuit

MC4558V

PACKAGE DIMENSIONS

SO-8
D SUFFIX
CASE 751-07
ISSUE V



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

Notes

Notes

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