DUAL DECADE UP/DOWN COUNTER

MC4354
MC4054

DUAL BINARY UP/DOWN COUNTER

MC4355
MC4055

These devices are presettable, synchronous (clocked) up/down coutners. The MC4354/4054 is a decade counter consisting of two separate but cascaded counters. One counter counts the least significant decade, and the other the most significant decade. The counter counts to 1001 1001, or 99, before resetting to 0000 0000. The MC4355/4055 is a binary counter consisting of two separate hexadecimal counters which are cascaded. This counter is essentially an 8-bit binary counter which counts to 1111 1111, or 255, before resetting to 0000 0000.

Both counters in a package are preset by means of a high level on the Preset (P) input. (The Preset input overrides all synchronous inputs: Clock, $\overline{SEI}$, and $\overline{UE}$.) Information is then loaded into the least significant counter thru inputs D0, D1, D2 and D3, and into the most significant counter thru inputs D0', D1', D2', and D3'.

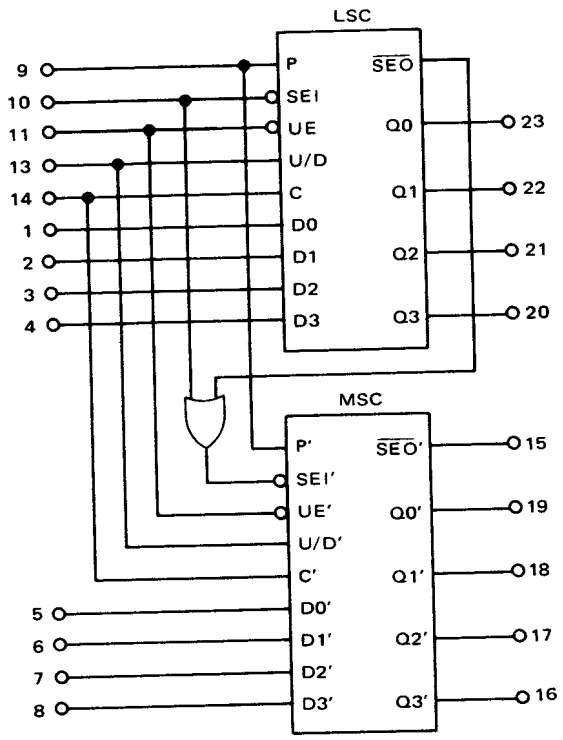
The Up/$\overline{Down}$ input determines the mode of counting: up when high, down when low.

Two Enable inputs are part of these circuits. The Unit Enable ($\overline{UE}$) affects only the counters within a specific package. The Serial Enable ($\overline{SEI}$) not only affects a particular package, but also furnishes a signal at the Serial Enable Output ($\overline{SEO}$) for control of succeeding packages in a counter chain. A high input to $\overline{SEI}$ forces $\overline{SEO}$ high. When $\overline{SEI}$ is low, $\overline{SEO}$ decodes the terminal state of the counter, independently from the $\overline{UE}$ control, when the counters are in the terminal state. (Terminal state is defined as 0000 0000 when counting down, and as 1111 1111 (256) for the binary counter and 1001 1001 (99) for the decade counter when counting up.)

Both the Serial Enable ($\overline{SEI}$) and the Unit Enable ($\overline{UE}$) must be low for the counter to be clocked. Logic levels on both of these lines must be settled prior to the trailing edge of the Clock, and must remain stable while the Clock is low.

The count state may change only on the leading edge of a Clock pulse. Any changes on the control inputs (Up/$\overline{Down}$, $\overline{SEI}$, and $\overline{UE}$) must be made while the Clock is high.

Counting data is read out on Q0 thru Q3 for the least significant counter, and Q0' thru Q3' for the most significant counter.



Input Loading Factors:
$\overline{SEI}$ = 3
$\overline{UE}$, Clock = 2
All Others = 1
Output Loading Factor = 10
Total Power Dissipation = 600 mW typ/pkg
Maximum Operating Frequency = 12 MHz typ

V_{CC} = Pin 24
Gnd = Pin 12

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COUNT	INPUTS													OUTPUTS								
						TENS				UNITS				TENS				UNITS				
	C	$\overline{UE}$	$\overline{SEI}$	U/$\overline{D}$	P	D3′	D2′	D1′	D0′	D3	D2	D1	D0	Q3′	Q2′	Q1′	Q0′	Q3	Q2	Q1	Q0	$\overline{SEO}$
0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	0	1	0	1	0	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	1
	A	1	0	1	0									0	0	0	0	0	0	0	0	1
	1	1	0	1	0									0	0	0	0	0	0	0	0	1
	1	0	1	1	0									0	0	0	0	0	0	0	0	1
	0	0	1	1	0									0	0	0	0	0	0	0	0	1
	A	0	1	1	0									0	0	0	0	0	0	0	0	1
	1	0	1	1	0									0	0	0	0	0	0	0	0	1
	1	0	0	1	0									0	0	0	0	0	0	0	0	1
	0	0	0	1	0									0	0	0	0	0	0	0	0	1
1	A	0	0	1	0									0	0	0	0	0	0	0	1	1
2	A	0	0	1	0									0	0	0	0	0	0	1	0	1
3	A	0	0	1	0									0	0	0	0	0	0	1	1	1
4	A	0	0	1	0									0	0	0	0	0	1	0	0	1
5	A	0	0	1	0									0	0	0	0	0	1	0	1	1
6	A	0	0	1	0									0	0	0	0	0	1	1	0	1
7	A	0	0	1	0									0	0	0	0	0	1	1	1	1
8	A	0	0	1	0									0	0	0	0	0	1	1	1	1
9	A	0	0	1	0									0	0	0	0	1	0	0	0	1
10	A	0	0	1	0									0	0	0	0	1	0	0	1	1
11	A	0	0	1	0									0	0	0	1	0	0	0	0	1
12	A	0	0	1	0									0	0	0	1	0	0	0	1	1
⋮	84A	0	0	1	0									0	0	0	1	0	0	1	0	1
97	A	0	0	1	0									*								1
98	A	0	0	1	0									1	0	0	1	0	1	1	1	1
99	A	0	0	1	0									1	0	0	1	1	0	1	0	1
00	1	0	0	1	0									1	0	0	1	1	0	0	1	1
00	1	0	0	0	0									1	0	0	1	0	0	0	0	1
00	0	0	0	0	0									0	0	0	0	0	0	0	0	1
99	A	0	0	0	0									0	0	0	0	0	0	0	1	1
98	A	0	0	0	0									0	0	0	0	1	0	0	0	1
97	A	0	0	0	0									0	0	0	0	1	0	0	1	1
⋮	94A	0	0	0	0									0	0	0	0	1	0	1	0	1
02	A	0	0	0	0									**								1
01	A	0	0	0	0									0	0	0	0	0	0	0	0	1
00	1	0	0	0	0									0	0	0	0	0	0	0	1	1
00	1	0	0	1	0									0	0	0	0	0	0	0	0	1
00	1	0	0	1	0									0	0	0	0	0	0	0	1	1
97	0	0	0	0	0									0	0	0	0	0	0	0	0	1
97	0	0	0	0	0									0	0	0	0	0	0	0	1	1
96	A	0	0	0	0									0	0	0	0	0	0	0	0	1
95	A	0	0	0	0									0	0	0	0	0	0	0	1	1
0	0	0	0	0	1	1	0	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0
						1	0	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0
						X	X	X	X	X	X	X	X	0	0	0	0	0	0	1	1	0
						0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

X = Don't Care

*Outputs count from 12 to 96 during these 84 clock pulses.

**Outputs count from 97 to 13 during these 94 clock pulses.

A = 

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The MC4355/4055 works in the same manner as the MC4354/4054 except the least significant counter counts to 1111 before clocking the most significant counter, and both counters count to 1111 1111 or 255 before resetting to 0.