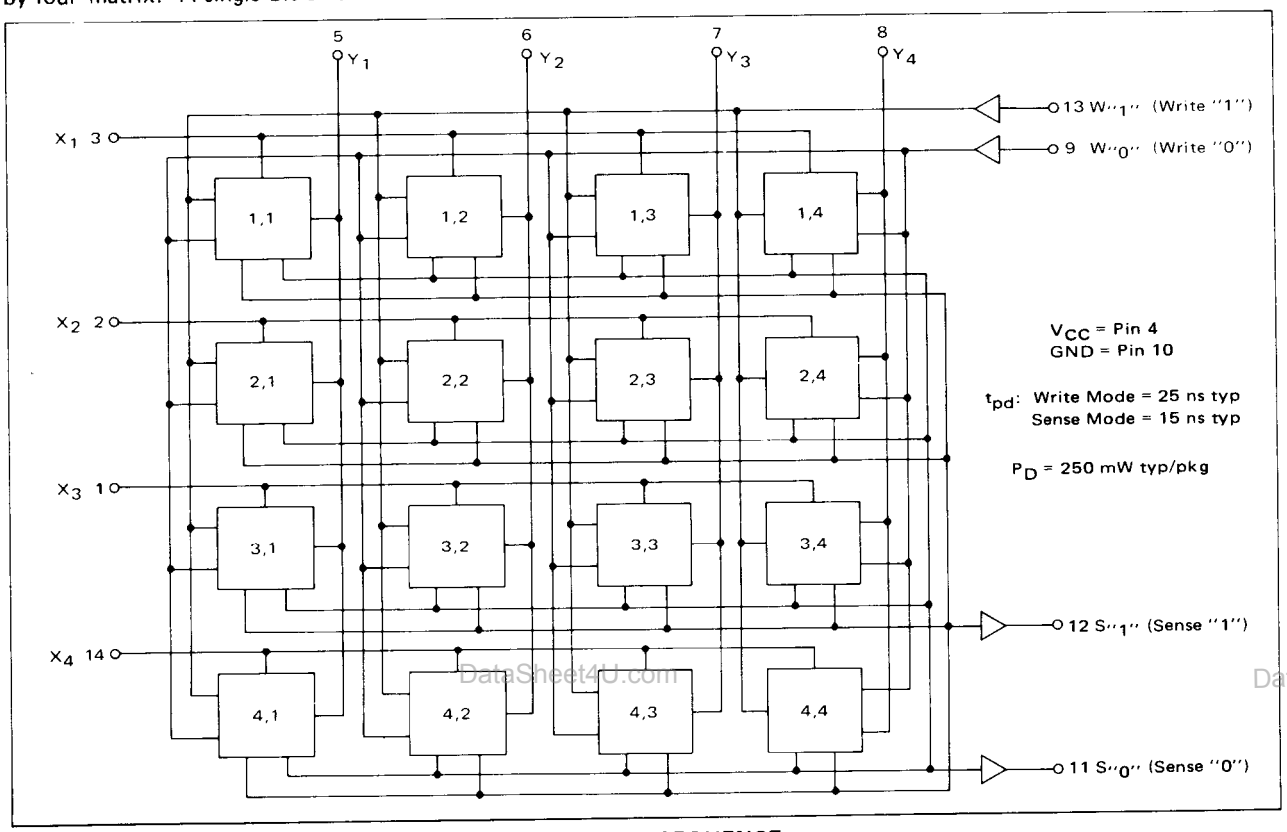
16-BIT SCRATCH PAD
MEMORY CELL

MC4304 • MC4305
MC4004 • MC4005

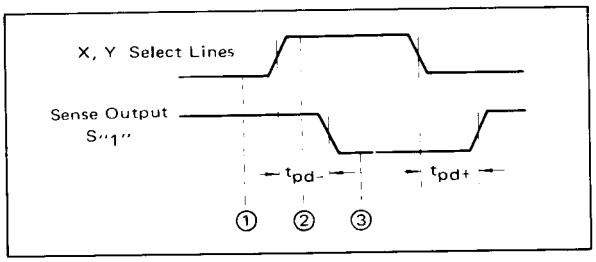
This 16-Bit memory cell serves as the basic building block for scratch pad memory systems having cycle times of less than 100 ns. The basic cell provides 16 words of one-bit memory operating in the non-destructive readout (NDRO) mode.

The memory contains 16 flip-flops arranged in a four-by-four matrix. A single bit of the matrix is selected by driving one of four X select lines and one of four Y select lines above the select threshold. Two sense amplifiers are shared by all 16 bits and provide a double rail output from the selected bit. The sense output of many devices can be "wired ORed" together since the output stage does not have a pullup resistor or network. Two write amplifiers allow a "1" or a "0" to be written into a selected bit.



– OPERATING SEQUENCE –

FIGURE 1 – READ MODE TIMING DIAGRAM

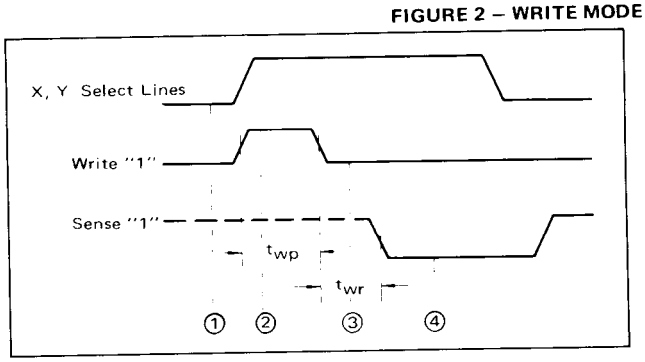


① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Desired bit selected by driving the appropriate X and Y select lines more positive than +2.1 V.

③ After the turn-on delay time(t_{pd-}), the S"1" output will be low (less than +0.45 V) and the S"0" output will be high (more than +2.5 V), providing that a "1" is stored in the selected bit.

FIGURE 2 – WRITE MODE TIMING DIAGRAM



① All X and Y selection lines and both write inputs are low (less than +0.8 V).

② Bit location selected by driving the appropriate X and Y select lines more positive than +2.1 V. To write a "1", drive the write "1" input more positive than +2.1 V for a minimum time of 25 ns (t_{wp}).

③ Write "1" line returned to low state.

④ The stored bit can be read after the write recovery time (t_{wr}) of 40 ns. (The sense output is in an indeterminate state between steps 2 and 4.)