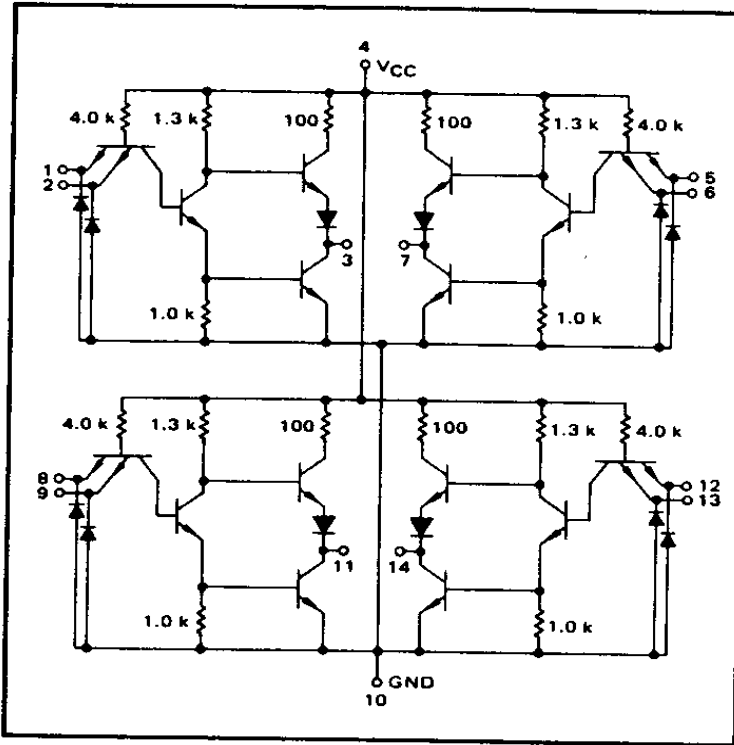


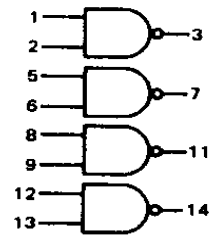
QUAD 2-INPUT "NAND" GATE

MTTL I MC500/400 series

MC508 • MC558
MC408 • MC458



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.



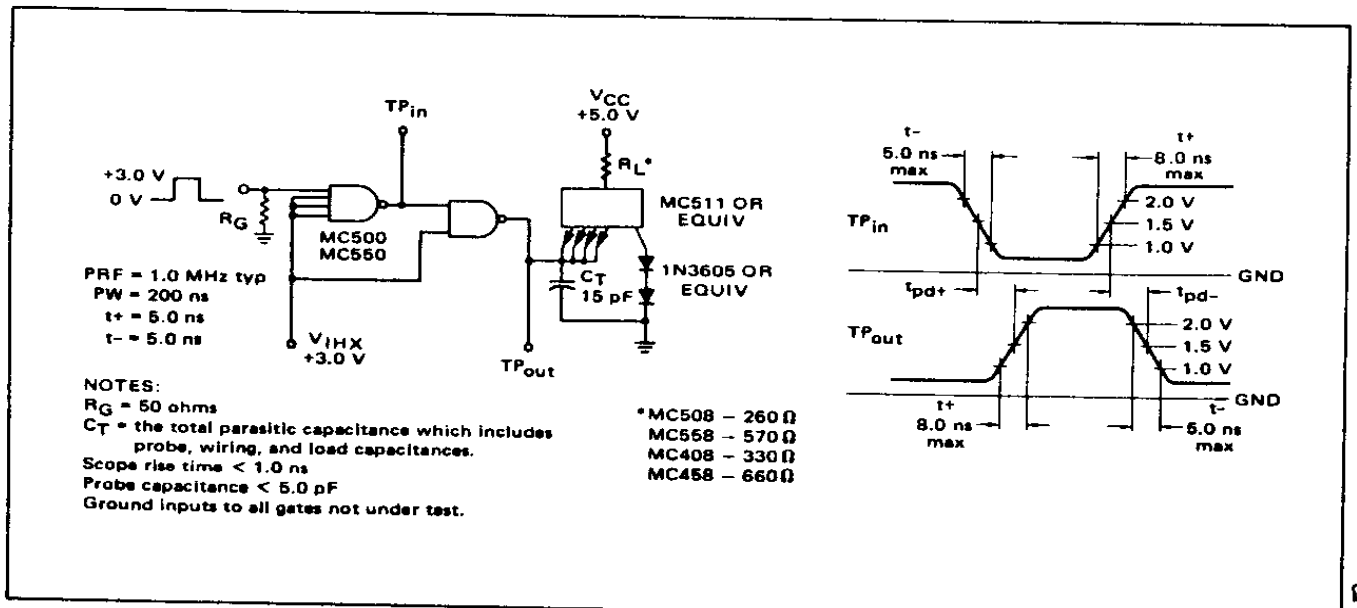
Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1} + \overline{2}$

Total Power Dissipation = 60 mW typ/pkg
Propagation Delay Time = 10 ns typ

TYPE NO.	INPUT LOADING FACTOR	(I _F)	OUTPUT DRIVE	(I _{OL})	TEMPERATURE RANGE
MC508 MC558	1	(-1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	-55°C to +125°C
MC408 MC458	1	(-1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

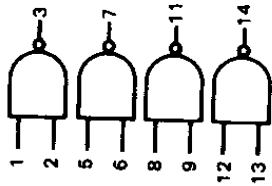
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



@ Test Temperature
 -55°C
 +25°C
 +125°C
 MC508, MC558
 0°C
 +25°C
 +75°C
 MC408, MC458

Characteristic	Symbol	Pin Under Test	MC508, MC558 Test Limits						MC408, MC458 Test Limits								
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C				
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Forward Current	I_F	1	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	-	-1.66	-	-	-	-
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	-	100	-
Breakdown Voltage	$BV_{in\ "0\ "}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5
	$BV_{in\ "1\ "}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5
Output Voltage	$V_{out\ "0\ "}$	3	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-
	$V_{out\ "1\ "}$	3	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	2.4	-	2.5
Leakage Current	I_{OLK}	3	-	250	-	250	-	250	-	250	-	250	-	250	-	250	-
Short-Circuit Current	I_{SC}	3	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-	0.40	-
	V_{OH}	3	2.6	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	3.0	-	3.1
Power Requirements (Total Device)	I_{max}	4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	Maximum Power Supply Current	4	-	24	-	24	-	24	-	24	-	24	-	24	-	24	-
Power Supply Drain	I_{PDH}	4	-	12	-	12	-	12	-	12	-	12	-	12	-	12	-
Switching Parameters	t_{pd}	1,3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	t_{pd}	1,3	-	20	-	20	-	20	-	20	-	20	-	20	-	20	-
	t_r	1,3	-	-	-	8.0	-	-	-	8.0	-	-	-	-	-	-	-
Fall Time	t_f	1,3	-	-	-	5.0	-	-	-	5.0	-	-	-	-	-	-	-

* Prime Fan-Out.
 † Ground inputs to gates not under test, during ALL tests unless otherwise noted.
 ‡ The inputs to all gates must be ungrounded.

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