

DUAL J-K FLIP-FLOP

MTTL III MC3100/3000 series

MC3161F • MC3061F
MC3161L • MC3061L,P

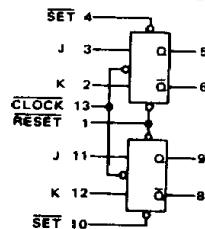
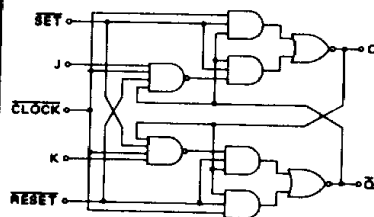
This dual JK flip-flop triggers on the negative edge of clock. Each flip-flop is provided with a separate direct SET input in addition to the common direct RESET input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between

the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Setup and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input. In addition, both flip-flops may be reset simultaneously by using the common RESET in a similar manner.

LOGIC DIAGRAM

1/2 OF DEVICE SHOWN.
 RESET AND CLOCK COMMON TO BOTH



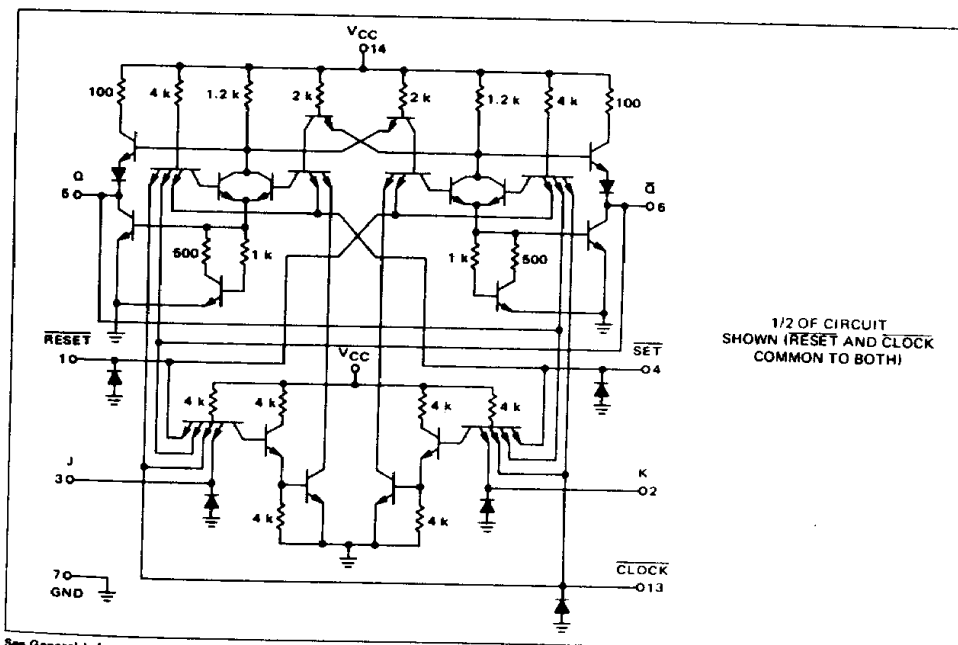
Input Loading Factors:
 SET = 1.75
 RESET, CLOCK = 3.7
 J, K = 0.75
 Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q ⁿ	Q ⁿ⁺¹
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics
 (V_{CC} = 5.0 V, T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
 Toggle Frequency = 50 MHz typ
 Logical "1" Setup Time = 8.0 ns
 Logical "0" Setup Time = 8.0 ns
 Logical "1" and "0" Hold Times = 0 ns
 t_{pd} = 12 ns
 t_{pd} = 12 ns



1/2 OF CIRCUIT
 SHOWN (RESET AND CLOCK
 COMMON TO BOTH)

See General Information section for packaging.

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MC3161F, MC3061F/MC3161L, MC3061L,P (continued)

OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

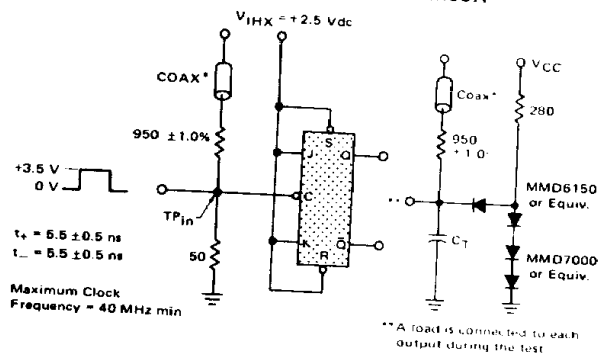
The direct SET (individual) inputs and RESET (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the Q = 1 state by applying a low level to the SET input or reset to the Q = 0 state by applying a low level to the RESET input. If these inputs are not used they should be returned to a voltage

age between 2.0 and 5.5 Vdc.

Negative edge triggering: The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

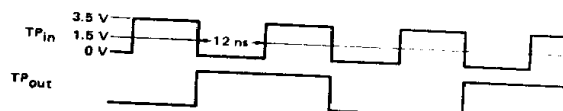
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



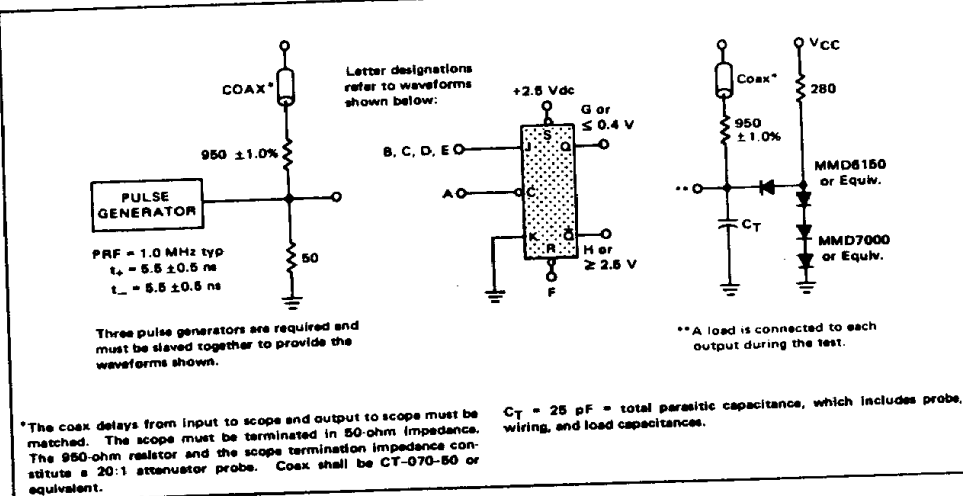
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MC3161F, MC3061F/MC3161L, MC3061L,P (continued)

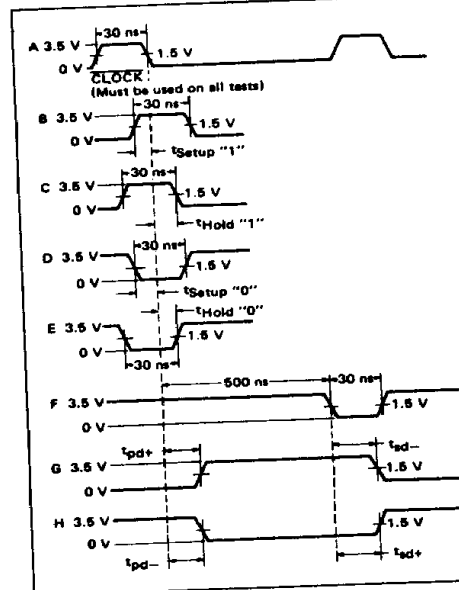
OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs and RESET Input; to test other inputs, refer to Test Procedures Chart)



VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

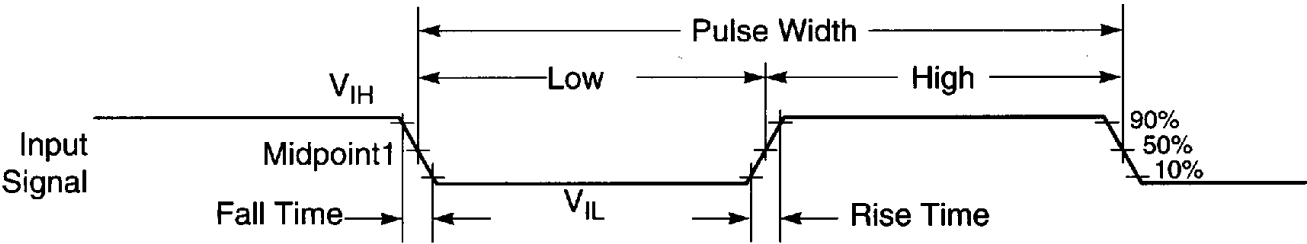
TEST	INPUT						LIMITS (ns)
	J*	SET*	RESET*	K*	Q*	G*	
tSetup "1" J	B	2.5 V	F	Gnd	G	H	10
tHold "1" J	C	2.5 V	F	Gnd	G	H	0**
tSetup "0" J	D	2.5 V	F	Gnd	≤0.4 V	≥2.5 V	10
tHold "0" J	E	2.5 V	F	Gnd	≤0.4 V	≥2.5 V	0**
tSetup "1" K	Gnd	F	2.5 V	B	H	Q	10
tHold "1" K	Gnd	F	2.5 V	C	H	Q	0**
tSetup "0" K	Gnd	F	2.5 V	D	≥2.5 V	≤0.4 V	10
tHold "0" K	Gnd	F	2.5 V	E	≥2.5 V	≤0.4 V	0**
tpd+	Delay from CLOCK to Q during tSetup "1" J test. Delay from CLOCK to Q during tSetup "1" K test.						10
tpd-	Delay from CLOCK to Q during tSetup "1" J test. Delay from CLOCK to Q during tSetup "1" K test.						10
tcd+	Delay from SET to Q during tSetup "1" K test. Delay from RESET to Q during tSetup "1" J test.						10
tcd-	Delay from SET to Q during tSetup "1" K test. Delay from RESET to Q during tSetup "1" J test.						10

*Letters shown in those columns refer to waveforms shown at the left.
 **Hold is typically a negative number.

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AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except $\overline{EXTAL}$, $\overline{RESET}$, $MODA$, $MODB$, and $MODC$. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference