MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC14400
MC14401
MC14402
MC14403
MC14405

2

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

CODEC-FILTER
PCM MONO-CIRCUIT

CODEC-FILTER PCM-MONO-CIRCUIT

The MC14400, MC14401, MC14402, MC14403, and MC14405 are all per channel codec-filter PCM mono-circuits. These devices perform the voice digitizing and recovery, as well as the band limiting and signal restoration necessary in PCM systems. The MC14400 and MC14403 are general purpose devices that are offered in a 16-pin package. They are designed to operate in both synchronous and asynchronous applications and contain an on-chip precision voltage reference. The MC14401 is the same device, but offered in an 18-pin package. In addition, it offers the user the capability of selecting from three peak overload voltages (2.5, 3.15 and 3.78 V). The MC14405 is a synchronous device in a 16-pin package intended for instrument use. The MC14402 is the full feature device which presents all of the options available on the chip. This device is packaged in a 22-pin DIP and 28-pin chip carrier package, and contains all the features of the MC14400 and MC14401 plus several more. Most of these features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

The devices were designed to be upward compatible with the MC14404/06/07 codecs and other industry standard codecs. They also maintain compatibility with Motorola's family of TSACs (MC14416/MC14417/MC14418) as well as the MC3419 SLIC.

The PCM codec-filter mono-circuits utilize CMOS due to its reliable low-power performance and proven capability for complex analog/ digital LSI functions.

MC14400

- 16-Pin Package
- On-Chip Precision Voltage Reference (3.15 V)
- Power Dissipation — 45 mW at 2.048 MHz at 10 V
  0.1 mW Powered Down at 10 V
- Compatibility with Various Supply Configurations: ±5, ±6, +10, +12 Volts (5%)
- Pin Selectable TTL and CMOS Digital Levels
- Automatic Prescale Divide of Any One of 6 Clock Frequencies (128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz) to Generate the Internal Sequencing Clock
- Pin Selection of Both A-LAW/Mu-LAW Companding and D3/D4 or CCITT Digital Formats
- Output Drive Capability for 600 and 900 Ohm Loads of +12 dBm
- Synchronous and Asynchronous Operation
- On-Chip Attendent Interrupt Conferencing
- Transmit Bandpass and Receive Low-Pass Filters on Chip

MC14401 — All of the Above Plus:

- 18-Pin Package
- Selectable Peak Overload Voltages (2.5, 3.15 and 3.78 Volts)
- Access to the "Minus" Input of the Tx Input Op Amp

MC14402 — All of the Above Plus:

- 22-Pin Package
- Variable Data Clocks (64 kHz to 3.088 MHz)
- Access to Transmit Input Amplifier
- An External Precision Reference May Be Used
- External Gain Adjust for Complex SLIC Configurations

MC14403

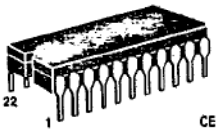
- 16-Pin Package
- Same Device as MC14400 with Access to Transmit Input Amplifier with Single Ended Receive Output
- MSI Tied Internally to TDE

MC14405

- 16-Pin Package
- Same Device as MC14403 with Common 64 kHz to 3.088 MHz Data Clocks

MC14400/03/05
L SUFFIX
CERAMIC PACKAGE
CASE 620

MC14401
L SUFFIX
CERAMIC PACKAGE
CASE 726



MC14402
L SUFFIX
CERAMIC PACKAGE
CASE 736

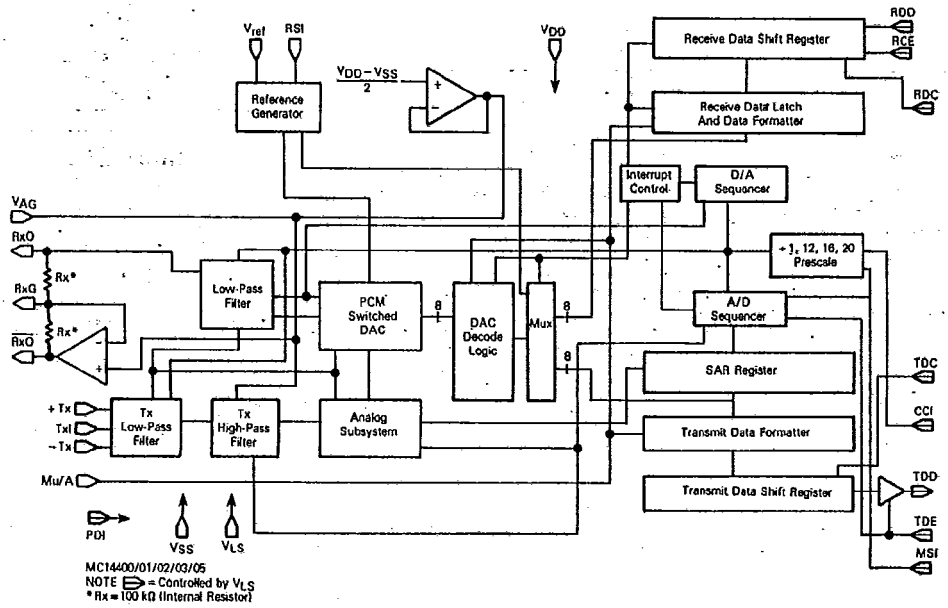
MC14402
Z SUFFIX
28-PIN CHIP CARRIER
CASE 763

ORDERING INFORMATION

MC14XXXXX

- 1 CCITT (G7.12)
- 2 D3/D4 (PUB 43801)
- L Ceramic Package
- Z Leadless Ceramic Package

PCM MONO-CIRCUIT BLOCK DIAGRAM



DEVICE DESCRIPTIONS

There are five distinct versions of the Motorola PCM mono-circuit.

MC14400

The MC14400 PCM mono-circuit is a PCM codec-filter intended for standard word interleaved synchronous or asynchronous applications. The TDC pin on this device is the input to both the TDC and CCI functions in the pin description. Consequently, for MSI = 8 kHz, TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty) 1.536, 1.544, 2.048 or 2.56 MHz. (For other data clock frequencies see MC14402 or MC14405.) The internal reference is set for 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM mono-circuit. All other functions are described in the pin description.

MC14401

The MC14401 PCM mono-circuit offers the same features and is for the same application as the MC14400, but offers two additional pins and features. The reference select input allows the full scale level of the device to be set at 2.5 Vp, 3.15 Vp or 3.78 Vp. The – Tx pin allows for external transmit gain adjust and simplifies interface to the MC3419 SLIC. Otherwise, it is identical to MC14400.

MC14402

The MC14402 PCM mono-circuit is the full featured 22-pin device. It is intended for use in applications requiring maximum flexibility. The MC14402 contains all the features of the MC14400 and MC14401. The MC14402 is intended for bit interleaved or word interleaved operation with data clock frequencies which are non standard or time varying. One of the five standard frequencies (listed above) is applied to the CCI input and the data clock inputs can be any frequency between 64 kHz and 3.088 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference and RxG and +Tx provide maximum flexibility for analog interface.

MC14403

The MC14403 PCM mono-circuit is intended for standard word interleaved asynchronous or synchronous applications. TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty) 1.536, 1.544, 2.048 or 2.56 MHz. (For other data clock frequencies see MC14402 or MC14405.) The internal reference is set of 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM mono-circuit. The +Tx and – Tx inputs provide maximum flexibility for analog interface. All other functions are described in the pin description.

MC14405

The MC14405 PCM mono-circuit is intended for word interleaved synchronous applications. The MC14405 has all the features of the MC14403 but internally connects TDC and RDC (see pin description) to the DC pin. One of five standard frequencies (listed above) should be applied to CCI and the DC input can be any frequency between 64 kHz and 3.088 MHz.

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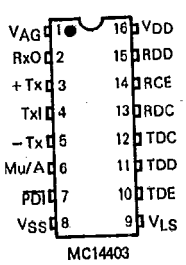
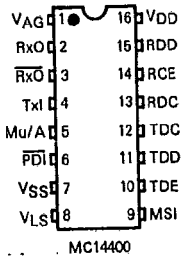
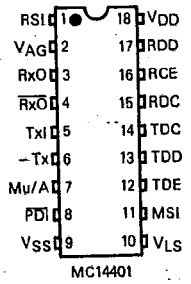


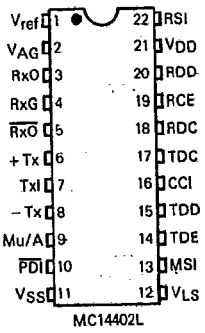
MC14403



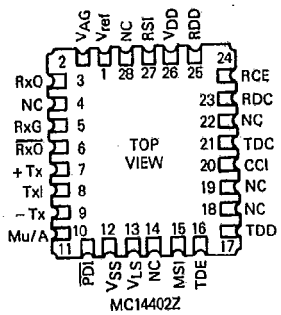
MC14400



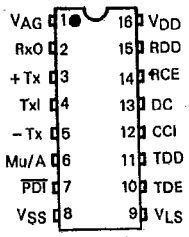
MC14401



MC14402L



MC14402Z



MC14405

MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage	V_{CC} to V_{SS}	6	10 to 12	13	V
Power Dissipation CMOS Mode 10 V TTL Mode 10 V	V_{DD} to V_{SS}	– –	45 75	70 110	mW
Power Down Dissipation 10 V	V_{DD} to V_{SS}	–	0.1	1.0	mW
Frame Rate Transmit and Receive	MSI	7.5	8.0	8.5	kHz
Data Rate MC14400, MC14401, and MC14403 (Must Use One of These Frequencies) ±2%	TDC, RDC	– – – – –	128 1536 1544 2048 2560	– – – – –	kHz
Data Rate MC14402, MC14405		64	–	3088	kHz
Full Scale Output and Input Levels MC14400, MC14403, MC14405 MC14401 and MC14402, $V_{ref}=V_{SS}$ RSI=V_{DD} RSI=V_{SS} RSI=V_{AG}	RxO, Txl	– – – –	3.15 3.78 3.15 2.50	– – – –	Vp

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DIGITAL LEVELS (T_A = 0 to 70°C)

Parameter		Symbol	V_{DD} to V_{SS}	Min	Typ	Max	Unit
CMOS Mode							
TDE, RCE, RDD, $\overline{PDI}$, RDC, TDC, DC, CCI, MSI	"0"	–	12	–	5.25	3.6	V
	"1"	–	12	8.4	6.75	–	
TTL Mode							
TDE, RCE, RDD, $\overline{PDI}$, RDC, TDC, DC, CCI, MSI	"0"	–	10	–	V_{LS} + 1.0	V_{LS} + 0.8	V
	"1"	–	10	V_{LS} + 2.0	V_{LS} + 1.8	–	
TDD Output Current (TTL Mode)	V_{OH} = 2.4 V	I_{OH}	10	150	–	–	µA
	V_{OL} = 0.8 V	I_{OL}	–	1.6	–	–	ma

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, 0 dBm0 = +6 dBm@600 Ω, V_{LS} = V_{AG} = 0, T_A = 0 to 70°C, TDC = RDC; TDE = RCE = 8 kHz)

Characteristic	E to E		A/D		D/A		Unit
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz)	−0.3	+0.3	−0.3	+0.3	−0.3	+0.3	dB
Gain vs Level Tone (Relative to −10 dBm0, 1.02 kHz)							
+3 to −40 dBm0	−0.4	+0.4	−0.2	+0.2	−0.2	+0.2	dB
−40 to −50 dBm0	−0.8	+0.8	−0.4	+0.4	−0.4	+0.4	
−55 dBm0	−1.6	+1.6	−1.0	+1.0	−0.8	+0.8	
Gain vs Level — Pseudo Noise (A-Law Only, MC144XXL1 Only) (Relative to −10 dBm0)							
−10 to −55 dBm0	−0.45	+0.45	–	–	–	–	dB
−60 dBm0	−0.90	+0.90	–	–	–	–	
Total Distortion — 1.02 kHz Tone (C Message)							
0 to −30 dBm0	35	–	35	–	36	–	dB
−40 dBm0	29	–	29	–	30	–	
−45 dBm0	24	–	24	–	26	–	
Total Distortion with Noise (A-Law Only, MC144XXL1 Only)							
−3 dBm0	27.5	–	–	–	–	–	dB
−6 to −27 dBm0	35	–	–	–	–	–	
−34 dBm0	33.1	–	–	–	–	–	
−40 dBm0	28.5	–	–	–	–	–	
−55 dBm0	13.5	–	–	–	–	–	
Idle Noise							
(Mu Law, C Message)	–	18	–	18	–	13	dBrnCo
(A Law, Psophometric — MC144XXL1 Only)	–	−68	–	−68	–	−75	dBmOp
Frequency Response (Relative to −10 dBm0, 1.02 kHz)							
15 to 60 Hz	–	−23	–	−23	–	0.15	dBm0
300 to 3000 Hz	−0.30	+0.30	−0.15	+0.15	−0.15	+0.15	
3400 Hz	−1.6	0	−0.8	0	−0.8	0	
4000 Hz	–	−28	–	−14	–	−14	
4600 Hz	–	−60	–	−32	–	−30	
Inband Spurious (1.02 kHz@0 dBm0)							
300 to 3400 Hz	–	−43	–	−43	–	−43	dBm0
Out-of-Band Spurious (0 to 12 kHz in, @0 dBm0)							
0 to 3400 Hz	–	−30	–	−30	–	–	dBm0
3400 to 4600 Hz	–	−28	–	–	–	–	
4600 Hz to 12 kHz	–	−30	–	–	–	–	
Idle Noise Selective							
@ 8 kHz with V_{AG} = TxI Measure at RxO, 30 Hz Bandwidth	–	−50	–	–	–	–	dBm0
Group Delay Difference							
0 dBm0, TDC = RDC = 2.048 MHz							
500 to 600 Hz	–	80	–	–	–	–	µsec
600 to 1000 Hz	–	60	–	–	–	–	
1000 to 2600 Hz	–	140	–	–	–	–	
2600 to 2800 Hz	–	80	–	–	–	–	
Go to Return Crosstalk @0 dBm0							
TxI to TDD @ RxO	–	–	–	−65	–	−65	dBm0
RDD to RxO @ TDD							
Absolute Group Delay @ 1.02 kHz							
TDC = RDC = 2.048 MHz	–	460	–	–	–	–	µs

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = (10-12 V) ±5%, 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	−Tx, +Tx, (TxI for MC14400)	I_{in}		±0.01	±30	nA
AC Input Impedance (1 kHz)	TxI (for MC14400) to V_{AG}	Z_{in}	100	200	–	kΩ
AC Input Impedance (1 kHz)	−Tx, +Tx to V_{AG}	Z_{in}	1.5	5.0	–	MΩ
Input Common Mode Voltage Range V_{DD} = 10.0 V	−Tx, +Tx	V_{ICR}	+1.5	–	+8.0	V
Output Voltage Range RL = 20 k to V_{AG} RL = 600 to V_{AG} RL = 900 to V_{AG}	RxO, $\overline{RxO}$ Each Output	V_{OR} to V_{AG}	−4.0 −3.2 −3.9	– – –	+4.0 +3.2 +3.9	V
Output Current RxO, $\overline{RxO}$	$V_{OH} = V_{DD} - 0.8$ $V_{OL} = 0.8$	–	−5.0 +5.0	– –	– –	mA
Power Supply Rejection Ratio V_{DD} = 12 V ±0.05 V peak @ 1 kHz	RxO to V_{AG} $\overline{RxO}$ to V_{AG}	PSRR	30 30	40 40	– –	dB
Shared External Reference	V_{ref} to V_{AG}		2.0	–	3.8	V
V_{ref} Input Current		I_{in}	–	0.3	–	mA
V_{AG} Output Current	Source	I_{VAG}		200		µA
	Sink	I_{VAG}		8.0		mA

MODE CONTROL LOGIC (V_{SS} = 0 V, 0 to 70°C)

Characteristics		V_{DD} Vdc	Min	Typ	Max	Unit
V_{LS} Voltage for TTL Mode		10 12	0 0	– –	6.0 8.0	V
V_{LS} Voltage for CMOS Mode		10 12	9.5 11.5	– –	– –	V
Mu/A Select Voltage Mu-Law Mode Sign Magnitude Mode A-Law Mode		10 12 10 12 10 12	9.5 11.5 4.0 5.0 – –	– – – – – –	– – 6.0 7.0 0.5 0.5	V
Reference Select Voltage	3.78 V Mode	10 12	9.5 11.5	– –	– –	V
	2.5 V Mode	10 12	4.0 5.0	– –	6.0 7.0	V
	3.15 V Mode	10 12	– –	– –	0.5 0.5	V
V_{ref} Mode Voltage	External Reference Mode	10 12	4.0 5.0	– –	– –	V
	Internal Reference Mode	10 12	– –	– –	0.5 0.5	
Analog Test Mode Selection Frequency, MSI = CCI See Pin Description; Test Modes		10 12	– –	128 128	– –	kHz

SWITCHING CHARACTERISTICS (V_{DD} = (10 to 12 V), T_A = 0 to 70°C, C_L = 50 pF CMOS or TTL Mode)

Characteristic			Symbol	Min	Typ	Max	Unit
Output Rise Time Output Fall Time		TDD	t_{TLH} t_{THL}	–	30	80	ns
Input Rise Time Input Fall Time		DC, TDE, CCI, RCE, RDC, TDC, MSI	t_{TLH} t_{THL}	–	–	4	µs
Pulse Width		DC, TDE Low, CCI, RCE, RDC, TDC, MSI	t_{WH}	100	–	–	ns
Clock Pulse Frequency		DC, TDC, RDC	f_{CL}	64	–	3088	kHz
Clock Pulse Frequency (MSI = 8 kHz) This Pin Will Accept One of These 5 Discrete Clock Frequencies and Compensate to Produce Internal Sequencing.		CCI 1 2 3 4 5	f_{CL1} f_{CL2} f_{CL3} f_{CL4} f_{CL5}	– – – – –	128 1536 1544 2048 2560	– – – – –	kHz
Propagation Delay Time	TTL CMOS TTL CMOS TTL CMOS	TDE to TDD Low Impedance TDE to TDD Low Impedance TDE to TDD High Impedance TDE to TDD High Impedance TDC* to TDD TDC* to TDD	t_{P1} t_{P1} t_{P2} t_{P2} t_{P3} t_{P3}	85 50 – – – –	130 100 50 20 120 80	180 160 75 40 180 160	ns
TDE Rising Edge to TDC Falling Edge Setup Time			t_{su1} t_{su2}	20 100	– –	– –	ns ns
RCE Rising Edge to RDC Falling Edge Setup Time			t_{su3} t_{su4}	20 100	– –	– –	ns ns
MSI Rising Edge to CCI Falling Edge Setup Time			t_{su6} t_{su7}	20 100	– –	– –	ns ns
RDD Valid to RDC Falling Edge Setup Time			t_{su5}	60	40	–	ns
RDD Hold Time from RDC Falling Edge			t_h	100	60	–	ns

*For the sign bit, t_{P3} is measured from TDE or TDC, whichever is last.

PIN DESCRIPTION

DIGITAL

V_{LS} selects CMOS or TTL compatibility for all digital I/Os. $V_{LS} = V_{DD}$; all I/O is CMOS, (V_{DD} to V_{SS} swing). $V_{LS} < V_{DD} - 4$ volts; all I/O is TTL with switchpoint 1.4 V above V_{LS}. The pins controlled by V_{LS} are inputs MSI, CCI, TDC, RDC, TDE, RCE, RDD, $\overline{PDI}$ and output TDD. In TTL applications V_{LS} is Digital GND.

MSI is a continuous 8 kHz (for sampling rate) signal which is used as a time base for internally selecting a prescale divider for CCI input. MSI should be tied to the frame sync or system sync signal, but has no relation to transmit or receive data timing, except as described under TDE. MSI should be derived from the transmit timing in asynchronous applications. In many applications MSI can be tied to TDE. (MSI is tied to TDE in MC14403/05.)

CCI input is designed to accept five discrete clock frequencies. These are 128 kHz 40 to 60% duty cycle, 1.536 MHz, 1.544 MHz, 2.048 MHz or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The four clocks in the MHz frequency range have only minimum pulse width duty cycle requirements. In the asynchronous applications, CCI should be derived from transmit timing. (CCI is tied to TDC in MC14400/01/03).

TDC is the transmit data bit rate input. It can be any frequency from 64 kHz to 3.088 MHz, and is often tied in common to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and leading edges produce successive data bits at TDD. In asynchronous applications, TDE should be derived from this clock. (TDC and RDC are tied together in MC14405 and are called DC.)

TDE serves two functions for the transmit data timing. It establishes the transmit sync in conjunction with MSI. If the leading edges of TDE occur at 8 kHz and both MSI and TDE are derived from TDC, then the MSI relationship is transparent and TDE is simply transmit sync. The leading edge of TDE produces the sign bit at TDD during the current TDC period. The TDC shifts out the remaining bits at the TDC rate. The TDD pin is active as long as TDE is high. If there is more than one TDE leading edge per frame, then the first TDE after MSI is the Tx sync. Thus, TDE may be taken low to three state TDD after the first leading edge. The additional TDE high periods before the next MSI merely un-three-states TDD. This can be used for bit interleaved systems. In asynchronous applications, TDE is derived from TDC.

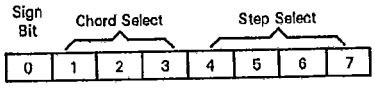
TDD is the digital data output. It operates in sync with TDC and TDE. It is a three-state output. TDC, TDE, and TDD independently control transmit data timing. The data format (Mu-Law, A-Law or sign magnitude) is controlled by Mu/A. This output may be made high-speed CMOS compatible using a pullup resistor.

RDC is the receive data clock and works in conjunction with RCE and RDD to produce all receive data timing. These three signals must be synchronous, but can be asynchronous with all other digital pins. RDC provides the receive register clock. The RDC clock may be any frequency from 64 kHz to 3.088 MHz.

RCE – The rising edge of RCE should identify the sign bit of a receive word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In the asynchronous mode and with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 and 8.5 kHz. Two receive words may be decoded each transmit frame to allow on chip conferencing.

RDD is the digital data input. It operates synchronously with RDC and RCE. The data format is determined by the Mu/A pin.

Code	Sign/ Magnitude	Mu-Law	A-Law (CCITT)
+ full scale	1111 1111	1000 0000	1010 1010
+ zero	1000 0000	1111 1111	1101 0101
− zero	0000 0000	0111 1111	0101 0101
− full scale	0111 1111	0000 0010	0010 1010



Note: Starting from sign magnitude, to change format:
To Mu-Law –
MSB is unchanged (sign)
invert remaining seven bits
if code is 0000 0000, change to 0000 0010 (for zero code suppression)
To A-Law –
MSB is unchanged (sign)
invert odd numbered bits
ignore zero code suppression

Mu/A Select – This pin selects the companding law and the data format at TDD and RDD.

Mu/A = V_{DD}; Mu255 Companding D3 Data Format with Zero Code Supress

Mu/A = V_{AG}; Mu255 Companding with Sign Magnitude Data Format

Mu/A = V_{SS}; A-law Companding with CCITT Data Format Bit Inversions

$\overline{PDI}$ – The power down input disables the bias circuitry and gates off all clock inputs. This puts the TxI, RxO, $\overline{RxO}$, and T_{DD} outputs into a high impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI} = V_{LS}$ or V_{SS}. The circuit operates normally with $\overline{PDI} = V_{DD}$ or with a logic high as defined by connection at V_{LS}. TDD will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

DC – In the MC14405, TDC and RDC are internally connected to this pin.

ANALOG

V_{AG} Analog Ground

Each version of the PCM mono-circuit produces its own analog ground internally. The DC voltage is approximately $(V_{DD} - V_{SS})/2$. All analog functions within the device use this as a reference point for signal processing. In symetric dual supply systems (±5, ±6, etc.), V_{AG} may externally be tied to the system analog ground supply. The V_{AG} output will sink more than 8 mA of current, but can source only 200 µA. When RxO or $\overline{RxO}$ are output drives for 600 or 900 loads tied to V_{AG}, a pullup resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground.

V_{ref} Positive Voltage Reference Input (MC14402 Only)

The V_{ref} pin provides for the supply of an external voltage reference or for the selection of an internal reference within the PCM mono-circuit. If V_{ref} is tied to V_{SS}, the internal reference is selected. If $V_{ref} > V_{AG}$, then the external mode is selected. In each case, the overload or full scale gains of the codec are selected by the reference select pin (RSI). Both the internal and external references are inverted within the PCM mono-circuit for negative input voltage such that only one reference is required.

External Mode – In the external reference mode ($V_{ref} > V_{AG}$), a 2.5 volt reference like the MC1403 is connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref}s and V_{AG}s from different PCM mono-circuits. In special applications, the reference voltage may be between 2 and 4 volts. However, the gain selection logic associated with RSI must be considered to arrive at the desired PCM mono-circuit gain.

Internal Mode – In the internal reference mode ($V_{ref} = V_{SS}$), an internal reference supplies the reference voltage for the PCM mono-circuit.

RSI Reference Select Input (MC14401/02 Only)

The RSI input allows the selection of three different overload or full scale voltages independent of the internal or external reference mode. The selection of maximum signed level is made by connecting RSI to V_{DD}, V_{AG} or V_{SS}. The various modes of operation are summarized in the table below. The internal reference is designed to give internal gains equal to those obtained with an external 2.5 volt reference.

RxO and $\overline{RxO}$ Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak-to-peak signal described with the reference. If a 2.5 V reference is used with RSI tied to V_{AG} and a +3 dBm0 sine wave is decoded, the RxO output will be a 5 V peak-to-peak signal. $\overline{RxO}$ will also have a signal output of 5 V peak-to-peak. External loads may be connected from RxO to $\overline{RxO}$ for a 6 dB push-pull signal gain or from either RxO or $\overline{RxO}$ to V_{AG}. With RSI tied to V_{SS}, each output will drive 600 Ω to +9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to +9 dBm.

ADDITIONAL PIN DESCRIPTIONS

RxG Receive Output Gain Adjust (MC14402 Only)

If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{RxO}$. Thus the push-pull gain to a load from RxO to $\overline{RxO}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{RxO}$ (RG), the gain of $\overline{RxO}$ can be set differently from −1. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{RxO}$ gain is equal to minus RG/RI(VRxO). The purpose of RxG is to allow external receive gain adjustment. The circuit for RxG and $\overline{RxO}$ is shown in the block diagram.

+Tx Positive Tx Amplifier Input (MC14402/03/05 Only)
−Tx Negative Tx Amplifier Input (MC14401/02/03/05 Only)

The TxI pin is the input to the transmit bandpass filter. If +Tx or −Tx are available, then there is an internal amplifier preceding the filter whose pins are +Tx, −Tx and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 k. If +Tx is not available, it is internally tied to V_{AG}. If −Tx and +Tx are not available, the TxI is a unity gain high impedance input.

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Txl Analog Input

Txl is the input to the transmit filter. It is also the output of the transmit gain amplifiers of the MC14401/02/03/05. The input impedance is greater than 100 k to V_{AG} in the MC14400. The Txl input has an internal gain of 1.0, such that a +3 dBm0 signal at Txl corresponds to the peak-to-peak swing of RxO described above. For ±2.5 V shared references and RSI=V_{AG}, the +3 dBm0 input should be 5.0 volt peak-to-peak.

Power Supplies

V_{DD} – Most Positive Supply. V_{DD} is typically 10 to 12 volts.

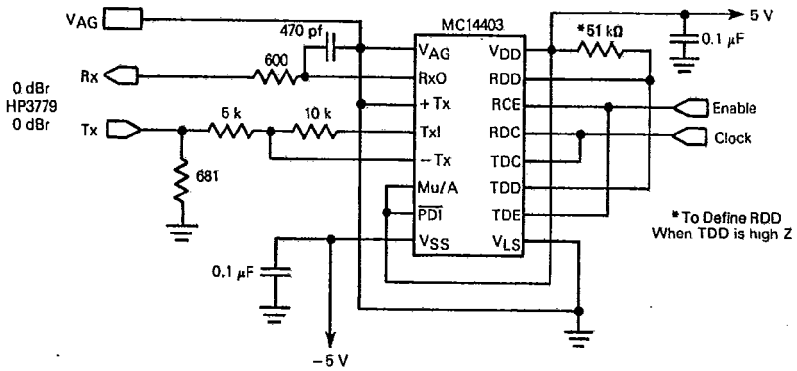
V_{SS} – Most Negative Supply. This is the most negative supply pin.

For single-supply systems, these are the only power pins. V_{LS} will be tied to V_{SS} or V_{DD} and V_{AG} is an output. In dual-supply systems, V_{LS} may be digital ground and V_{AG} may be analog ground.

Testing Considerations (MC14400/01/02 Only)

An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the codec (the output of the Tx filter) is available on the PDI pin. This input is a DC auto zeroed access to the A/D side of the codec. If monitored with a high-impedance buffer, the output of the Tx low-pass filter can also be measured at the PDI pin. This test mode allows independent evaluation of the transmit low-pass filter and A/D side of the codec. The receive channel of the mono-circuit is tested with the codec and filter together.

TEST CIRCUIT



OPTIONS AVAILABLE BY PIN SELECTION

RSI* Pin Level	V_{ref}* Pin Level	Peak-to-Peak Overload Voltage (Txl, RxO)
V_{DD}	V_{SS}	7.56 V_{PP}
V_{DD}	$V_{AG}+V_{EXT}$	(3.02 × V_{EXT}) V_{PP}
V_{AG}	V_{SS}	5 V_{PP}
V_{AG}	$V_{AG}+V_{EXT}$	(2 × V_{EXT}) V_{PP}
V_{SS}	V_{SS}	6.3 V_{PP}
V_{SS}	$V_{AG}+V_{EXT}$	(2.52 × V_{EXT}) V_{PP}

*On MC14400/03/05, RSI and V_{ref} tied internally to V_{SS}.
On MC14401, V_{ref} tied internally to V_{SS}.

SUMMARY OF OPERATION CONDITIONS USER PROGRAMMED THROUGH PINS V_{DD}, V_{AG}, AND V_{SS}

Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu-Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu-Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Levels V_{AG} Up
V_{SS}	A-Law Companding Curve and CCITT Digital Format	3.15	TTL Levels V_{SS} Up

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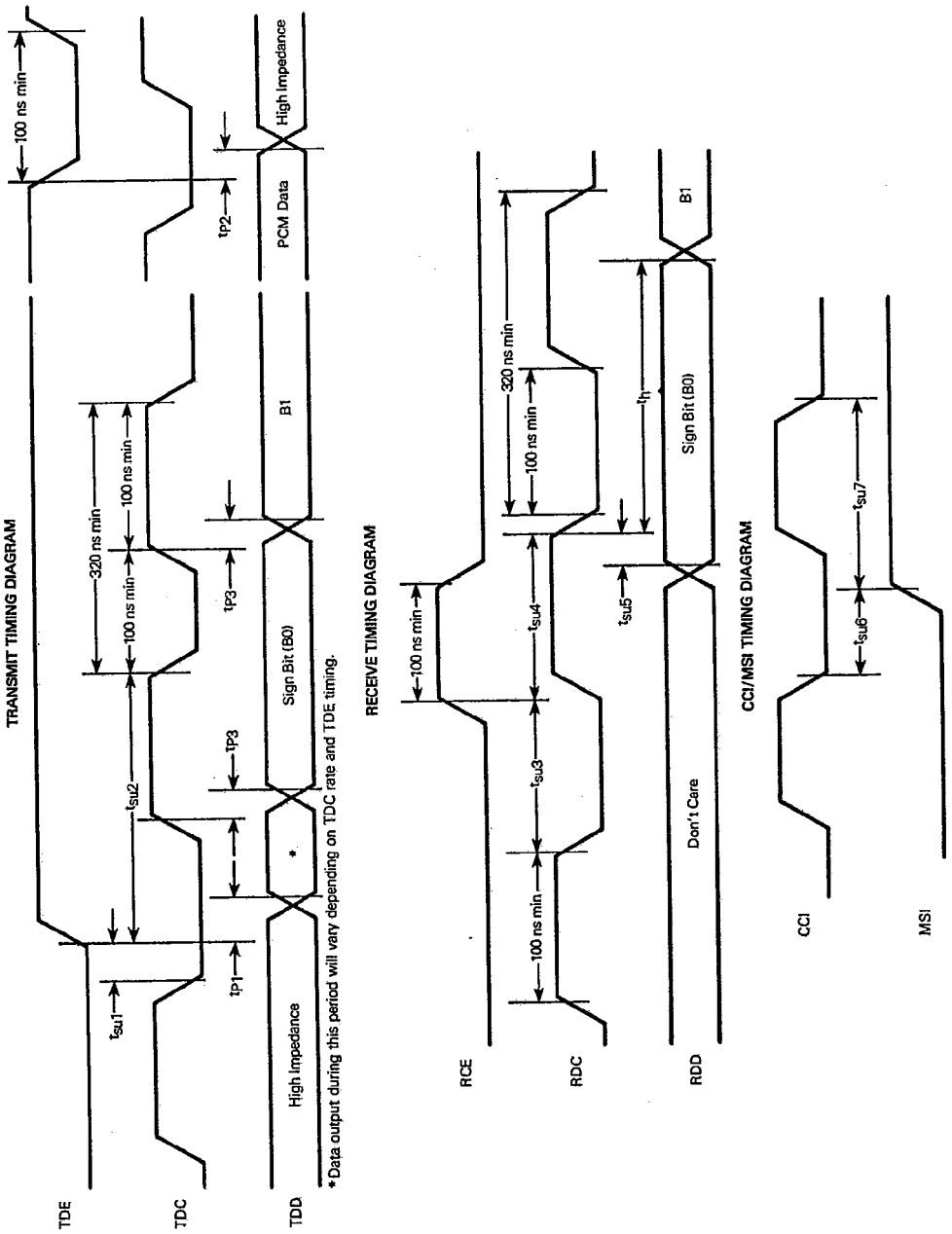

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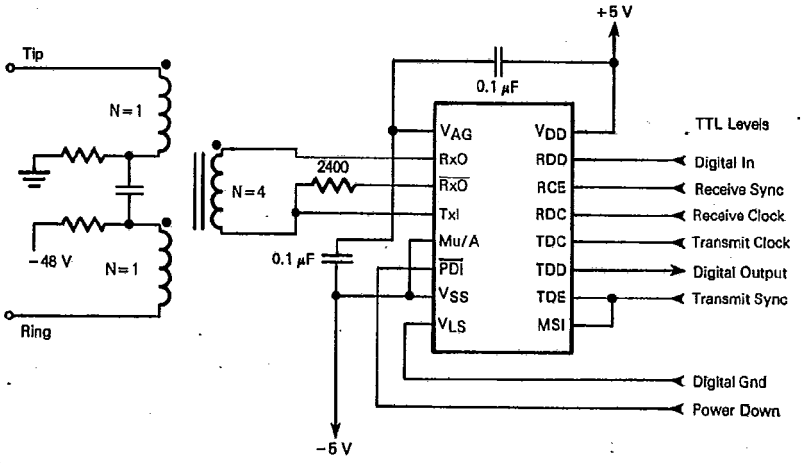
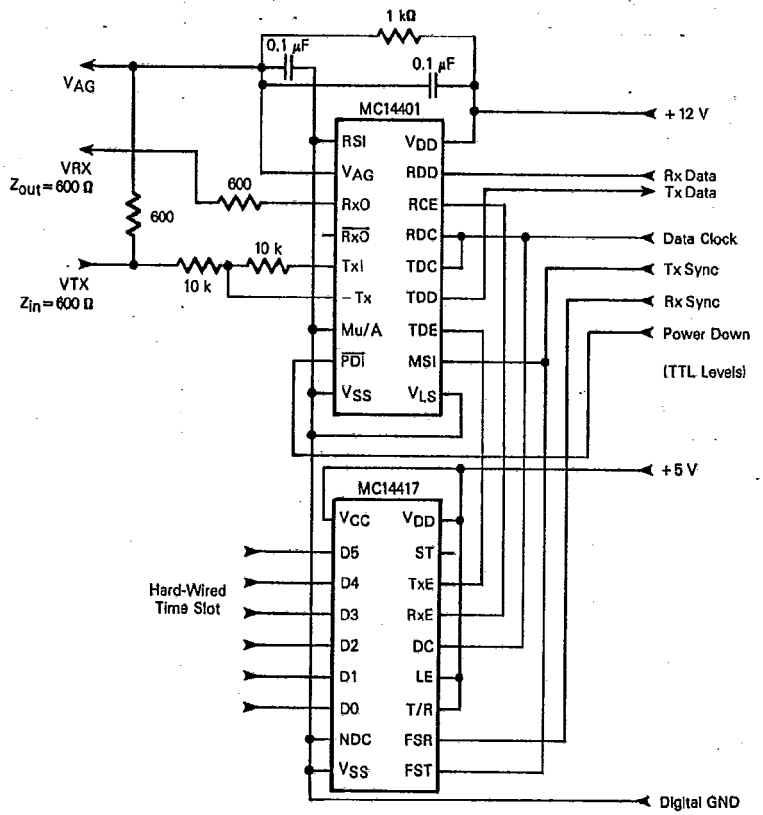
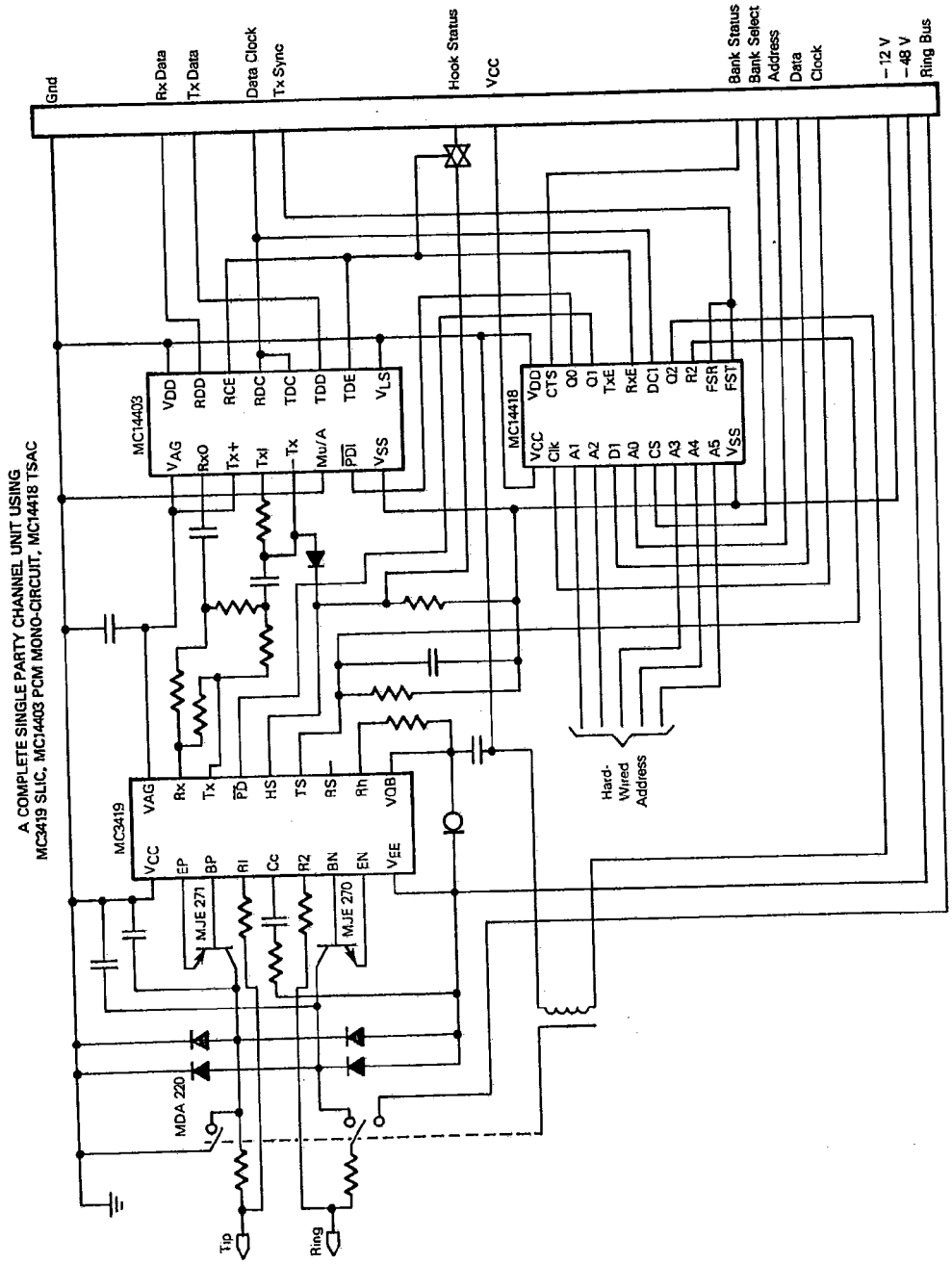
THE BASIC VOICE CHANNEL USING THE MC14400 PCM CODEC/FILTER MONO-CIRCUIT



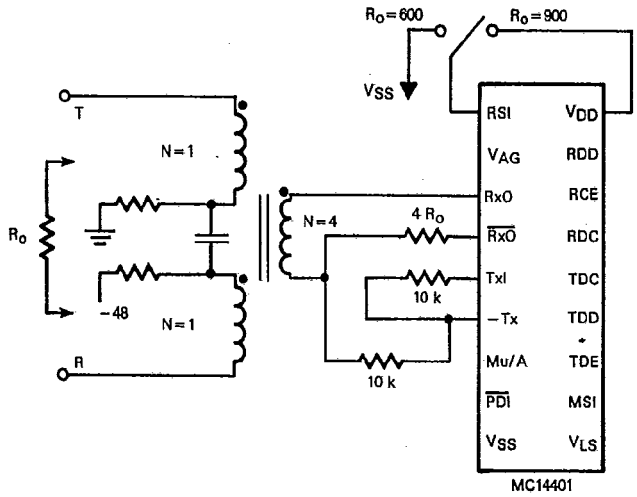
MC14401 PCM MONO-CIRCUIT WITH MC14417 TSAC



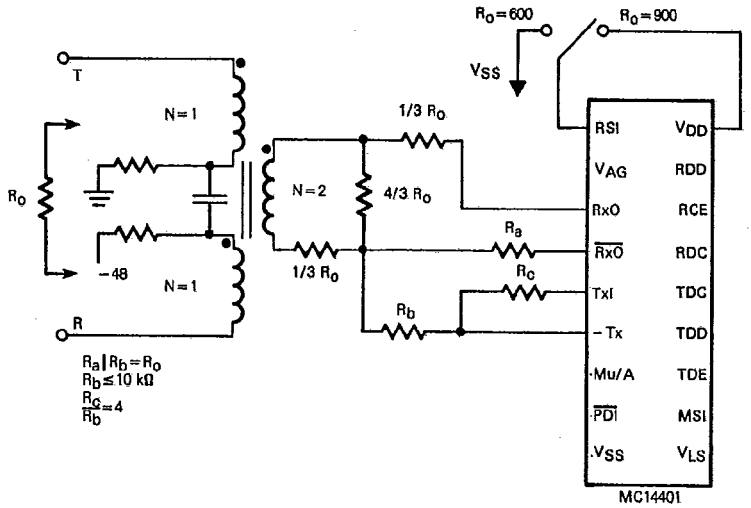


A COMPLETE SINGLE PARTY CHANNEL UNIT USING MC3419 SLIC, MC14403 PCM MONO-CIRCUIT, MC14418 TSAC

HYBRID INTERFACES TO MC14401 PCM CODEC FILTER MONO-CIRCUIT



Simplified Transformer Hybrid Using MC14401



"T" Padded Transformer Hybrid Using MC14401

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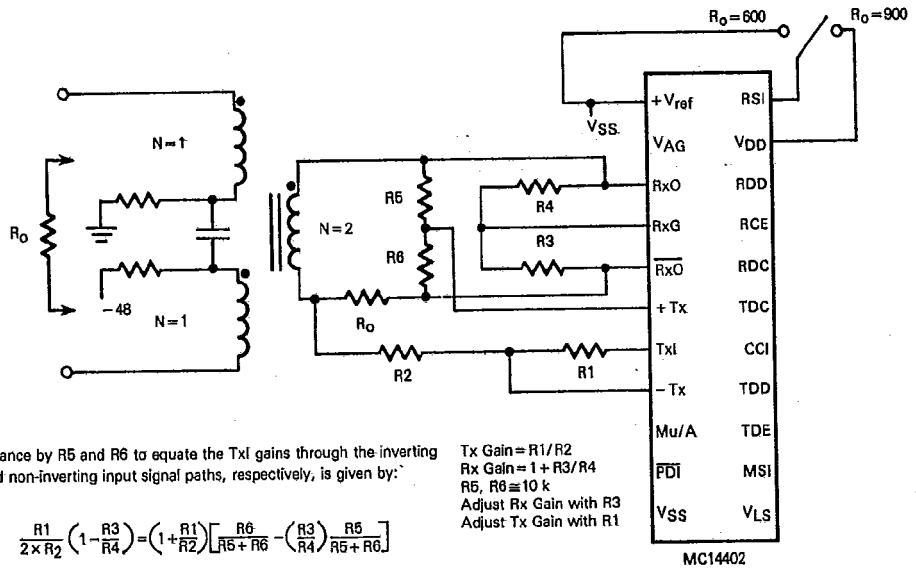
HYBRID INTERFACES TO THE MC14402 PCM CODEC/FILTER MONO-CIRCUIT

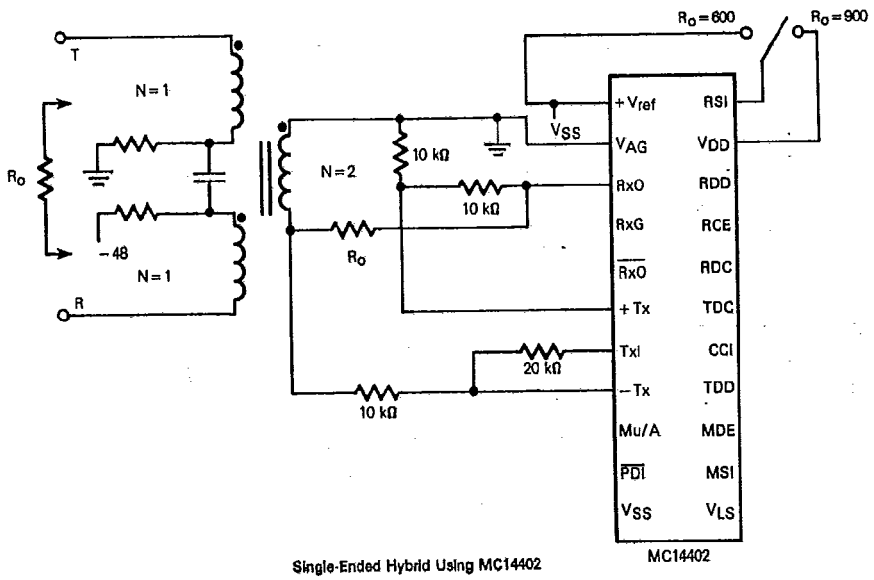


Balance by R5 and R6 to equate the TxI gains through the inverting and non-inverting input signal paths, respectively, is given by:

$$\frac{R1}{2\times R2}\left(1-\frac{R3}{R4}\right)=\left(1+\frac{R1}{R2}\right)\left[\frac{R6}{R5+R6}-\left(\frac{R3}{R4}\right)\frac{R5}{R5+R6}\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≅ 10 k
Adjust Rx Gain with R3
Adjust Tx Gain with R1

Universal Transformer Hybrid Using MC14402



Single-Ended Hybrid Using MC14402

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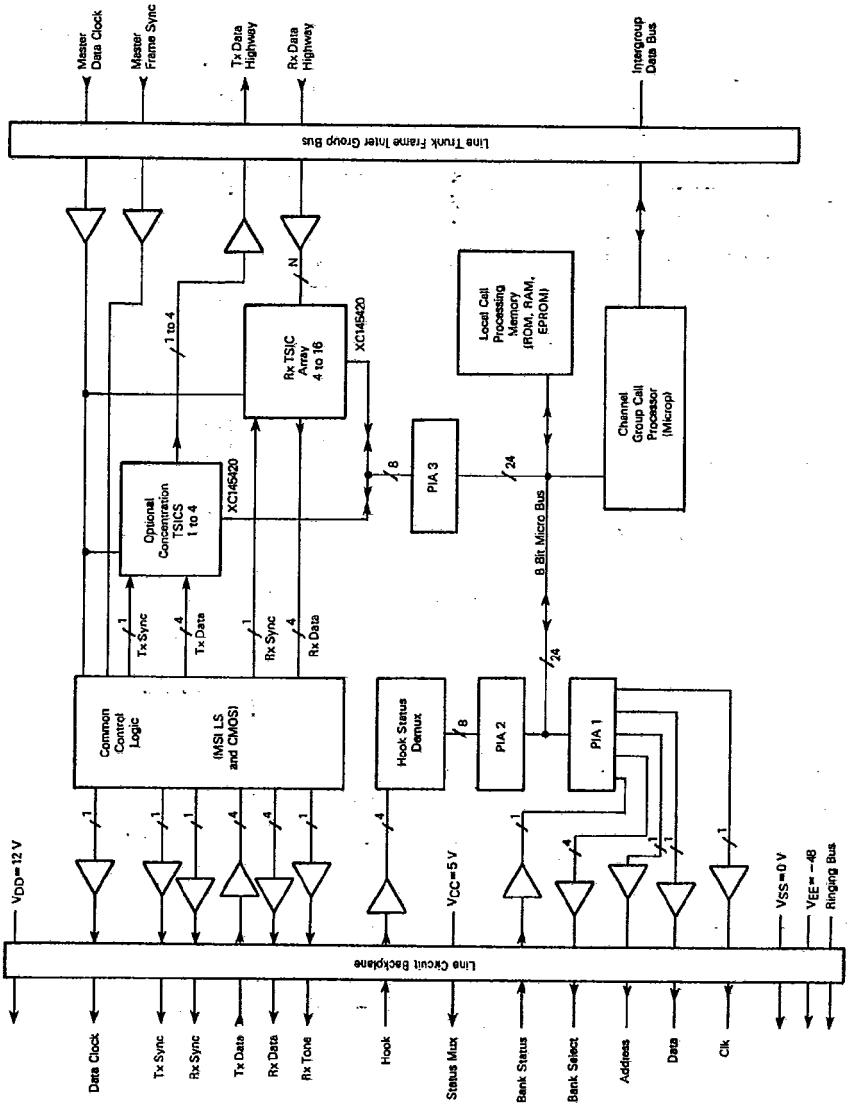

128 CHANNEL GROUP COMMON CONTROL IN A TYPICAL SWITCHING SYSTEM

NOTE: See single party line drawing for line card details.