

Registered Hex ECL/TTL Translator

The MC10/100H605 is a 6-bit, registered, dual supply ECL to TTL translator. The device features differential ECL inputs for both data and clock. The TTL outputs feature balanced 24mA sink/source capabilities for driving transmission lines.

With its differential ECL inputs and TTL outputs the H605 device is ideally suited for the receive function of a HPPI bus type board-to-board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

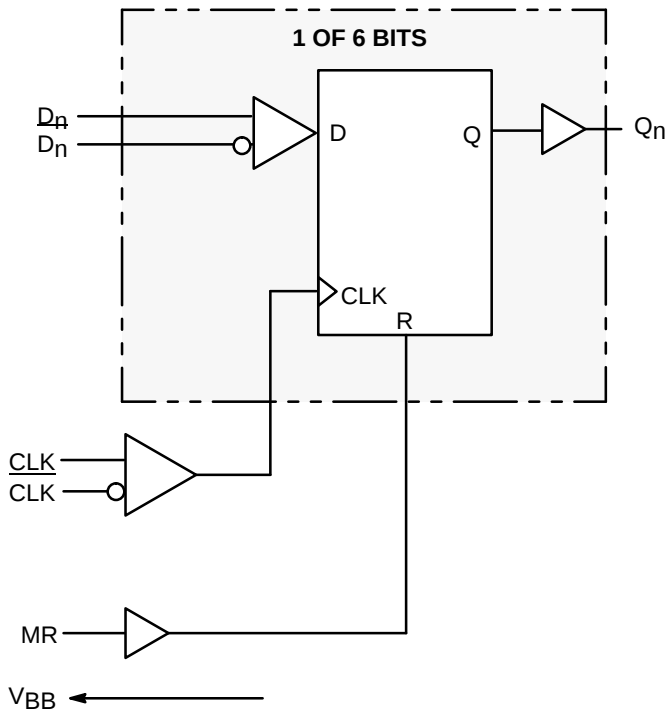
A V_{BB} reference voltage is supplied for use with single-ended data or clock. For single-ended applications the V_{BB} output should be connected to the "bar" inputs ($\overline{D_n}$ or $\overline{CLK}$) and bypassed to ground via a $0.01\mu F$ capacitor. To minimize the skew of the device differential clocks should be used.

The ECL level Master Reset pin is asynchronous and common to all flip-flops. A "HIGH" on the Master Reset forces the Q outputs "LOW".

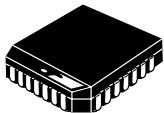
The device is available in either ECL standard: the 10H device is compatible with MECL 10H™ logic levels while the 100H device is compatible with 100K logic levels.

- Differential ECL Data and Clock Inputs
- 24mA Sink, 24mA Source TTL Outputs
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- 2.0ns Part-to-Part Skew

LOGIC SYMBOL



MC10H605 MC100H605



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

PIN NAMES

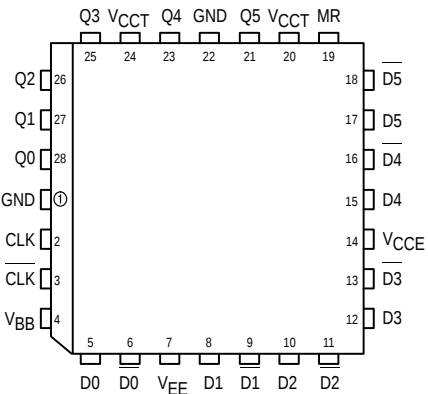
PIN	FUNCTION
$\overline{D_0}$ – $\overline{D_5}$	True ECL Data Inputs
D_0 – D_5	Inverted ECL Data Inputs
$\overline{CLK}$, CLK	Differential ECL Clock Input
MR	ECL Master Reset Input
Q_0 – Q_5	TTL Outputs
V_{CCE}	ECL V_{CC}
V_{CCT}	TTL V_{CC}
GND	TTL Ground
V_{EE}	ECL V_{EE}

TRUTH TABLE

$\overline{D_n}$	MR	$\overline{CLK}/CLK$	Q_{n+1}
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

Pinout: 28-Lead PLCC (Top View)



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10H ECL DC CHARACTERISTICS ($V_{CCT} = +5.0V \pm 5\%$; $V_{EE} = -5.20V \pm 5\%$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Supply Current		63	75		63	75		61	75	mA	
I_{IH}	Input High Current			225			145			145	μA	
I_{IL}	Input Low Current	0.5			0.5			0.5			μA	
V_{IH}	Input High Voltage	-1170		-840	-1130		-810	-1060		-720	mV	
V_{IL}	Input Low Voltage	-1950		-1480	-1950		-1480	-1950		-1480	mV	
V_{BB}	Output Bias Voltage	-1400		-1280	-1370		-1270	-1330		-1210	mV	
V_{Diff}	Input Differential Voltage	150			150			150			mV	
V_{max} CMRR	Input Common Mode Reject Range			0			0			0	mV	
V_{min} CMRR	Input Common Mode Reject Range	-2800 -3000 -3300			-2800 -3000 -3300			-2800 -3000 -3300			mV	$V_{EE} = -4.94$ $V_{EE} = -5.20$ $V_{EE} = -5.46$

100H ECL DC CHARACTERISTICS ($V_{CCT} = +5.0V \pm 5\%$; $V_{EE} = -4.5V \pm 0.3V$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{EE}	Supply Current		65	75		65	75		70	85	mA	
I_{IH}	Input High Current			225			145			145	μA	
I_{IL}	Input Low Current	0.5			0.5			0.5			μA	
V_{IH}	Input High Voltage	-1165		-880	-1165		-880	-1165		-880	mV	
V_{IL}	Input Low Voltage	-1810		-1475	-1810		-1475	-1810		-1475	mV	
V_{BB}	Output Bias Voltage	-1400		-1280	-1400		-1280	-1400		-1200	mV	
V_{Diff}	Input Differential Voltage	150			150			150			mV	
V_{max} CMRR	Input Common Mode Reject Range			0			0			0	mV	
V_{min} CMRR	Input Common Mode Reject Range	-2000 -2200 -2400			-2000 -2200 -2400			-2000 -2200 -2400			mV	$V_{EE} = -4.20$ $V_{EE} = -4.50$ $V_{EE} = -4.80$

* NOTE: DO NOT short the ECL inputs to the TTL V_{CC} .

TTL DC CHARACTERISTICS ($V_{CC} = +5.0V \pm 5\%$; $V_{EE} = -5.2V \pm 5\%$ (10H); $V_{EE} = -4.5V \pm 0.3V$ (100H))

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{CCL}	Supply Current		65	75		65	75		65	75	mA	Outputs Low
I_{CCH}	Supply Current		65	75		65	75		65	75	mA	Outputs High
V_{OL}	Output Low Voltage			0.5			0.5			0.5	mV	$I_{OL} = 24mA$
V_{OH}	Output High Voltage	2.5			2.5			2.5			mV	$I_{OH} = 24mA$
I_{OS}	Output Short Circuit Current	100		225	100		225	100		225	mA	$V_{OUT} = 0V$

AC TEST LIMITS ($V_{CC} = +5.0V \pm 5\%$; $V_{EE} = -5.2V \pm 5\%$ (10H); $V_{EE} = -4.5V \pm 0.3V$ (100H))

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	4.5 4.3	5.3 5.3	6.5 6.7	4.5 4.3	5.4 5.4	6.5 6.7	4.5 4.3	5.6 5.6	6.5 6.7	ns	Across P.S. and Temp $C_L = 50pF$
t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	4.0 3.8	5.0 5.0	6.0 6.2	4.0 3.8	5.1 5.1	6.0 6.2	4.0 3.8	5.5 5.5	6.0 6.2	ns	Across P.S. and Temp $C_L = 50pF$
t_{PHL}	Propagation Delay MR to Q	2.5	4.9	7.0	2.5	5.2	7.0	3.0	5.8	7.5	ns	Across P.S. and Temp $C_L = 50pF$
t_{SKEW}	Device Skew Part-to-Part (Diff) Within-Device		1.0 0.3	2.0 0.7		1.0 0.3	2.0 0.7		1.0 0.3	2.0 0.7	ns	$C_L = 50pF$
t_S	Setup Time	1.5			1.5			1.5			ns	
t_H	Hold Time	1.5			1.5			1.5			ns	
t_{PW}	Minimum Pulse Width CLK	1.0			1.0			1.0			ns	
t_{PW}	Minimum Pulse Width MR	1.0			1.0			1.0			ns	
V_{PP}	Minimum Input Swing	150			150			150			mV	Peak-to-Peak
t_r	Rise Time	0.7	1.0	1.5	0.7	1.0	1.5	0.7	1.0	1.5	ns	1V to 2V
t_f	Fall Time	0.5	0.7	1.2	0.5	0.7	1.2	0.5	0.7	1.2	ns	1V to 2V
t_{RR}	Reset/Recovery Time	2.5			2.5			2.5			ns	

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