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MC10321

Specifications and Applications Information

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

The MC10321 is a 7-bit high speed parallel flash A/D converter, which employs an internal Grey Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 volt supply, and a negative supply between −3.0 and −6.0 volts. Three-state TTL outputs allow direct connection to a data bus or common I/O memory.

The MC10321 contains 128 parallel comparators wired along a precision input reference network. The comparator outputs are fed to latches, and then to an encoder network which produces a 7-bit data byte, plus an overrange bit. The data is latched and converted to three-state LSTTL levels. Enable inputs permit setting the outputs to a three-state condition. The overrange bit is always active to allow for sensing of the overrange condition, and to ease the interconnection of two MC10321s into an 8-bit configuration.

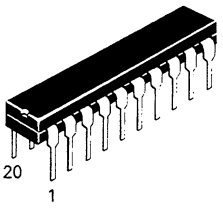
The MC10321 is available in a 20-pin standard plastic and SOIC packages.

Applications include Video displays (digital TV, picture-in-picture, special effects), radar processing, high speed instrumentation, and TV broadcast.

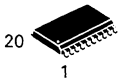
- Internal Grey Code for Speed and Accuracy
- 25 MHz Sampling Rate
- 7-Bit Resolution with 8-Bit Accuracy
- Easily Cascadable into an 8-Bit System
- Three-State LSTTL Outputs with True and Complement Enable Inputs
- Low Input Capacitance: 25 pF
- No Clock Kick-Out Currents on Input or Reference
- Wide Input Range: 1.0–2.1 Volts within a ± 2.1 Volt Range
- No Sample and Hold Required for Video Applications
- Edge Triggered Conversion — No Pipeline Delay
- True and Complement Enable Inputs for Three-State Control
- Standard DIP and Surface Mount Packages Available
- Operating Temperature Range: −40° to +85°C

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



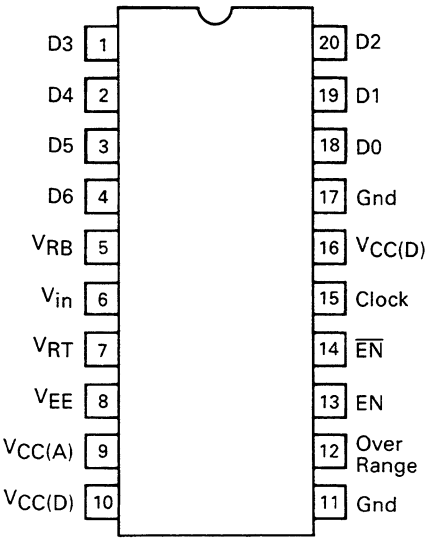
P SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03
SO-20

PIN CONNECTIONS

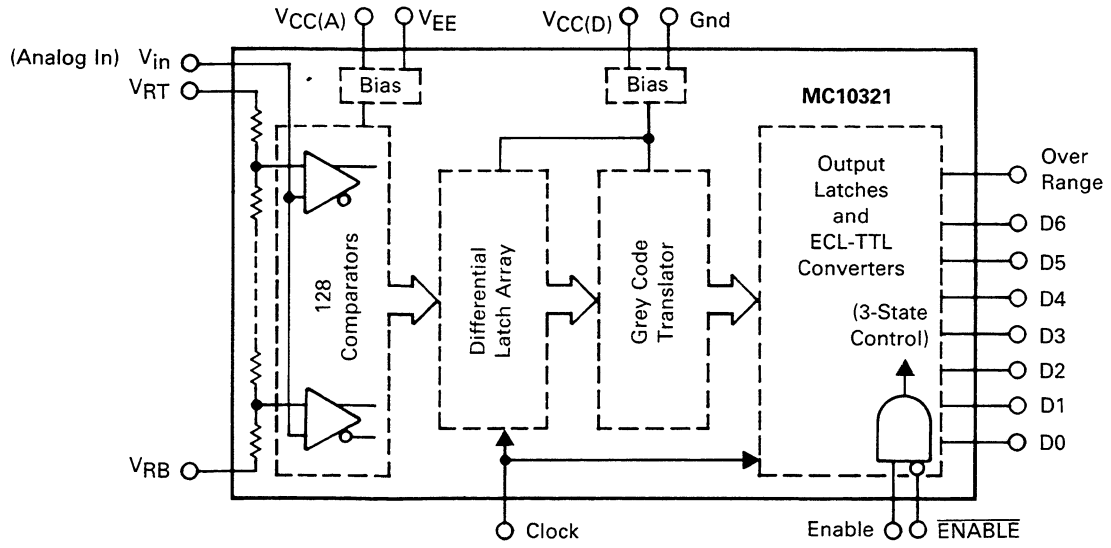
(Top View)



ORDERING INFORMATION

Device	Temperature Range	Package
MC10321P	−40° to +85°C	Plastic DIP
MC10321DW		SO-20

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Supply Voltage	$V_{CC(A)}$, $V_{CC(D)}$ V_{EE}	+7.0 −7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}-V_{CC(A)}$	−0.3, +0.3	Vdc
Digital Input Voltage (Pins 13–15)	$V_{I(D)}$	−0.5, +7.0	Vdc
Analog Input Voltage (Pins 5, 6, 7)	$V_{I(A)}$	−2.5, +2.5	Vdc
Reference Voltage Span (Pin 7–Pin 5)	—	+2.3	Vdc
Applied Output Voltage (D0–D6 in 3-State)	—	−0.3, +7.0	Vdc
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage (Pin 9) Power Supply Voltage (Pins 10, 16) $V_{CC(D)}-V_{CC(A)}$	$V_{CC(A)}$ $V_{CC(D)}$ ΔV_{CC}	+4.5 +4.5 −0.1	+5.0 +5.0 0	+5.5 +5.5 +0.1	Vdc
Power Supply Voltage (Pin 8)	V_{EE}	−6.0	−5.0	−3.0	Vdc
Digital Input Voltages (Pins 13–15)	—	0	—	$V_{CC(D)}$	Vdc
Analog Input (Pin 6)	V_{in}	−2.1	—	+2.1	Vdc
Voltage @ V_{RT} (Pin 7) @ V_{RB} (Pin 5) $V_{RT}-V_{RB}$ $V_{RB}-V_{EE}$	V_{RT} V_{RB} ΔV_R —	−1.0 −2.1 +1.0 1.3	— — — —	+2.1 +1.0 +2.1 —	Vdc
Applied Output Voltage (Pins D0–D6 in 3-State)	V_O	0	—	$V_{CC(D)}$	Vdc
Clock Pulse Width — High — Low	t_{CKH} t_{CKL}	5.0 15	— —	— —	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	−40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, except where noted)

Characteristic	Symbol	Min	Typ	Max	Units
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	—	—	7.0	Bits
Monotonicity	MON		Guaranteed		Bits
Integral Nonlinearity Differential Nonlinearity	INL DNL	— —	±1/4 —	±1.0 ±1.0	LSB
Differential Phase (See Figure 11) Differential Gain (See Figure 11)	DP DG	— —	2.0 2.0	— —	Deg. %
Power Supply Rejection Ratio (4.5 V < V_{CC} < 5.5 V, V_{EE} = −5.2 V) (−6.0 V < V_{EE} < −3.0 V, V_{CC} = +5.0 V)	PSRR	 — —	 0.02 0	 — —	LSB/V
ANALOG INPUT (Pin 6)					
Input Current @ V_{in} = V_{RB} − 0.1 V (See Figure 4) @ V_{in} = V_{RT} + 0.1 V (See Figure 4)	I_{INL} I_{INH}	— —	+1.0 +60	+5.0 +80	μA
Input Capacitance (1.0 V < (V_{RT} − V_{RB}) < 2.0 V)	C_{in}	—	22	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	100	140	175	Ω
Temperature Coefficient	T_C	—	+0.29	—	%/°C
Ladder Capacitance (Pin 1 Open)	C_{ref}	—	5.0	—	pF
ENABLE INPUTS (V_{CC} = 5.5 V)					
Input Voltage — High — Low	V_{IHE} V_{ILE}	2.0 —	— —	— 0.8	V
Input Current @ 2.4 Volts (See Figure 5) @ 0.4 Volts (See Figure 5)	I_{IHE} I_{ILE}	— −200	+0.2 −120	2.0 —	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKE}	−1.5	−1.3	—	V
CLOCK INPUT (V_{CC} = 5.5 V)					
Input Voltage — High — Low	V_{IHC} V_{ILC}	2.0 —	— —	— 0.8	Vdc
Input Current @ 0.4 V (See Figure 6) @ 2.7 V (See Figure 6)	I_{ILC} I_{IHC}	−150 −80	−80 −40	— —	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKC}	−1.5	−1.3	—	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = −400 μA @ D6–D0, OR, V_{CC} = 4.5 V, See Figure 7)	V_{OH}	2.4	3.0	—	V
Low Output Voltage (I_{OL} = 4.0 mA @ D6–D0, OR, V_{CC} = 4.5 V, See Figure 8)	V_{OL}	—	0.3	0.4	V
Output Short Circuit Current* (D6–D0, OR, V_{CC} = 5.5 V)	I_{SC}	—	−35	—	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0–D6 in 3-State Mode)	I_{LK}	−10	—	+10	μA
Output Capacitance (D0–D6 in 3-State Mode)	C_{out}	—	5.0	—	pF

*Only one output to be shorted at a time, not to exceed 1 second.

POWER SUPPLIES

$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V, Outputs Unloaded) $V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V, Outputs Unloaded) V_{EE} Current (−6.0 V < V_{EE} < −3.0 V)	$I_{CC(A)}$ $I_{CC(D)}$ I_{EE}	10 40 −16	13 60 −13	16 80 −8.0	mA
Power Dissipation (V_{RT} − V_{RB} = 2.0 V, Outputs Unloaded)	P_D	—	459	668	mW

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, See System Timing Diagram)

Parameter	Symbol	Min	Typ	Max	Units
INPUTS					
Min Clock Pulse Width — High — Low	t_{CKH} t_{CKL}	— —	5.0 15	— —	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	22	—	ns
Aperture Delay	t_{AD}	—	3.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	22	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	17	—	ns
Data High to 3-State from $\overline{\text{ENABLE}}$ High*	$t_{E'HZ}$	—	27	—	ns
Data Low to 3-State from $\overline{\text{ENABLE}}$ High*	$t_{E'LZ}$	—	19	—	ns
Valid Data from Enable High (Pin 14 = 0 V)*	t_{EDV}	—	13	—	ns
Valid Data from $\overline{\text{ENABLE}}$ Low (Pin 13 = 5.0 V)*	$t_{E'DV}$	—	20	—	ns
Output Transition Time (10%–90%)*	t_{tr}	—	6.0	—	ns

*See Figure 2 for output loading.

TEMPERATURE CHARACTERISTICS

Parameter	Typical Value @ 25°C	Typical Change −40 to +85°C
I_{CC} (+5.0 V Supply Current)	73 mA	−100 μA/°C
I_{EE} (−5.2 V Supply Current)	−13 mA	+7.0 μA/°C
Ladder Resistance	140 Ω	+0.29%/°C
V_{OL} (Output Low Voltage @ 4.0 mA)	0.3 V	+8.0 μV/°C
V_{OH} (Output High Voltage @ −400 μA)	3.0 V	2.1 mV/°C
Differential Nonlinearity	—	−0.0008 LSB/°C
Integral Nonlinearity	0.25 LSB	−0.001 LSB/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
GND	11,17	Power supply ground. The two pins should be connected directly together, and through a low impedance path to the power supply.
OR	12	Overrange output. Indicates V_{in} is more positive than V_{RT}-1/2 LSB. This output does not have 3-state capability, and therefore is always active.
D6–D0	1–4, 18–20	Digital Outputs. D6 (Pin 4) is the MSB, D0 (Pin 18) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	10,16	Power supply for the digital section. +5.0 V, ±10% required.
V_{EE}	8	Negative Power supply. Nominally −5.2 V, it can range from −3.0 to −6.0 V, and must be more negative than V_{RB} by >1.3 V.
V_{in}	6	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33 kΩ (See Figure 4) in parallel with 22 pF.

PIN DESCRIPTIONS

Symbol	Pin	Description
$V_{CC(A)}$	9	Power supply for the analog section. +5.0 V, ±10% required.
CLK	15	Clock input, TTL compatible, and can range from dc to 25 MHz. Conversion occurs on the negative edge of the clock.
EN	13	Enable input. TTL compatible, a Logic "1" (and Pin 14 a Logic "0") enables the data outputs. A Logic "0" sets the outputs (except Overrange) to a 3-state mode.
$\overline{\text{EN}}$	14	$\overline{\text{ENABLE}}$ input. TTL compatible, a Logic "0" (and Pin 13 a Logic "1") enables the data outputs. A Logic "1" sets the outputs (except Overrange) to a 3-state mode.
V_{RB}	5	The bottom (most negative point) of the internal reference resistor ladder. The ladder resistance is typically 140 Ω to V_{RT}.
V_{RT}	7	The top (most positive point) of the internal reference resistor ladder.

Pin assignments are the same for the standard DIP package and the surface mount package.

FIGURE 1 — SYSTEM TIMING DIAGRAM

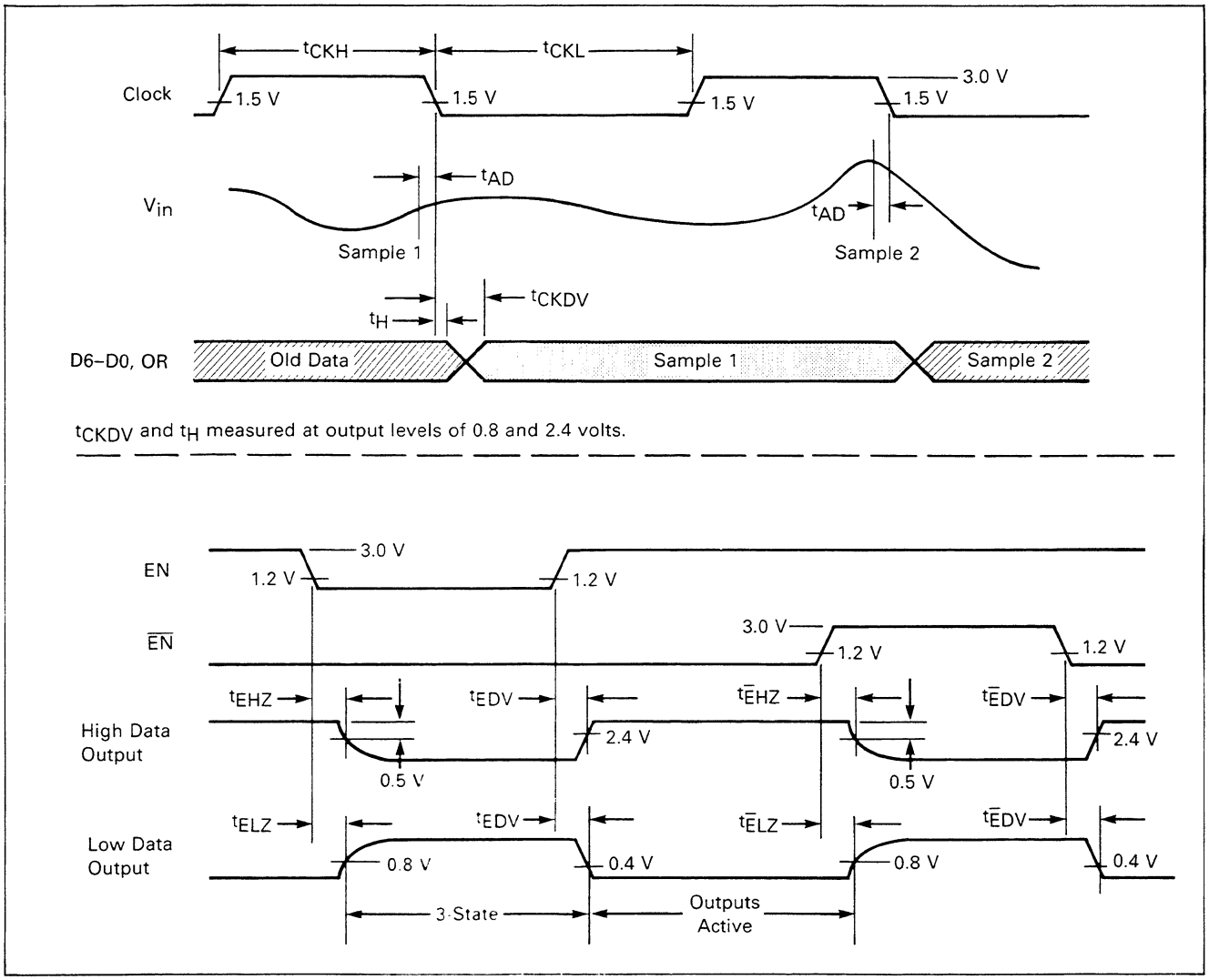


FIGURE 2 — DATA OUTPUT TEST CIRCUIT

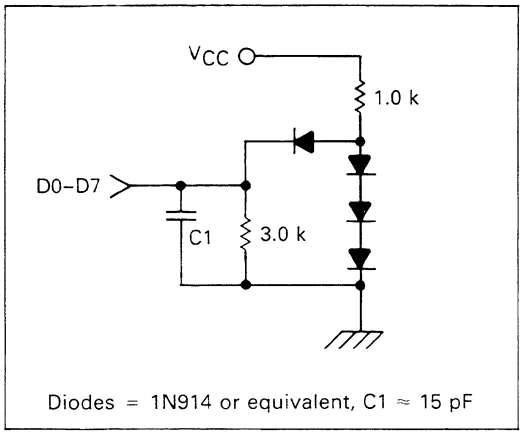


FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

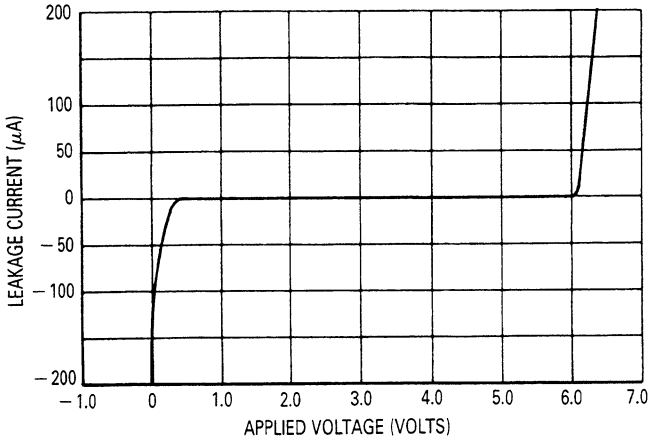


FIGURE 4 — INPUT CURRENT @ V_{in}

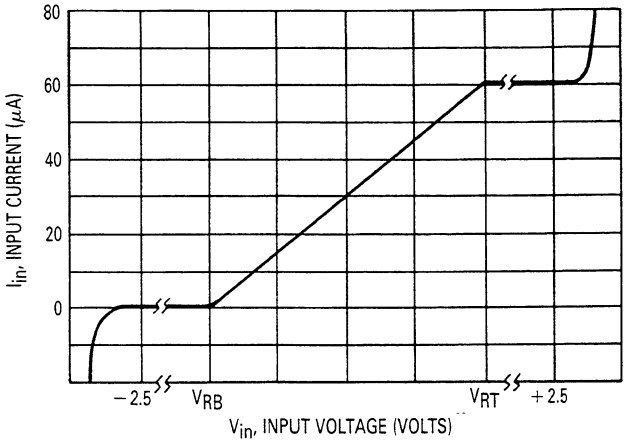


FIGURE 5 — INPUT CURRENT AT ENABLE, $\overline{\text{ENABLE}}$

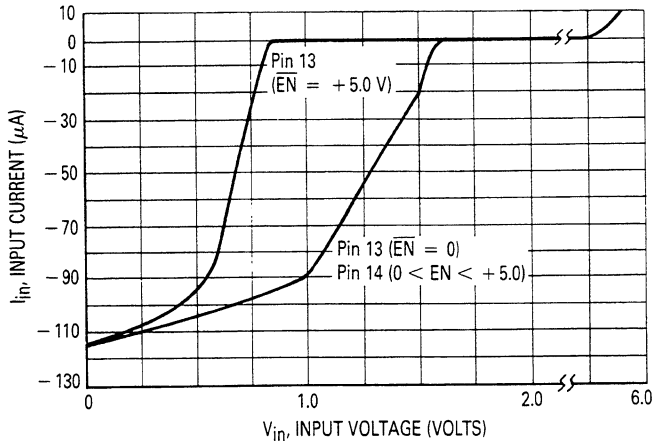


FIGURE 6 — CLOCK INPUT CURRENT

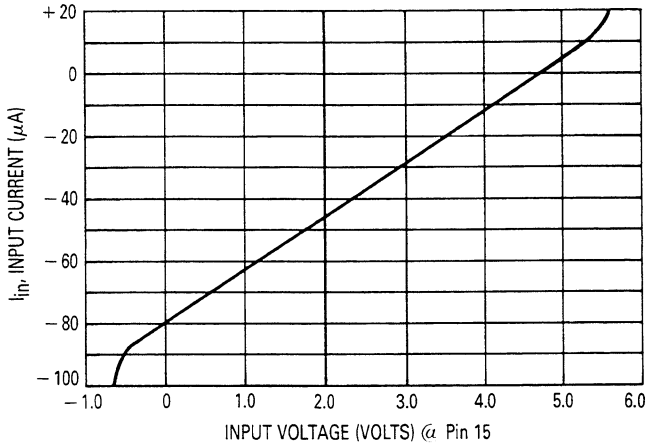


FIGURE 7 — OUTPUT VOLTAGE versus OUTPUT CURRENT

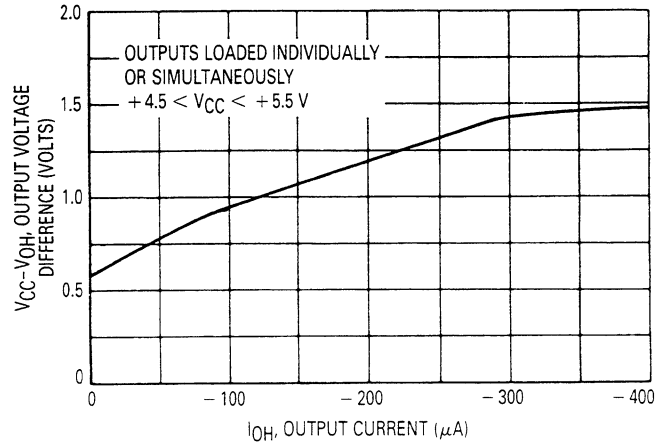


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

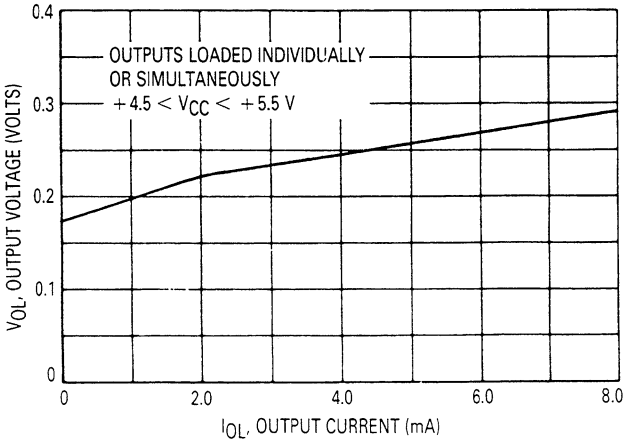


FIGURE 9 — INTEGRAL LINEARITY ERROR IN LSBs versus CODE

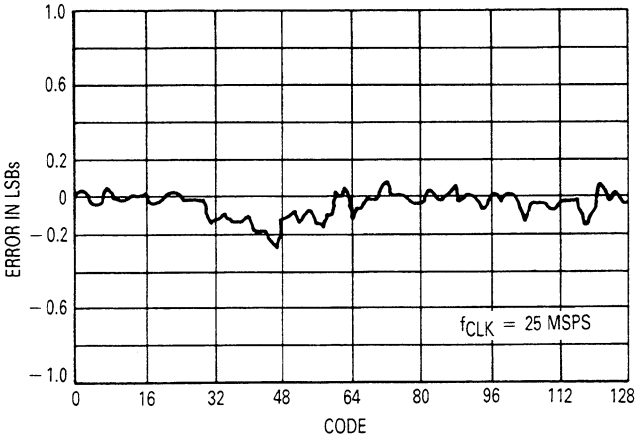
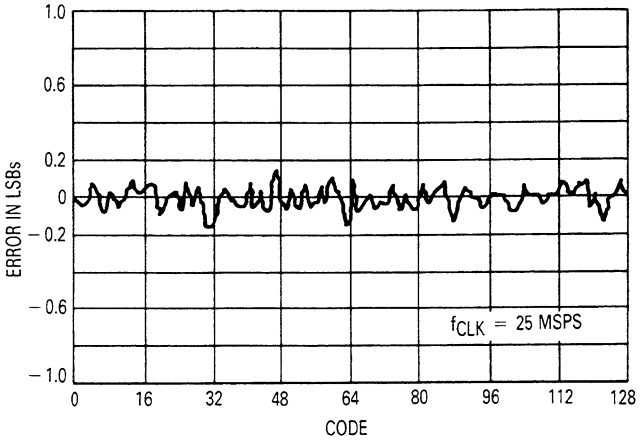


FIGURE 10 — DIFFERENTIAL LINEARITY ERROR IN LSBs versus LOWER CODE



DESIGN GUIDELINES

INTRODUCTION

The MC10321 is a high speed, 7-bit parallel ("Flash") type Analog-to-Digital converter containing 128 comparators at the front end. See Figure 12 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of each of the comparators is connected to the input signal (V_{in}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to a 7-bit Grey code by the Differential Latch Array. The Grey code ensures that errors caused at the input stage, due to cross talk, feed-thru, or timing disparaties, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to a 7-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. ENABLE inputs (EN and $\overline{EN}$) at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

ANALOG SECTION

SIGNAL INPUT

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 128 comparators through Pin 6. The other inputs of the comparators are connected to 128 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal to the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 6 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 μA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 4). However, V_{in} must be maintained within the absolute range of ±2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 6.

The input capacitance at Pin 6 is typically 22 pF, and is constant as V_{in} varies from V_{RT} to V_{RB}.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 128 equally spaced voltages for the comparators (see Figure 12 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and the 128th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 140 Ω, ±25%, requiring 14.3 mA @ 2.0 volts and 7.14 mA @ 1.0 volt. There is a nominal warm up change of ≈ +8.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span [$V_{RT} - V_{RB}$] is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of −2.1 to +2.1 volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversely with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level

applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤2.1 volts.

POWER SUPPLIES

$V_{CC(A)}$ (Pin 9) is the positive power supply for the comparators, and $V_{CC(D)}$ (Pins 10, 16) is the positive power supply for the digital portion. Both are to be +5.0 volts, ±10%, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10321 to the failed supply.

$I_{CC(A)}$ is nominally 13 mA, and does not vary with clock frequency or with V_{in}, but does vary slightly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 60 mA, and is independent of clock frequency. It does vary, however, by 4–5 mA as V_{in} is varied from V_{RT} to V_{RB}, and varies directly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range −3.0 to −6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB}. I_{EE} is a nominal −13 mA, and is independent of clock frequency, V_{in} and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC.** A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input (Pin 15) is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitation, but the minimum low and high times must be adhered to. See Figure 6 for the input current requirements.

The conversion sequence is shown in Figure 13, and is as follows:

— On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).

— During the high time, the comparators track the input signal. The data output latches retain the old data.

— On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data in ≈22 ns.

— During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge. The minimum amount of time the data must be present prior to the clock falling edge (aperture delay) is 2.0–6.0 ns, typically 3.0 ns.

The comparator output latches provide the circuit with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs (Pins 13, 14) are TTL compatible, and are used to change the data outputs (D6–D0) from active to 3-state. This capability allows cascading two MC10321s into an 8-bit configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 13 must be Logic "1," and Pin 14 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. Both pins have a nominal threshold of ≈1.2 volts, their input currents are shown in Figure 5, and their input-output timing is shown in Figure 1 and 14. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overrange output (Pin 12) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs (Pins 1–4, 12, 18–20) are TTL level outputs with high impedance capability (except Overrange). Pin 4 is the MSB (D6), and Pin 18 is the LSB (D0). The seven outputs are active as long as the Enable inputs are true (EN = high, $\overline{EN}$ = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 14. Figures 7 and 8 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in Table 1.

The Overrange output (Pin 12) goes high when the input, V_{in}, is more positive than V_{RT} − 1/2 LSB. This output is always active — it does not have high impedance capability. Besides used to indicate an input overrange, it is additionally used for cascading two MC10321s to form an 8-bit A/D converter (see Figure 21).

TABLE 1

Input	V_{RT}, V_{RB} (Volts)			Output Code	Overrange
	2.048, 0	+1.0 V, −1.0 V	+1.0 V, 0 V		
$>V_{RT}$ − 1/2 LSB	>2.040 V	>0.9922 V	>0.9961 V	$7F_H$	1
V_{RT} − 1/2 LSB	2.040 V	0.9922 V	0.9961 V	$7F_H$	0 ↔ 1
V_{RT} − 1 LSB	2.032 V	0.9844 V	0.9922 V	$7F_H$	0
V_{RT} − 1 1/2 LSB	2.024 V	0.9766 V	0.9883 V	$7E_H \leftrightarrow 7F_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	40_H	0
V_{RB} + 1/2 LSB	8.0 mV	−0.9922 V	3.9 mV	$00_H \leftrightarrow 01_H$	0
$< V_{RB}$ + 1/2 LSB	<8.0 mV	< −0.9922 V	<3.9 mV	00_H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10321 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10321.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10321 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10321 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10321.

The two ground pins (11, 17) must be connected directly together. Any long path between them can cause stability problems due to the inductance (@ 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2.0 volts, then 1/2 LSB is only 7.8 millivolts, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of −40 to +85°C, a maximum temperature coefficient of 31 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (up to 500 mV) present on the supplies and on their ground lines. Generally ±15 volts, or ±12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 15 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 20 mA @ 2.0 volts). The MC1403 series of references have very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 15, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 15, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 16 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 17 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 15 and 16, and have similar accuracy and stability. The MC1403 reference is used in conjunction with an op amp configured as an inverter, providing the negative voltage. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10321 is suitable for digitizing video signals directly without signal conditioning, although the standard 1.0 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 18 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 19 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈225 ns at the base. Figure 20 shows an application circuit for digitizing video.

8-BIT A/D CONVERTER

Figure 21 shows how two MC10321s can be connected to form an 8-bit converter. In this configuration, the outputs (D6–D0) of the two 7-bit converters are paralleled. The outputs of one device are active, while the outputs of other are in the 3-state mode. The selection is made by the OVERRANGE output of the lower MC10321, which controls Enable inputs on the two devices. Additionally, this output provides the 8th bit.

The reference ladders are connected in series, providing the 256 steps required for 8 bits. The input voltage range is determined by V_{RT} of the upper MC10321, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10321s may not be identical in value. Without the adjustment, a nonequal voltage division could occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ±1.0 volt or ±2.0 volts), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application. If latches are required, SN74LS173As are recommended.

50 MHz, 7 BIT A/D CONVERTER

Figure 22 shows how two MC10321s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the SELECT input to the MC74F257 multiplexers to alternately select the outputs of the two converters. A brief timing diagram is shown in the figure.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −3.0 to −6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 23 can be used to generate −5.0 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC10321. The MC34063 is a switching regulator, and in Figure 23 is configured in an inverting mode of operation. The regulator operating specifications are given in the figure.

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −1.0 to +1.0 V, −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of a 7-bit A/D) of the 40_H to 41_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A/D set up for a symmetrical bipolar input (e.g., −1.0 to +1.0 V).

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ±1 LSB for proper operation.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as **reflected binary code,** it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningfull. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 - A_1 2^1 - A_0 2^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes corresponds to a zero input voltage of an A/D, and all ones corresponds to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative input voltage (of an A/D), while all ones corresponds to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converters performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of $\pm 1/2$ LSB.

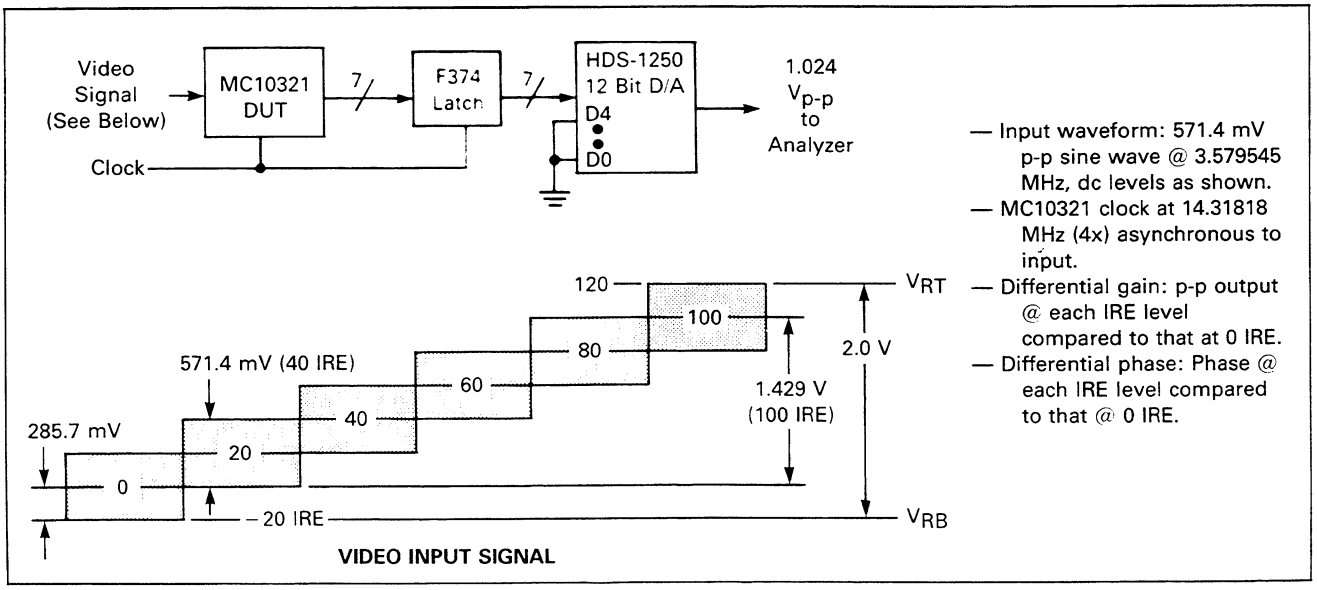
RESOLUTION — The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A/D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +2.0 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

FIGURE 11 — DIFFERENTIAL PHASE AND GAIN TEST



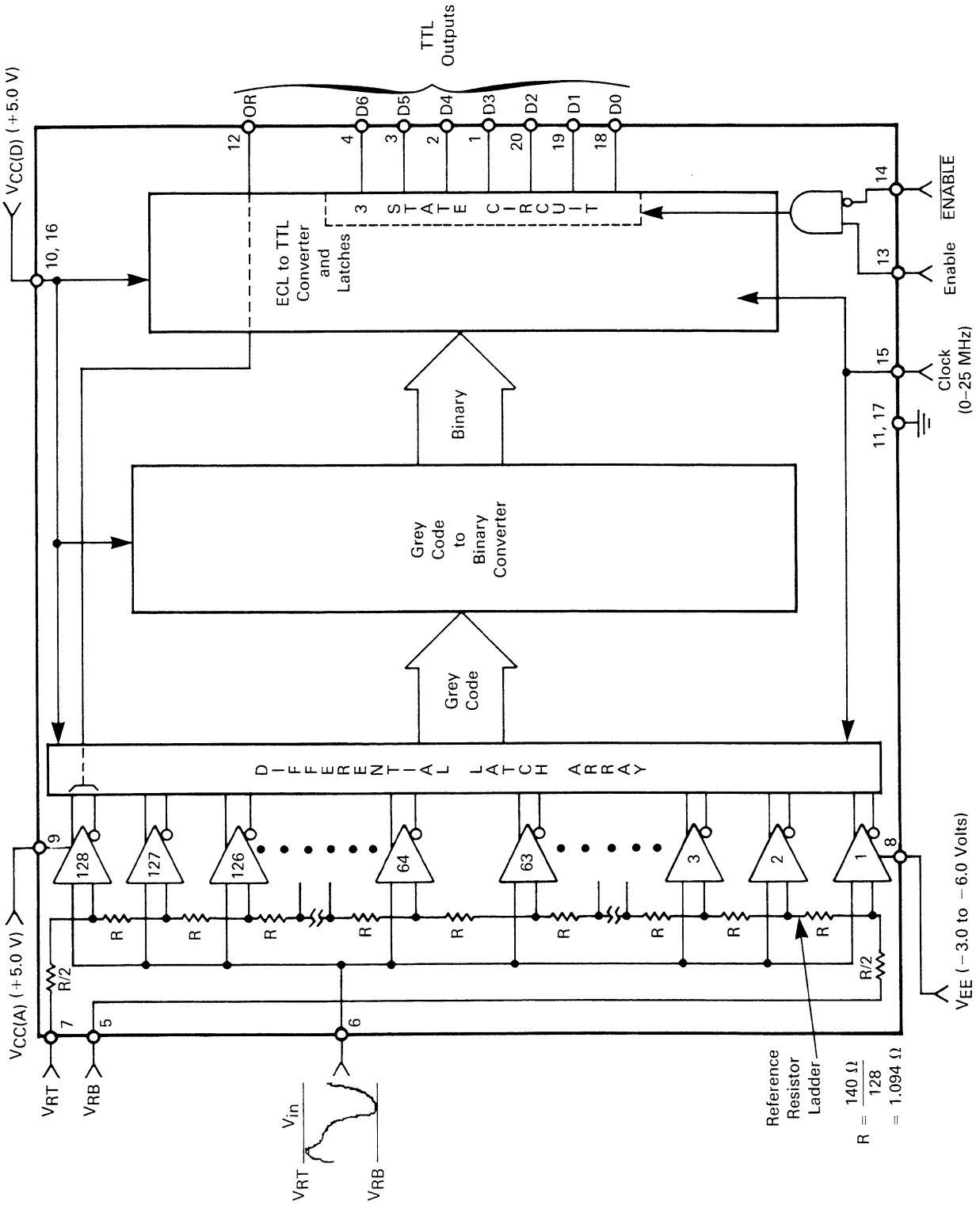


FIGURE 12 — MC10321

FIGURE 13 — CONVERSION SEQUENCE

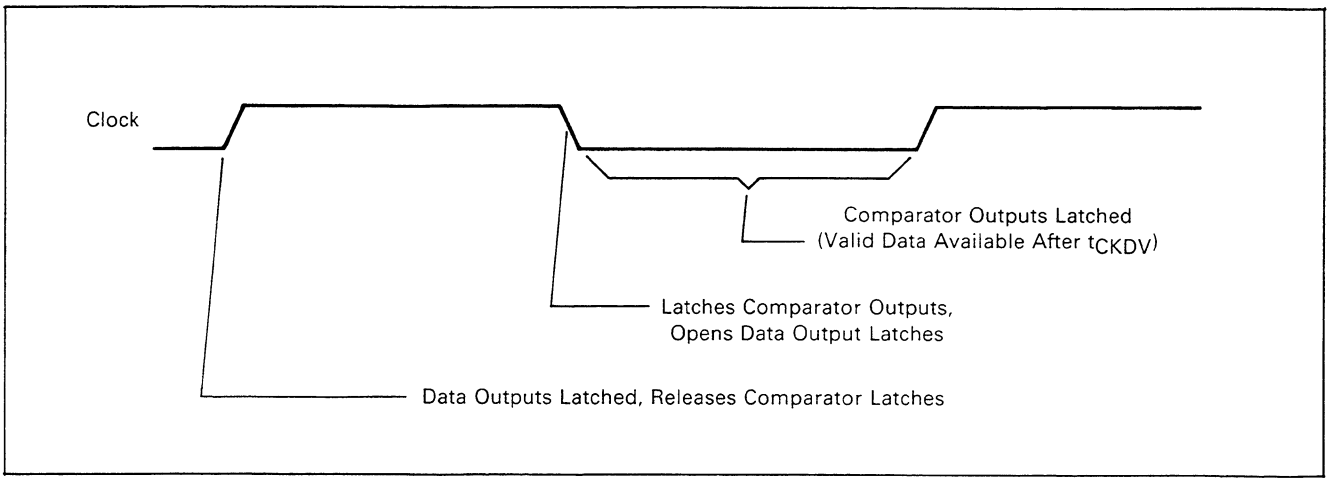
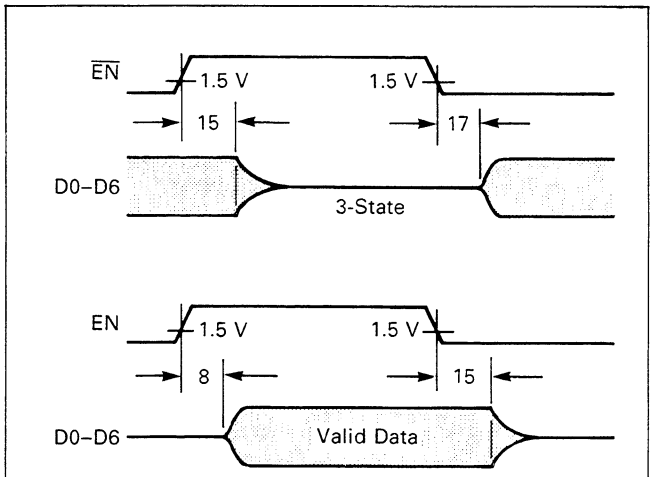
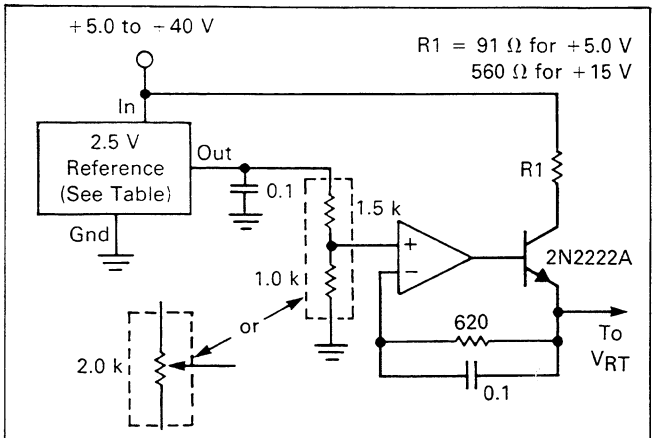


FIGURE 14 — ENABLE TO OUTPUT CRITICAL TIMING



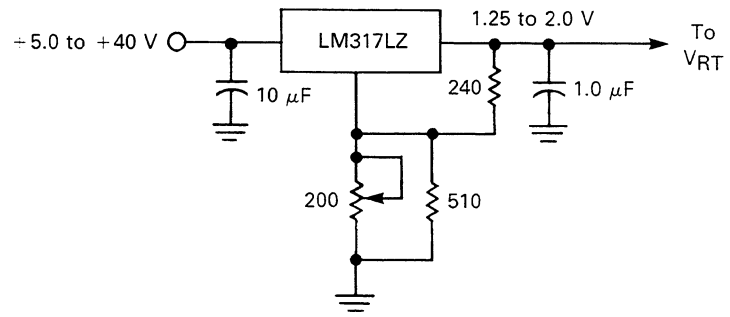
Timing « D6–D0 measured where waveform starts to change. Indicated time values are typical « 25°C, and are in ns.

FIGURE 15 — PRECISION V_{RT} VOLTAGE SOURCE



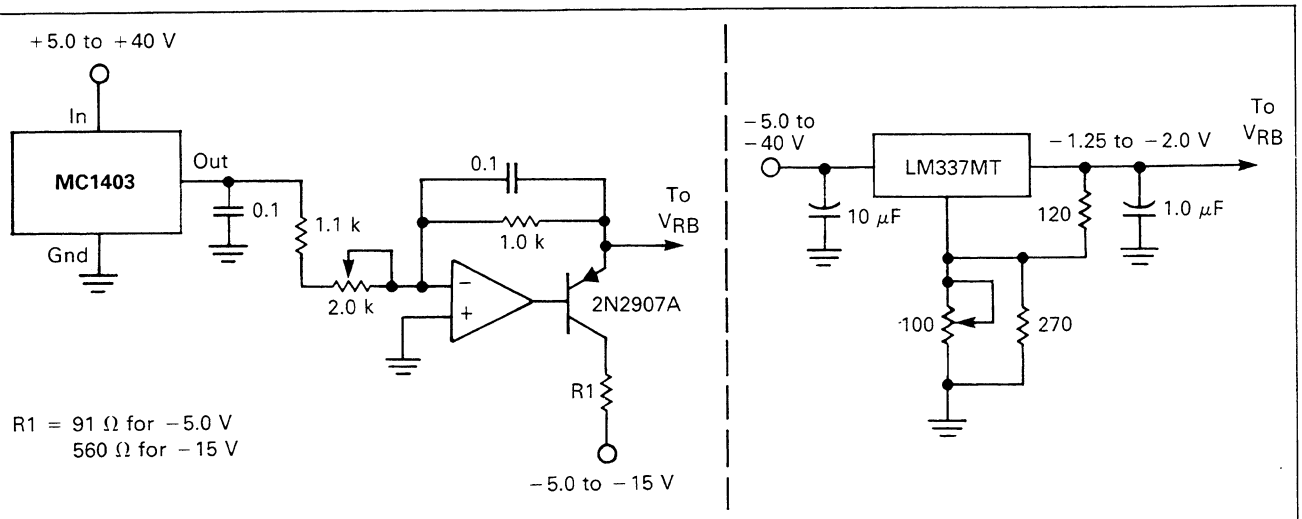
2.5 V References	MC1403U	MC1403AU
Line Regulation	0.5 mV	0.5 mV
TC (ppm °C) max	40	25
ΔV_{out} for 0–70°C	7.0 mV	4.4 mV
Initial Accuracy	±1.0%	±1.0%

FIGURE 16 — V_{RT} VOLTAGE SOURCE



LM317LZ	
Line Regulation	1.0 mV
TC (ppm/°C) max	60
ΔV_{out} for 0–70°C	8.4 mV
Initial Accuracy	±4.0%

FIGURE 17 — V_{RB} VOLTAGE SOURCES



Reference	MC1403U	MC1403AU	LM337MT
Line Regulation	0.5 mV	0.5 mV	1.0 mV
TC (ppm/°C) max	40	25	48
ΔV_{out} for 0–70°C	7.0 mV	4.4 mV	6.7 mV
Initial Accuracy	±1.0%	±1.0%	±4.0%

FIGURE 18

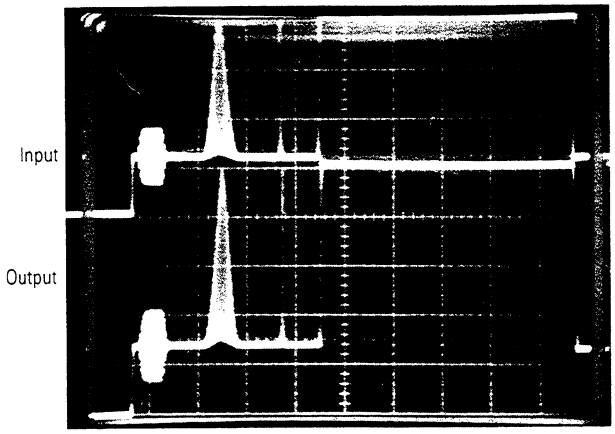


FIGURE 19

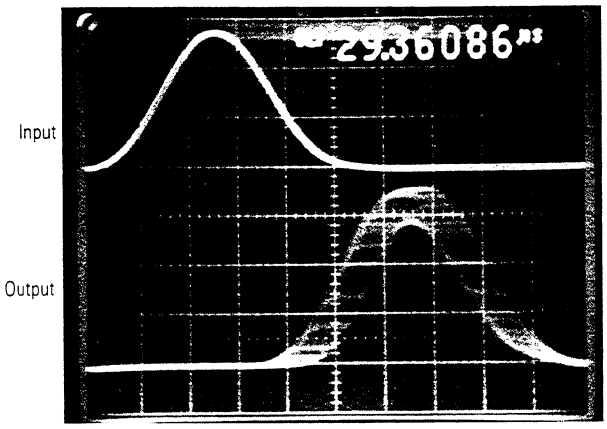
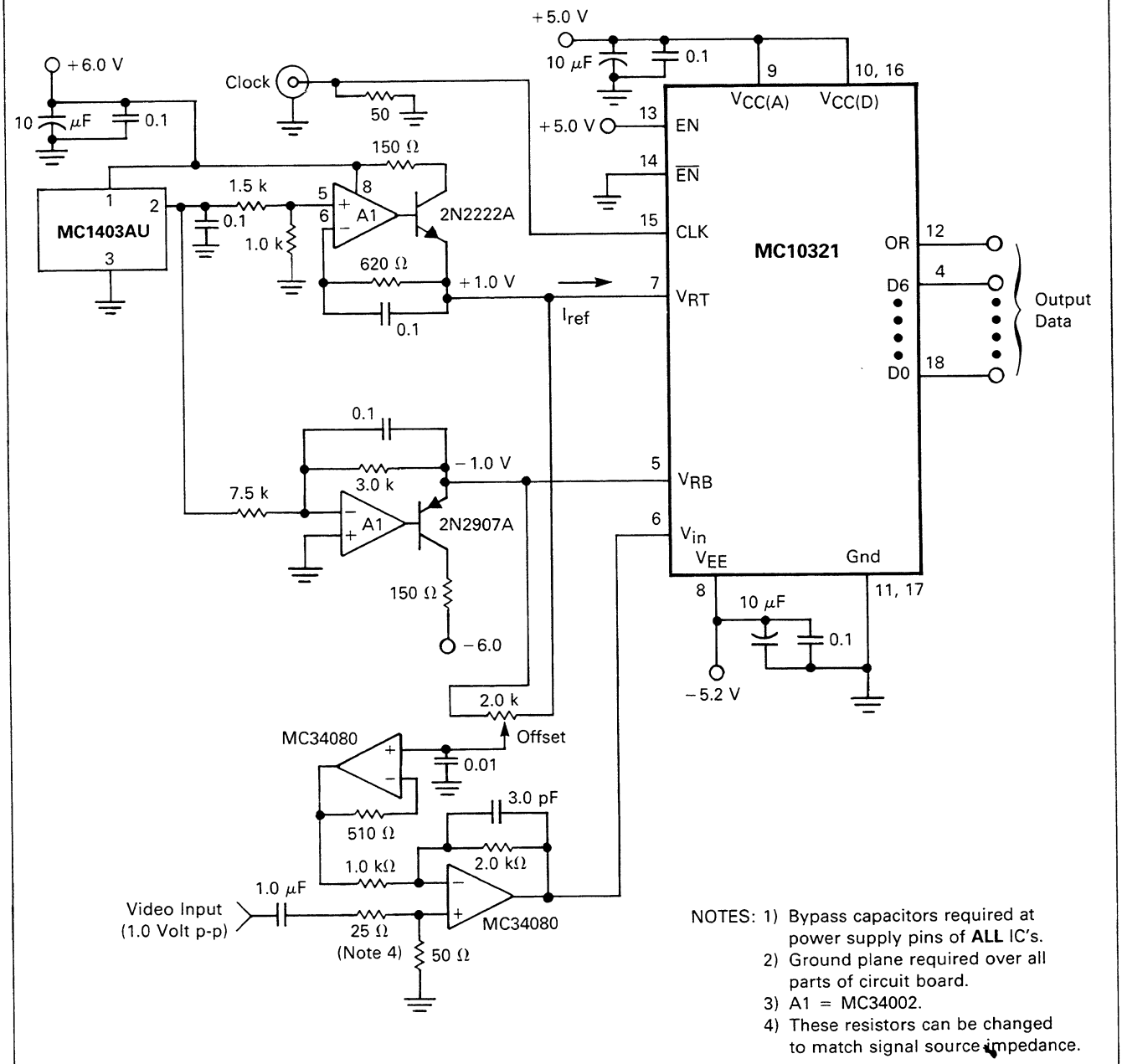


FIGURE 20 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



NOTES: 1) Bypass capacitors required at power supply pins of **ALL** IC's.
2) Ground plane required over all parts of circuit board.
3) A1 = MC34002.
4) These resistors can be changed to match signal source impedance.

FIGURE 21 — 8-BIT A/D CONVERTER

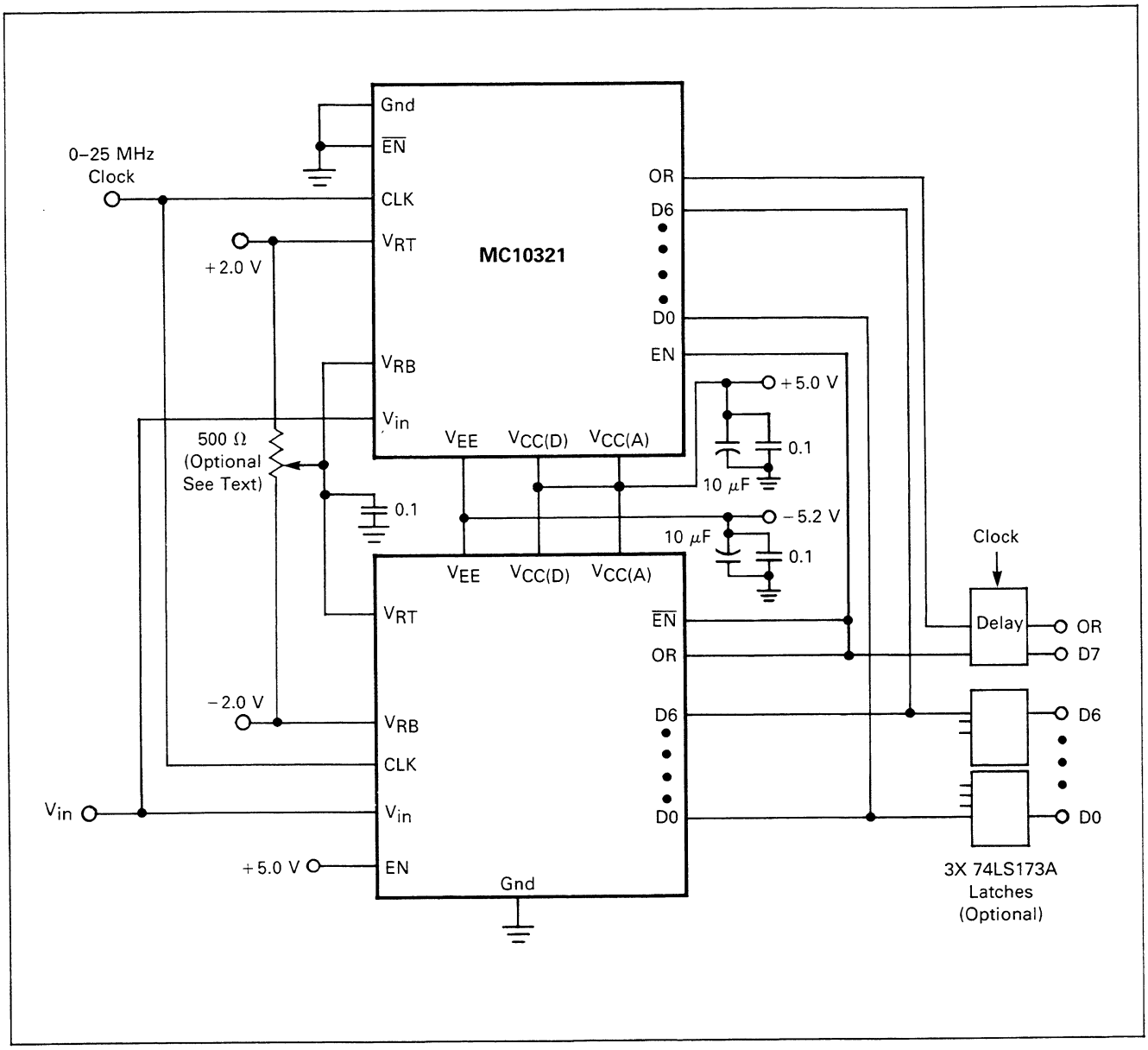


FIGURE 22 — 50 MHz 7 BIT A/D CONVERTER

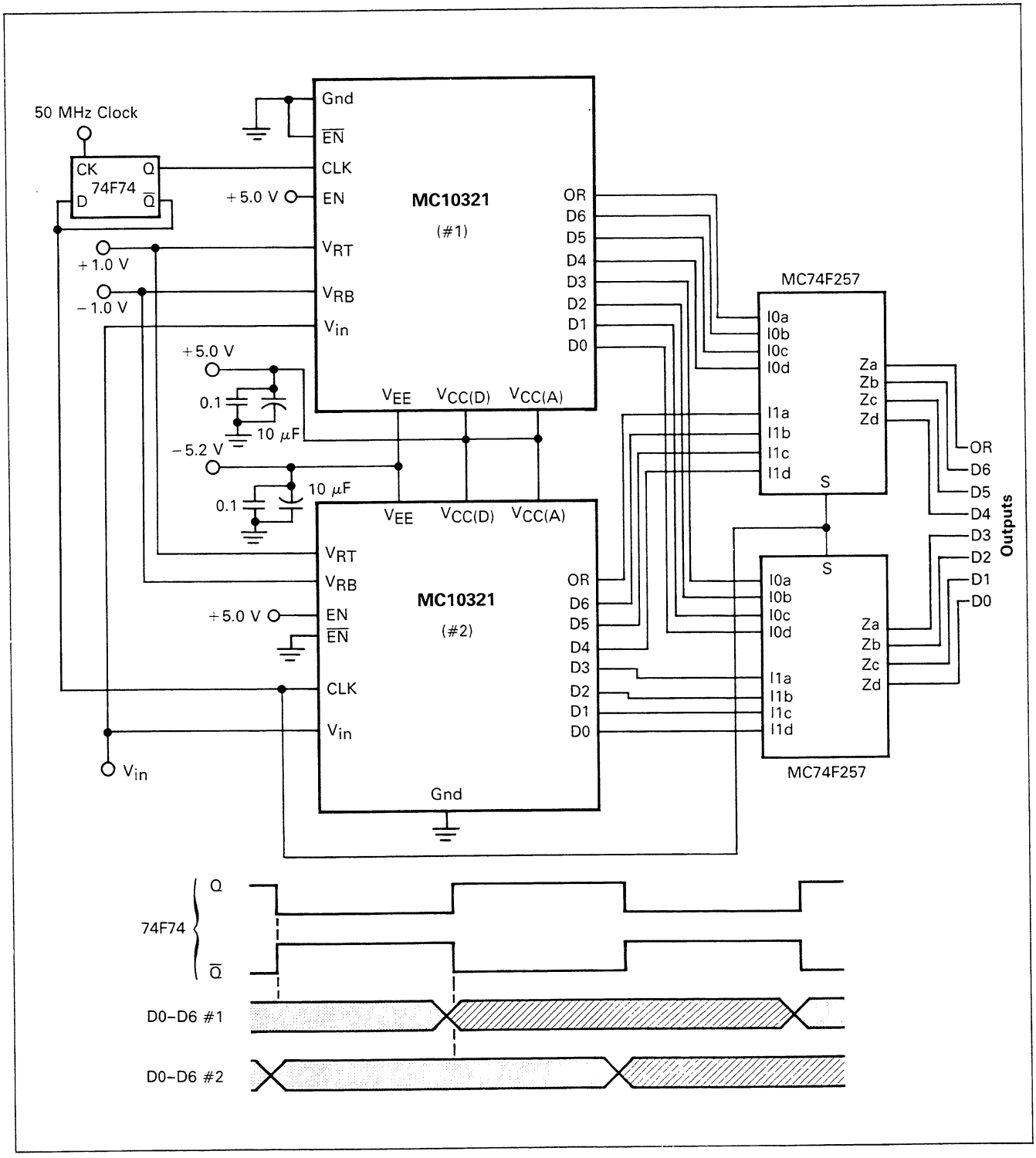
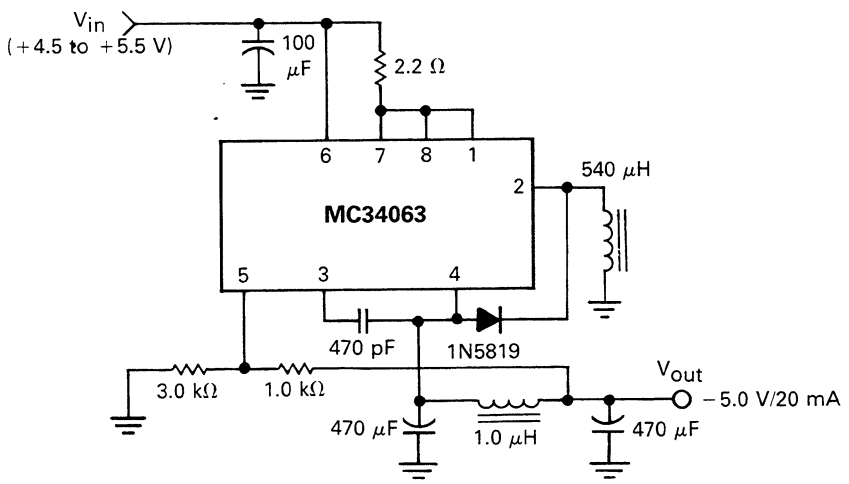
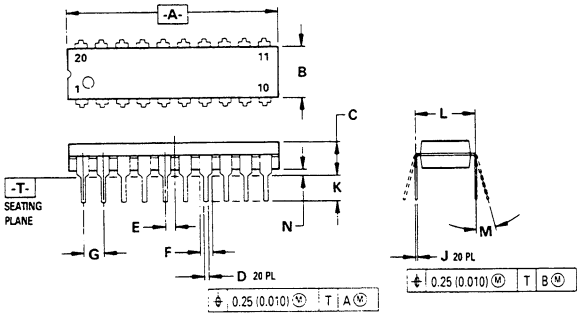


FIGURE 23 — −5.0 VOLT REGULATOR



Line Regulation	4.5 V < V_{in} < 5.5 V, I_{out} = 10 mA	0.16%
Load Regulation	V_{in} = 5.0 V, 8.0 mA < I_{out} < 20 mA	0.4%
Output Ripple	V_{in} = 5.0 V, I_{out} = 20 mA	2.0 mV p-p
Short Circuit I_{out}	V_{in} = 5.0 V, R_L = 0.1 Ω	140 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	52%

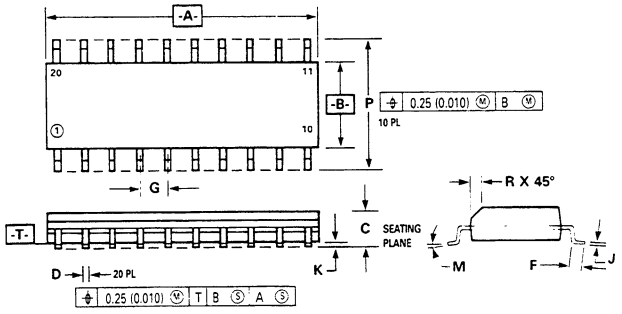
OUTLINE DIMENSIONS



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

P SUFFIX
PLASTIC PACKAGE
CASE 738-03



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.509
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

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MC10321/D

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