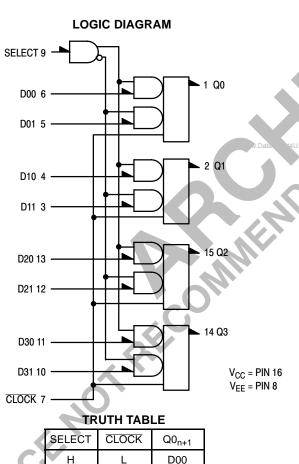
# Quad 2-Input Multiplexer/ Latch

The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

- $P_D = 275 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 2.5 \text{ ns typ}$
- $t_r$ ,  $t_f = 2.0$  ns typ (20%–80%)



L

D01

 $Q0_n$ 

# ON

## ON Semiconductor

http://onsemi.com

### MARKING DIAGRAMS



CDIP-16 L SUFFIX CASE 620 MC10173L AWLYYWW



PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775

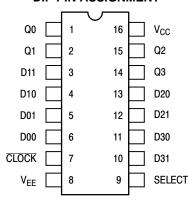


A = Assembly Location

WL = Wafer Lot

YY = Year WW = Work Week

### **DIP PIN ASSIGNMENT**



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

### **ORDERING INFORMATION**

Device	Package	Shipping		
MC10173L	CDIP-16	25 Units / Rail		
MC10173P	PDIP-16	25 Units / Rail		
MC10173FN	PLCC-20	46 Units / Rail		

L

### **ELECTRICAL CHARACTERISTICS**

;		Pin			' 	Test Limits				1
;		Under	-30			+25°C	1	+85	1	1
	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Uni
Current	Ι <sub>Ε</sub>	8		73			66		73	mAc
	$I_{inH}$	5		470			295		295	μΑσ
		6 7		470 400			295 250		295 250	
		9		400			250		250	
	I <sub>inL</sub>	All	0.5		0.5			0.3		μAc
Logic 1	V <sub>OH</sub>	1 2	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdd
Logic 0	V <sub>OL</sub>	1 2	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vd
Logic 1	V <sub>OHA</sub>	1 2	-1.080 -1.080		-0.980 -0.980			-0.910 -0.910		Vdd
Logic 0	V <sub>OLA</sub>	1 2		-1.655 -1.655			-1.630 -1.630		-1.595 -1.595	Vdo
Ω Load)								V		ns
ta Input	t <sub>6+1+</sub>	1	0.8	3.7	1,0	2.5	3.5	1.1	5.3	
·	t <sub>6-1-</sub>	1	0.8	3.7	1.0	2.5	3.5	1.1	5.3	
ck Innut										
ж прис	t <sub>7-1-</sub>	1	1.6	7.2	1.6	4.5	6.8	1.4	6.8	
ct Input	t <sub>9+1+</sub>	1	1.1	6.2	1.3	3.5	5.7	1.2	6.7	
	t <sub>9+1-</sub>									
	t <sub>9-1+</sub>	1	1.1	6.2	1.3	3.5	5.7	1.2	6.7	
ta Input ct Input	t <sub>setup</sub> t <sub>setup</sub>	1	2.0 3.0		2.0 3.0	1.5 2.5		2.0 3.0		
ta Input ct Input	t <sub>hold</sub> t <sub>hold</sub>	1	2.5 1.5		2.5 1.5	0.0 -0.5		2.5 1.5		
to 80%)	t+	1	1.2	4.0	1.5	2.0	3.5	1.4	4.0	
to 80%)	t–	1	1.2	4.0	1.5	2.0	3.5	1.4	4.0	
1 1 1	Logic 0  Logic 0  Logic 0  Logic 0  Logic 0  Logic 1  Logic 0  Logic 1  Logic 1  Logic 1	Logic 1 VOH  Logic 0 VOL  Logic 1 VOHA  Logic 0 VOLA  D Load)  Ita Input t6+1+ t6-1- t5+1+ t5-1- Ek Input t7-1+ t7-1- Et Input t9+1- t9-1+ t9-1- ta Input tsetup ta Input thold  Input thold  Logic 1 VOHA  Input t6+1+ t6-1- t5+1+ t7-1- Ek Input t7-1- t7-1- Et Input t7-1- t8-1- t9-1- t9-1- ta Input thold Input thold	Logic 1 VOH 1 2  Logic 0 VOL 1 2  Logic 1 VOHA 1 2  Logic 0 VOLA 1 2  Logic 1 VOHA 1 2  Logic 0 VOLA 1 2  Logic 1 VOHA 1 2  Logic 0 VOLA 1 2  Logic 0 VOLA 1 2  Logic 0 VOLA 1 2  Logic 1 VOHA 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Logic 1 V <sub>OH</sub> 1 -1.060  Logic 0 V <sub>OL</sub> 1 -1.890  Logic 1 V <sub>OHA</sub> 1 -1.080  Logic 1 V <sub>OHA</sub> 1 -1.080  Logic 0 V <sub>OLA</sub> 1  Logic 1 1 0.8  Logic 0 V <sub>OLA</sub> 1  Logic 0 V <sub>OLA</sub> 1  Logic 1 1 0.8  Logic 0 V <sub>OLA</sub> 1  Logic 0 V <sub>OLA</sub> 1  Logic 0 I 0.8  Logic 1 1 0.8  Logic 1 1 0.8  Logic 1 1 0.8  Logic 1 1 1 0.8  Logic 1 1 1 0.8  Logic 1 1 1 1 0.8  Logic 1 1 1 1 1.6  Logic 1 1 1 1.6  Logic 1 1 1.1  Logic 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Logic 1 V <sub>OH</sub> 1 -1.060 -0.890  Logic 0 V <sub>OL</sub> 1 -1.890 -1.675  Logic 1 V <sub>OHA</sub> 1 -1.080  Logic 0 V <sub>OLA</sub> 1 -1.080  Logic 0 V <sub>OLA</sub> 1 -1.080  Logic 0 V <sub>OLA</sub> 1 -1.655  Logic 1 V <sub>OHA</sub> 1 0.8 3.7  ta Input t <sub>6+1+</sub> 1 0.8 3.7  t <sub>5+1+</sub> 1 0.8 3.7  t <sub>1</sub> 1 1.6 7.2  tt Input t <sub>9+1+</sub> 1 1.6 7.2  tt Input t <sub>9+1+</sub> 1 1.1 6.2  t <sub>1</sub> 1.1 6.2  t <sub>2</sub> 1.1 6.2  ta Input t <sub>setup</sub> 1 2.0  ta Input t <sub>setup</sub> 1 3.0  ta Input t <sub>setup</sub> 1 2.0  ta Input t <sub>setup</sub> 1 2.5  ta Input t <sub>nold</sub> 1 2.5	Logic 1 V <sub>OH</sub> 1 -1.060 -0.890 -0.960  Logic 0 V <sub>OL</sub> 1 -1.890 -1.675 -1.850  Logic 1 V <sub>OHA</sub> 1 -1.080 -0.980  Logic 0 V <sub>OLA</sub> 1 -1.080 -0.980  Logic 0 V <sub>OLA</sub> 1 -1.655 -1.655  Logic 0 V <sub>OLA</sub> 1 -1.655 -1.655  Logic 1 V <sub>OHA</sub> 1 -1.080 -0.980  Logic 0 V <sub>OLA</sub> 1 -1.655 -1.655  Logic 1 V <sub>OHA</sub> 1 -1.655 -1.655  Logic 0 V <sub>OLA</sub> 1 -1.655 -1.655  Logic 1 V <sub>OHA</sub> 1 -1.655 -1.655  Logic 0 V <sub>OLA</sub> 1 -1.655 -1.655  Logic 1 V <sub>OHA</sub> 1 -1.655 -1.675  Logic 1 V <sub>OHA</sub> 1 -1.655 -1.675  Logic 1 V <sub>OHA</sub> 1 -1.655 -1.675  Logic 1 V <sub>OHA</sub> 1 -1.890 -1.675 -1.850  Logic 1 V <sub>OHA</sub> 1 -1.890 -1.675 -1.850  -1.890 -1.675 -1.850  -1.850 -1.850  -1.850 -1.85	Logic 1 VoH 1 1 -1.060 -0.890 -0.960   Logic 0 VoL 1 -1.890 -1.675 -1.850   Logic 1 VoHA 1 -1.080 -0.980   Logic 0 VoLA 1 -1.080 -0.980   Logic 0 VoLA 1 -1.080 -0.980   Logic 0 VoLA 1 -1.655   Logic 0 VoLA 1 -1.655   Logic 1 VoHA 2 -1.655   Logic 0 VoLA 1 -1.655   Logic 0 VoLA 1 -1.655   Logic 1 VoHA 2 -1.655   Logic 0 VoLA 1 -1.655   Logic 1 -1.655    Logic 1 -1.655   Logic 1 -1.655    Logic 1 -1.655   Logic 1 -1.65	Logic 1 V <sub>OH</sub> 1	Logic 1 V <sub>OH</sub> 1 -1.060 -0.890 -0.960 -0.810 -0.890 -0.890 Logic 0 V <sub>OL</sub> 1 -1.890 -1.675 -1.850 -1.650 -1.825 -1.850 -1.850 -1.850 -1.825 -1.850 -1.850 -1.825 -1.850 -1.850 -1.825 -1.850 -1.650 -1.825 -1.850 -1.825 -1.850 -1.850 -1.825 -1.850 -1.85	Logic 1 V <sub>OH</sub> 1 1 -1.060 -0.890 -0.960 -0.810 -0.890 -0.700  Logic 0 V <sub>OL</sub> 1 -1.890 -1.675 -1.850 -1.650 -1.825 -1.615  Logic 1 V <sub>OHA</sub> 1 -1.080 -0.980 -0.980 -0.980  Logic 0 V <sub>OLA</sub> 1 -1.080 -1.675 -1.850 -1.650 -1.825 -1.615  Logic 1 V <sub>OHA</sub> 1 -1.080 -0.980 -0.980 -0.9910  Logic 0 V <sub>OLA</sub> 1 -1.655 -1.655 -1.630 -1.630 -1.595  Logic 0 V <sub>OLA</sub> 1 -1.655 -1.655 -1.630 -1.630 -1.595  Logic 1 V <sub>OHA</sub> 1 0.8 3.7 1.0 2.5 3.5 1.1 5.3 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.5 1.1 5.3 1.

## **ELECTRICAL CHARACTERISTICS** (continued)

				TEST VOLTAGE VALUES (Volts)					
	@ Test Temperature			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
			–30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
Pin			TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
Characteristic		Symbol	Under Test	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	(V <sub>CC</sub> ) Gnd
Power Supply Drain Cu	ırrent	Ι <sub>Ε</sub>	8					8	16
Input Current			5	5				8	16
			6 7	6 7				8 8	16 16
			9	9				8	16
		I <sub>inL</sub>	All		*			8	16
Output Voltage	Logic 1	V <sub>OH</sub>	1	6, 9	7			8	16
			2	5	7			8	16
Output Voltage	Logic 0	$V_{OL}$	1 2	9	7 7			8 8	16 16
Threshold Voltage	Logic 1	V <sub>OHA</sub>	1 2	9	7 7	6 5		8 8	16 16
Threshold Voltage	Logic 0	V <sub>OLA</sub>	1 2	9	7 7		6 5	8 8	16 16
Switching Times	(50Ω Load)			+1.11V	+0.31V	Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	Data Input	t <sub>6+1+</sub>	1	9	7	6	1	8	16
		t <sub>6-1-</sub>	1	9	7	6	1	8	16
		t <sub>5+1+</sub> t <sub>5–1–</sub>	1		7	. 5 5	1 1	8 8	16 16
	Clock Input	-	1			5, 7		_	16
	Clock Input	t <sub>7–1+</sub> t <sub>7–1–</sub>	1			5, 7 5, 7	1 1	8 8	16
	Select Input	t <sub>9+1+</sub>	1	6	7	9	1	8	16
	Ocicet input	t <sub>9+1+</sub> t <sub>9+1-</sub>	1	5	7	9	1	8	16
		t <sub>9-1+</sub>	1	5	7	9	1	8	16
	Ì	t <sub>9-1-</sub>	1	6	7	9	1	8	16
Setup TIme	Data Input Select Input	t <sub>setup</sub> t <sub>setup</sub>		6		5, 7 7, 9	1 1	8 8	16 16
Hold TIme	Data Input Select Input	t <sub>hold</sub> t <sub>hold</sub>	1	6		5, 7 7, 9	1 1	8 8	16 16
Rise Time	(20 to 80%)	t+	1	5		7	1	8	16
Fall Time	(20 to 80%)	t–	1			7	1	8	16

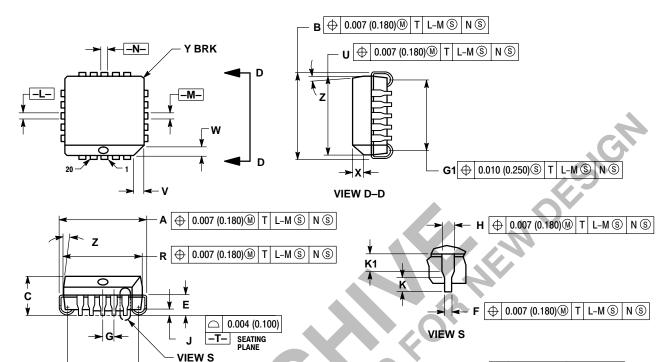
<sup>\*</sup> V<sub>ILmin</sub> applied to each input pin, one at a time.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

### PACKAGE DIMENSIONS

### PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



### NOTES:

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF VICE NOT PRESCO

- IOTES:

  1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

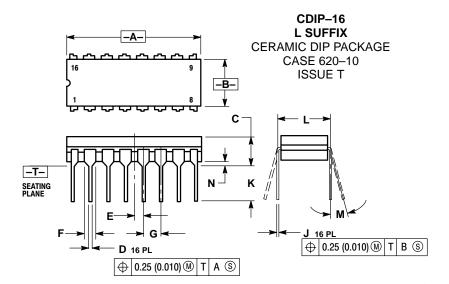
  2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

  3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

  4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982.
- Y14.5M, 1982. 5. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIMETERS			
DIM	MIN MAX		MIN	MAX		
Α	0.385	0.395	9.78	10.03		
В	0.385	0.395	9.78	10.03		
С	0.165	0.180	4.20	4.57		
E	0.090	0.110	2.29	2.79		
F	0.013	0.019	0.33	0.48		
G	0.050	BSC	1.27 BSC			
Н	0.026	0.032	0.66	0.81		
J	0.020		0.51			
K	0.025		0.64			
R	0.350	0.356	8.89	9.04		
U	0.350	0.356	8.89	9.04		
٧	0.042	0.048	1.07	1.21		
W	0.042	0.048	1.07	1.21		
X	0.042	0.056	1.07	1.42		
Y		0.020		0.50		
Z	2°	10°	2°	10 °		
G1	0.310	0.330	7.88	8.38		
K1	0.040		1.02			

### PACKAGE DIMENSIONS



### NOTES:

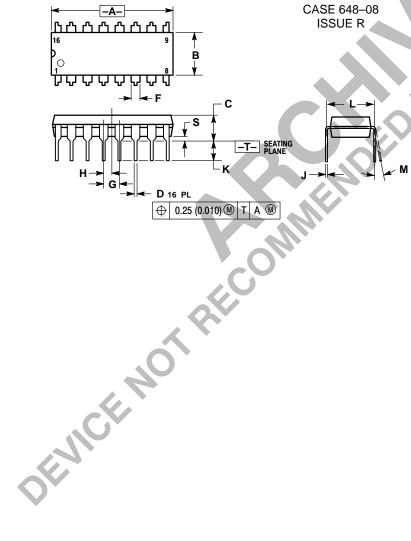
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
   CONTROLLING DIMENSION: INCH.
   DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

  DIMENSION F MAY NARROW TO 0.76 (0.030)
  WHERE THE LEAD ENTERS THE CERAMIC
  BODY.

	INC	HES	MILLIMETERS			
DIM	MIN MAX		MIN	MAX		
Α	0.750	0.785	19.05	19.93		
В	0.240	0.295	6.10	7.49		
C		0.200		5.08		
D	0.015	0.020	0.39	0.50		
E	0.050	BSC	1.27 BSC			
F	0.055	0.065	1.40	1.65		
G	0.100	BSC	2.54 BSC			
Н	0.008	0.015	0.21	0.38		
K	0.125	0.170	3.18	4.31		
L	0.300	BSC	7.62	BSC		
M	0 °	15°	0 °	15°		
N	0.020	0.040	0.51	1.01		

### PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS	
DIM	MIN MAX		MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27	BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

# **Notes**



# **Notes**





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