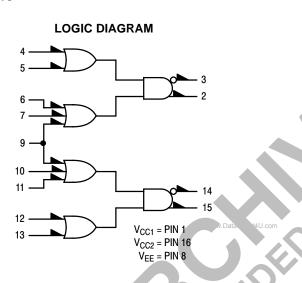
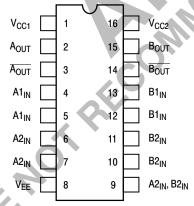
# Dual 2-Wide 2-3-Input OR-AND/OR-AND Gate

The MC10117 is a dual 2-wide 2-3-input OR-AND/OR-AND-Invert gate. This general purpose logic element is designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

- $P_D = 100 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 2.3 \text{ ns typ}$
- $t_r$ ,  $t_f = 2.2$  ns typ (20%–80%)



#### DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



### ON Semiconductor

http://onsemi.com

#### MARKING DIAGRAMS

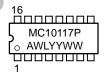


CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

#### **ORDERING INFORMATION**

Device	Package	Shipping
MC10117L	CDIP-16	25 Units / Rail
MC10117P	PDIP-16	25 Units / Rail
MC10117FN	PLCC-20	46 Units / Rail

#### **ELECTRICAL CHARACTERISTICS**

Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)	VOLA  VOHA  VOLA  VOLA  t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same l <sub>inH</sub> limit	Pin Under Test  8  6  9  4  2  3  2  3  2  3  2  3  2  3  2  3  2  3  2  3  2  3  2  3  3	-3 Min  0.5  -1.060 -1.060 -1.890 -1.890 -1.080  -1.080  1.4 1.4 1.4 1.4 0.9 0.9 0.9	0°C Max 29 425 560 390 -0.890 -0.780 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1	0.5 -0.960 -0.960 -1.850 -0.980 -0.980 -0.980	+25°C Typ 20  2.3 2.3 2.3 2.3 2.2	Max  26  265 350 245  -0.810 -0.700 -1.650 -1.650  -1.630  3.4 3.4 3.4 3.4	-85 Min  0.3  -0.890 -0.890 -1.825 -1.825 -0.910 -0.910  1.4 1.4 1.4 1.4	-0.700 -0.590 -1.615 -1.595 -1.595 -3.8 3.8 3.8 3.8	Vo
Power Supply Drain Current Input Current  Output Voltage Logic 0  Threshold Voltage Logic 0  Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)  Inputs 4, 5, 12 and 13 have s	IE	8 6 9 4 4 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3	0.5 -1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	29 425 560 390  -0.890 -0.780 -1.675 -1.675  -1.655 3.9 3.9 3.9 3.9 4.1 4.1	0.5 -0.960 -0.960 -1.850 -1.850 -0.980 -0.980 1.4 1.4 1.4 1.4 1.4	2.3 2.3 2.3 2.3 2.3	26 265 350 245 -0.810 -0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 3.4	0.3 -0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4	29 265 350 245 -0.700 -0.590 -1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8	mA μA να
Output Voltage Logic 1  Output Voltage Logic 0  Threshold Voltage Logic 0  Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)	IinH*   IinH   VOH   VOHA   VOHA	6 9 4 4 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	425 560 390 -0.890 -0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 1.4 1.4 1.4 1.4	2.3 2.3 2.3 2.3	265 350 245 -0.810 -0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 3.4	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4	265 350 245 -0.700 -0.590 -1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8	μΑ Vc Vc
Output Voltage Logic 1 Output Voltage Logic 0 Threshold Voltage Logic 0 Threshold Voltage Logic 0 Switching Times (50Ω Load) Propagation Delay  Rise Time (20 to 80%) Fall Time (20 to 80%)	IinL   VOH   VOL   VOHA   VOLA	9 4 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	-0.890 -0.780 -1.675 -1.675 -1.655 -1.655 -3.9 3.9 3.9 3.9 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 1.4 1.4 1.4 1.4	2.3 2.3 2.3	350 245 -0.810 -0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 3.4	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4	-0.700 -0.590 -1.615 -1.615 -1.595 -1.595 -3.8 3.8 3.8	μAi Vo
Output Voltage Logic 0  Threshold Voltage Logic 0  Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)	VOH  VOLA  VOLA  VOLA  t4+2+ t4-2- t4+3- t4-3+ t2- t3+ t2- t3- same I <sub>inH</sub> limit	4 4 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	390  -0.890 -0.780  -1.675 -1.675  -1.655 -1.655  3.9 3.9 3.9 3.9 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 1.4 1.4 1.4 1.4	2.3 2.3 2.3	-1.630 -1.630 -1.630 -3.4 3.4 3.4 3.4	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4	-0.700 -0.590 -1.615 -1.615 -1.595 -1.595 -3.8 3.8 3.8	Vo Vo
Output Voltage Logic 0  Threshold Voltage Logic 0  Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)	VOH  VOLA  VOLA  VOLA  t4+2+ t4-2- t4+3- t4-3+ t2- t3+ t2- t3- same I <sub>inH</sub> limit	2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	-0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 1.4 1.4 1.4 1.4	2.3 2.3 2.3	-0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4	-0.590 -1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8	μAα Vd Vd Vd
Output Voltage Logic 0  Threshold Voltage Logic 0  Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)	VOLA  VOHA  VOLA  t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same I <sub>inH</sub> limit	3 2 3 2 3 2 3 2 2 3 3 2 3 2 3 2 3	-1.060 -1.890 -1.890 -1.080 -1.080 -1.080 -1.080	-0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1	-0.960 -1.850 -1.850 -0.980 -0.980 -1.4 1.4 1.4 1.4	2.3 2.3 2.3	-0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4	-0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4	-0.590 -1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8	Vo
Threshold Voltage Logic 1  Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)	VOHA  VOLA  t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same l <sub>inH</sub> limit	2 3 2 3 2 3 2 2 3 3 2 3 2 3 2 3	-1.890 -1.890 -1.080 -1.080 -1.080 -1.080	-1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1	-1.850 -1.850 -0.980 -0.980 -1.4 1.4 1.4 1.4	2.3 2.3 2.3	-1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4	-1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4	-1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8	Vo
Threshold Voltage Logic 1  Threshold Voltage Logic 0  Switching Times (50Ω Load)  Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)	VOHA  VOLA  t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same l <sub>inH</sub> limit	3 2 3 2 3 2 2 2 3 3 2 3	-1.890 -1.080 -1.080 -1.080 1.4 1.4 1.4 1.4 0.9 0.9	-1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1	-1.850 -0.980 -0.980 1.4 1.4 1.4 1.4	2.3 2.3 2.3	-1.630 -1.630 3.4 3.4 3.4 3.4	-1.825 -0.910 -0.910 1.4 1.4 1.4	-1.615 -1.595 -1.595 3.8 3.8 3.8	Vo
Threshold Voltage Logic 0 Switching Times (50Ω Load) Propagation Delay  Rise Time (20 to 80%) Fall Time (20 to 80%)	t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same I <sub>inH</sub> limit	2 3 2 3 2 2 2 3 3 2 3	1.4 1.4 1.4 1.4 1.4 0.9 0.9	-1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1	1.4 1.4 1.4 1.4 1.1	2.3 2.3 2.3	-1.630 -1.630 3.4 3.4 3.4 3.4	1.4 1.4 1.4 1.4	-1.595 3.8 3.8 3.8	Vo
Threshold Voltage Logic 0 Switching Times (50Ω Load) Propagation Delay  Rise Time (20 to 80%) Fall Time (20 to 80%)	t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same I <sub>inH</sub> limit	3 2 3 2 2 2 3 3 2 3	1.4 1.4 1.4 1.4 1.4 0.9 0.9	3.9 3.9 3.9 3.9 3.9 4.1 4.1	1.4 1.4 1.4 1.4 1.1	2.3 2.3 2.3	3.4 3.4 3.4 3.4 3.4	1.4 1.4 1.4 1.4	-1.595 3.8 3.8 3.8	Vo
Switching Times (50Ω Load) Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)	t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same l <sub>inH</sub> limit	2 2 3 3 2 3	1.4 1.4 1.4 0.9 0.9	3.9 3.9 3.9 3.9 3.9 4.1 4.1	1,4 1.4 1.4	2.3 2.3 2.3	3.4 3.4 3.4 3.4 3.4	1.4 1.4 1.4	-1.595 3.8 3.8 3.8	
Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)  Inputs 4, 5, 12 and 13 have s	t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub>	2 2 3 3 2 3	1.4 1.4 1.4 0.9 0.9	3.9 3.9 3.9 3.9 4.1 4.1	1,4 1.4 1.4	2.3 2.3 2.3	3.4 3.4 3.4 3.4	1.4 1.4 1.4	3.8 3.8 3.8	ns
Propagation Delay  Rise Time (20 to 80%)  Fall Time (20 to 80%)  Inputs 4, 5, 12 and 13 have s	t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub>	2 3 3 2 3	1.4 1.4 1.4 0.9 0.9	3.9 3.9 3.9 4.1 4.1	1,4 1.4 1.4	2.3 2.3 2.3	3.4 3.4 3.4	1.4 1.4 1.4	3.8 3.8	ns
Rise Time (20 to 80%) Fall Time (20 to 80%) Inputs 4, 5, 12 and 13 have s	t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub>	2 3 3 2 3	1.4 1.4 1.4 0.9 0.9	3.9 3.9 3.9 4.1 4.1	1,4 1.4 1.4	2.3 2.3 2.3	3.4 3.4 3.4	1.4 1.4 1.4	3.8 3.8	
Fall Time (20 to 80%) Inputs 4, 5, 12 and 13 have s	t <sub>4+3</sub> - t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same l <sub>inH</sub> limit	3 3 2 3	1.4 1.4 0.9 0.9	3.9 3.9 4.1 4.1	1.4 1.4 1.1	2.3 2.3	3.4 3.4	1.4 1.4	3.8	
Fall Time (20 to 80%) Inputs 4, 5, 12 and 13 have s	t <sub>4-3+</sub> t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same I <sub>inH</sub> limit	3 2 3 2	1.4 0.9 0.9	3.9 4.1 4.1	1.4 1.1	2.3	3.4	1.4		
Fall Time (20 to 80%) Inputs 4, 5, 12 and 13 have s	t <sub>2+</sub> t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same I <sub>inH</sub> limit	3 2	0.9	4.1		2.2	4.0			
Inputs 4, 5, 12 and 13 have s	t <sub>3+</sub> t <sub>2-</sub> t <sub>3-</sub> same l <sub>inH</sub> limit	2			4.4		4.0	1.1	4.6	
Inputs 4, 5, 12 and 13 have s	t <sub>3-</sub> same l <sub>inH</sub> limit		0.9		1.1	2.2	4.0	1.1	4.6	
Inputs 4, 5, 12 and 13 have s Inputs 6, 7, 10 and 11 have s	same I <sub>inH</sub> Iimit	3	0.9	4.1 4.1	1.1 1.1	2.2 2.2	4.0 4.0	1.1 1.1	4.6 4.6	
OFNICE	51 04									

#### **ELECTRICAL CHARACTERISTICS** (continued)

				TEST VOLTAGE VALUES (Volts)					
		@ Test Te	mperature	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
			–30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
Pin			TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
Characteristic		Symbol	Under Test	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	(V <sub>CC</sub> ) Gnd
Power Supply Drain (	Current	Ι <sub>Ε</sub>	8					8	1, 16
Input Current		I <sub>inH</sub> *	6	4				8	1, 16
			9 4	9	4			8 8	1, 16 1, 16
		I <sub>inL</sub>	4		9			8	1, 16
Output Voltage	Logic 1	V <sub>OH</sub>	2 3	4, 9				8	1, 16 1, 16
Output Voltage	Logic 0	V <sub>OL</sub>	2 3	4, 9				8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V <sub>OHA</sub>	2 3	9		4	4	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V <sub>OLA</sub>	2 3	9		4	4	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			+1.11V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay		t <sub>4+2+</sub> t <sub>4-2-</sub> t <sub>4+3-</sub> t <sub>4-3+</sub>	2 2 3 3	9 9 9 9		4 4 4 4	2 2 3 3	8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time	(20 to 80%)	t <sub>2+</sub> t <sub>3+</sub>	2 3	9 9		4 4	2 3	8 8	1, 16 1, 16
Fall Time	(20 to 80%)	t <sub>2-</sub> t <sub>3-</sub>	2 3	9 9		4 4	2 3	8 8	1, 16 1, 16

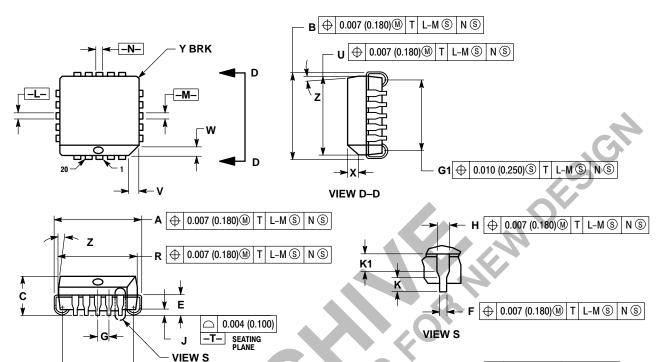
<sup>\*</sup> Inputs 4, 5, 12 and 13 have same I<sub>inH</sub> limit. Inputs 6, 7, 10 and 11 have same I<sub>inH</sub> limit.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

#### PACKAGE DIMENSIONS

#### PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



#### NOTES:

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF MICE. NOT PERSON

- IOTES:

  1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

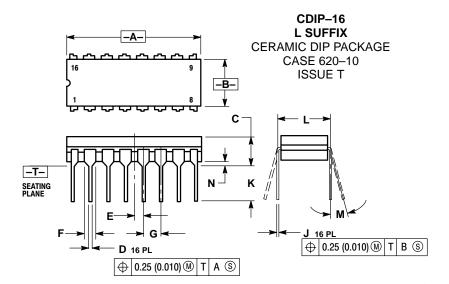
  2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

  3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

  4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982.
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.385	0.395	9.78	10.03
В	0.385	0.395	9.78	10.03
С	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
Н	0.026	0.032	0.66	0.81
J	0.020		0.51	
K	0.025		0.64	
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
٧	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50
Z	2°	10°	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040		1.02	

#### PACKAGE DIMENSIONS



#### NOTES:

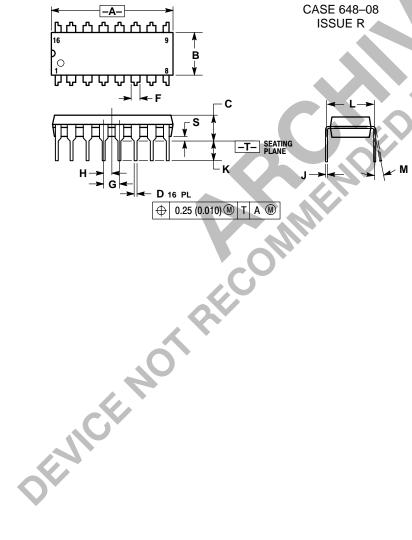
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
   CONTROLLING DIMENSION: INCH.
   DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

  DIMENSION F MAY NARROW TO 0.76 (0.030)
  WHERE THE LEAD ENTERS THE CERAMIC
  BODY.

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
E	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100	BSC	2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62	BSC	
М	0 °	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	





- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

## **Notes**



## **Notes**





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