NEC

MOS INTEGRATED CIRCUI

MC-451AB64S

1M-WORD BY 64-BIT SYNCHRONOUS DYNAMIC RAM MODULE (SO DIMM)

Description

The MC-451AB64S is a 1,048,576 words by 64 bits synchronous dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M SDRAM: μPD4516161 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- Clock frequency and Clock access time

	Family	/CAS latency	Clock frequency (MAX.)	Clock access time (MAX.)	Power consumption (MAX.)	
					Active	Standby
★	MC-451AB64S-A10	CL = 3	100 MHz	8 ns	2,448 mW	28.8 mW (CMOS level input)
		CL = 2	67 MHz	10 ns		
	MC-451AB64S-A67	CL = 3	67 MHz	9 ns	2,160 mW	
		CL = 2		10 ns		
★	MC-451AB64S-A12	CL = 3	83 MHz	9 ns	2,160 mW	
		CL = 2	55 MHz	12 ns		

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by BA0 (Bank Select)
- ★ • Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- ★ • Single 3.3 V ±0.3 V power supply
- LVTTL compatible
- 2,048 refresh cycles/32 ms
- Burst termination by Burst Stop command and Precharge command
- 144-pin dual in-line memory module (Pin pitch = 0.8 mm)
- Unbuffered type
- Serial PD

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The mark ★ shows major revised points.

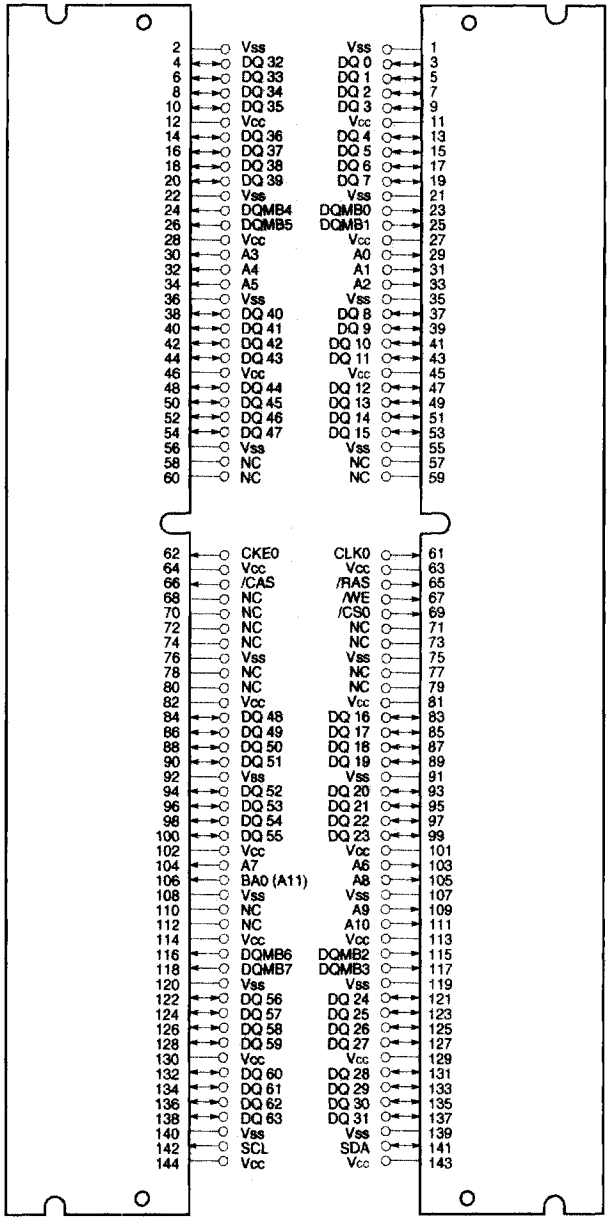
Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
★ MC-451AB64S-A10	100 MHz	144-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated 25.4 mm (1 inch) height	4 pieces of μPD4516161G5 (400 mil TSOP (II)) [Single side]
MC-451AB64S-A67	67 MHz		4 pieces of μPD4516161G5-PC (400 mil TSOP (II)) SDRAM Lite [Single side]
MC-451AB64S-A12	83 MHz		4 pieces of μPD4516161G5 (400 mil TSOP (II)) [Single side]

Pin Configuration

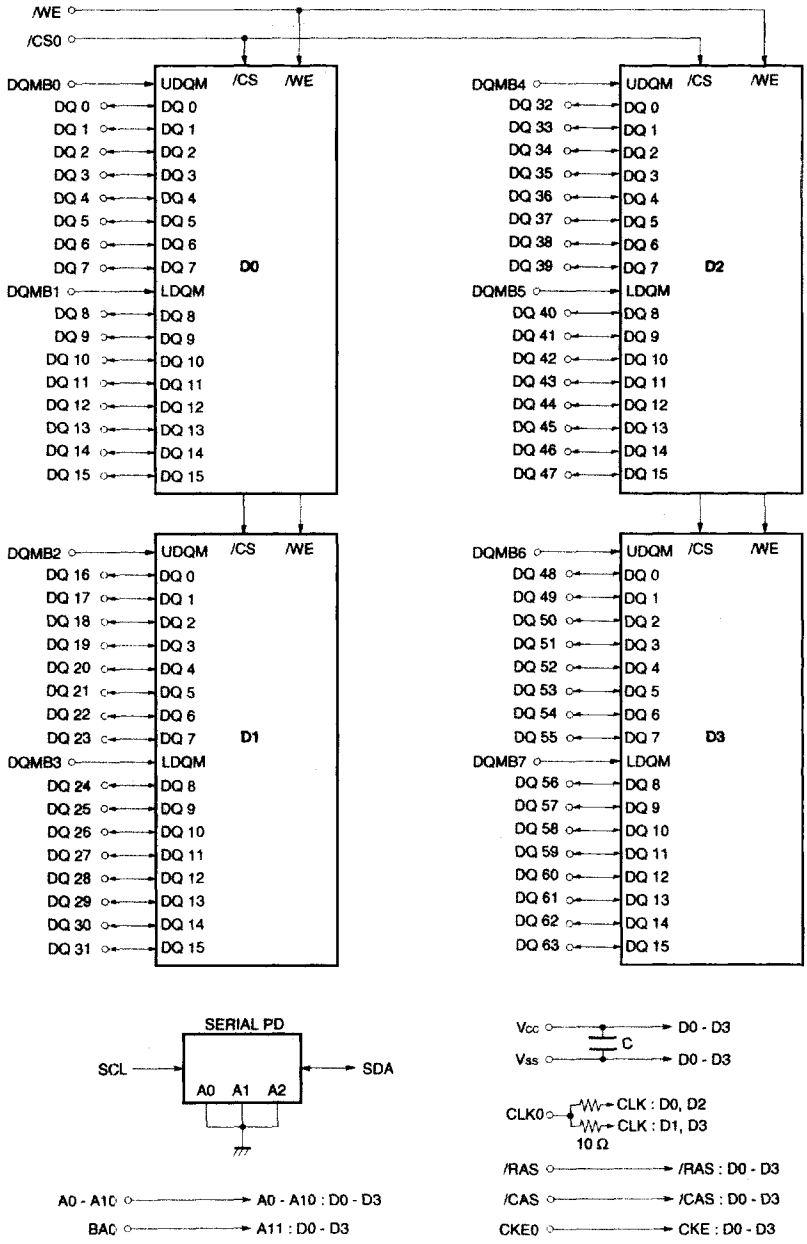
144-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

[MC-451AB64S]



A0 - A10	: Address Inputs
[Row: A0 - A10, Column: A0 - A7]	
BA0 (A11)	: SDRAM Bank Select
DQ0 - DQ63	: Data Inputs/Outputs
CLK0	: Clock Input
CKE0	: Clock Enable Input
/CS0	: Chip Select Input
/RAS	: Row Address Strobe
/CAS	: Column Address Strobe
/WE	: Write Enable
DQMB0 - DQMB7	: DQ Mask Enable
SDA	: Serial Data I/O for PD
SCL	: Clock Input for PD
Vcc	: Power Supply
Vss	: Ground
NC	: No Connection

★ **Block Diagram**



Remark D0 - D3 : μPD4516161(512K words x 16 bits x 2 banks)

Electrical Specifications (Preliminary)

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		−1.0 to +4.6	V
Voltage on input pin relative to GND	V_T		−1.0 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		− 55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		4.6	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, BA0(A11), /RAS, /CAS, /WE			30	pF
	C_{I2}	CLK0			30	
	C_{I3}	CKE0			30	
	C_{I4}	/CS0			30	
	C_{I5}	DQMB0 - DQMB7			10	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63			10	pF

★ **DC Characteristics (Recommended Operating Conditions unless otherwise noted)**

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC(MIN.)}$ I_O = 0 mA	/CAS latency = 2			340	mA	1
			/CAS latency = 3			360		
Precharge standby current in power down mode	I_{CC2P}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				12	mA	
	I_{CC2PS}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				8		
Precharge standby current in non power down mode	I_{CC2N}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				100	mA	
	I_{CC2NS}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				24		
Active standby current in power down mode	I_{CC3P}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				12	mA	
	I_{CC3PS}	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				8		
Active standby current in non power down mode	I_{CC3N}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				120	mA	
	I_{CC3NS}	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				40		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$ I_O = 0 mA	/CAS latency = 2	-A10		560	mA	2
				-A67		560		
				-A12		480		
			/CAS latency = 3	-A10		680		
				-A67		600		
				-A12		600		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$				360	mA	3
Self refresh current	I_{CC6}	CKE ≤ 0.2 V				8	mA	
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V			−20	+20	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V			−5	+5	μA	
High level output voltage	V_{OH}	I_O = −2.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA				0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

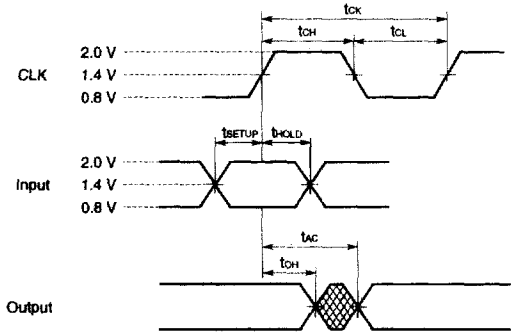
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

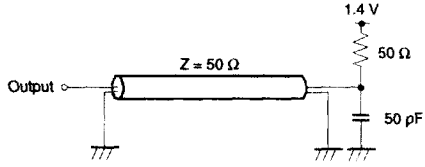
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



★ **Synchronous Characteristics**

Parameter		Symbol	-A10		-A67		-A12		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	10		15		12		ns	
	/CAS latency = 2	t_{CK2}	15		15		18		ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		8		9		9	ns	1
	/CAS latency = 2	t_{AC2}		10		10		12	ns	1
CLK high level width		t_{CH}	3.5		4		4		ns	
CLK low level width		t_{CL}	3.5		4		4		ns	
Data-out hold time		t_{OH}	4		3		4		ns	1
Data-out low-impedance time		t_{LZ}	0		0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t_{HZ3}	3	8	3	8	3	8	ns	
	/CAS latency = 2	t_{HZ2}	3	9	3	8	3	11	ns	
Data-in setup time		t_{DS}	2.5		3		3		ns	
Data-in hold time		t_{DH}	1		1.5		1.5		ns	
Address setup time		t_{AS}	2.5		3		3		ns	
Address hold time		t_{AH}	1		1.5		1.5		ns	
CKE setup time		t_{CKS}	2.5		3		3		ns	
CKE hold time		t_{CKH}	1		1.5		1.5		ns	
CKE setup time (Power down exit)		t_{CKSP}	2.5		3		3		ns	
Command (/CS0, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t_{CMS}	2.5		3		3		ns	
Command (/CS0, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t_{CMH}	1		1.5		1.5		ns	

Note 1. Output load



★ **Asynchronous Characteristics**

Parameter		Symbol	-A10		-A67		-A12		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period		t_{RC}	100		105		102		ns	
ACT to PRE command period		t_{RAS}	60	120,000	75	120,000	72	120,000	ns	
PRE to ACT command period		t_{RP}	30		30		30		ns	
Delay time ACT to READ/WRITE command		t_{RCD}	30		30		30		ns	
ACT(0) to ACT(1) command period		t_{RRD}	20		30		24		ns	
Data-in to PRE command period		t_{DPL}	10		15		12		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t_{DAL3}	2CLK+ 30		2CLK+ 30		2CLK+ 30		ns	
	/CAS latency = 2	t_{DAL2}	1CLK+ 30		1CLK+ 30		1CLK+ 30		ns	
Mode register set cycle time		t_{RSC}	20		20		20		ns	
Transition time		t_T	1	30	1	30	1	30	ns	
Refresh time		t_{REF}		32		32		32	ms	1

Note 1. 2,048 rows

★ **Serial PD**(1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows		0BH	0	0	0	0	1	0	1	1	11 rows
4	Number of columns		08H	0	0	0	0	1	0	0	0	8 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		40H	0	1	0	0	0	0	0	0	64 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTL
9	CL = 3 Cycle time	(-A10)	A0H	1	0	1	0	0	0	0	0	10 ns
		(-A67)	F0H	1	1	1	1	0	0	0	0	15 ns
		(-A12)	C0H	1	1	0	0	0	0	0	0	12 ns
10	CL =3 Access time	(-A10)	80H	1	0	0	0	0	0	0	0	8 ns
		(-A67)	90H	1	0	0	1	0	0	0	0	9 ns
		(-A12)	90H	1	0	0	1	0	0	0	0	9 ns
11	DIMM configuration type		00H	0	0	0	0	0	0	0	0	None
12	Refresh rate/type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		10H	0	0	0	1	0	0	0	0	×16
14	Error checking SDRAM width		00H	0	0	0	0	0	0	0	0	None
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM		02H	0	0	0	0	0	0	1	0	2 banks
18	/CAS latency supported		06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes		00H	0	0	0	0	0	0	0	0	
22	SDRAM device attributes : General		0EH	0	0	0	0	1	1	1	0	
23	CL = 2 Cycle time	(-A10)	F0H	1	1	1	1	0	0	0	0	15 ns
		(-A67)	F0H	1	1	1	1	0	0	0	0	15 ns
		(-A12)	30H	0	0	1	1	0	0	0	0	18 ns
24	CL = 2 Access time	(-A10)	A0H	1	0	1	0	0	0	0	0	10 ns
		(-A67)	A0H	1	0	1	0	0	0	0	0	10 ns
		(-A12)	C0H	1	1	0	0	0	0	0	0	12 ns
25-26			00H	0	0	0	0	0	0	0	0	
27	$t_{RP(MIN.)}$	(-A10)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A67)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A12)	1EH	0	0	0	1	1	1	1	0	30 ns
28	$t_{RRD(MIN.)}$	(-A10)	14H	0	0	0	1	0	1	0	0	20 ns
		(-A67)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A12)	18H	0	0	0	1	1	0	0	0	24 ns
29	$t_{RCD(MIN.)}$	(-A10)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A67)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A12)	1EH	0	0	0	1	1	1	1	0	30 ns
30	$t_{RAS(MIN.)}$	(-A10)	3CH	0	0	1	1	1	1	0	0	60 ns
		(-A67)	4BH	0	1	0	0	1	0	1	1	75 ns
		(-A12)	48H	0	1	0	0	1	0	0	0	72 ns
31	Module bank density		02H	0	0	0	0	0	0	1	0	8M bytes

★ **Serial PD**(2/2)

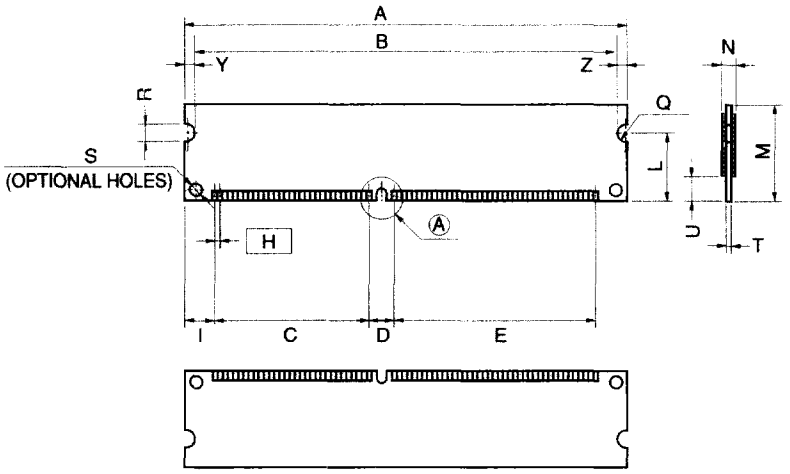
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32-61			00H	0	0	0	0	0	0	0	0	
62	SPD revision		01H	0	0	0	0	0	0	0	1	1
63	Checksum for bytes 0 - 62	(-A10)	58H	0	1	0	1	1	0	0	0	
		(-A67)	D1H	1	1	0	1	0	0	0	1	
		(-A12)	F8H	1	1	1	1	1	0	0	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-126	Mfg specific											
126	Intel specification frequency		66H	0	1	1	0	0	1	1	0	66 MHz
127	Intel specification /CAS latency support		06H	0	0	0	0	0	1	1	0	2, 3

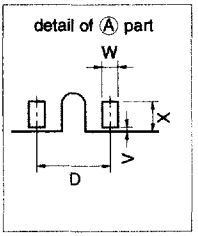
Timing Chart

Please refer to the attached timing chart 1 (p.411).

Package Drawing

144 PIN SMALL OUTLINE DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS
A	67.45 ~ 67.75
B	63.6
C	23.2 ± 0.05
D	4.6 ± 0.05
E	32.8 ± 0.05
H	0.8 (T.P.)
I	3.3
L	20.0
M	25.4 ± 0.15
N	3.8 (MAX.)
Q	R2
R	4.0 ± 0.1
S	1.8
T	0.9 ~ 1.1
U	3.2
V	0.25 (MAX.)
W	0.6 ± 0.05
X	2.55 (MIN.)
Y	2.0 (MIN.)
Z	2.0 (MIN.)