FUJITSU SEMICONDUCTOR
DATA SHEET

DS704-00003-0v01-E

16-bit Proprietary Microcontroller

CMOS

F²MC-16FX MB96650 Series

MB96F656/F657*

■ DESCRIPTION

MB96650 series is based on FUJITSU's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products.
16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For high processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 32MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 31.2ns going together with excellent EMI behavior. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows selecting suitable operation frequencies for peripheral resources independent of the CPU speed.

*: These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

For the information for microcontroller supports, see the following website.

http://edevice.fujitsu.com/micom/en-support/

2011.7

■ FEATURES

● Technology

- 0.18µm CMOS

● CPU

- F^2MC-16FX CPU
- Optimized instruction set for controller applications
  (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, variety of pointers)
- 8-byte instruction execution queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

● System clock

- On-chip PLL clock multiplier (×1 to ×8, ×1 when PLL stop)
- 4 MHz to 8 MHz external crystal oscillator clock
  (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 16 MHz external clock for devices with fast clock input feature
- 32.768 kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
- Clock source selectable from mainclock oscillator, subclock oscillator and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals
- The subclock oscillator is enabled by the Boot ROM program controlled by a configuration marker after a Power or External reset
- Low Power Consumption - 13 operating modes (different Run, Sleep, Timer modes, Stop mode)

● On-chip voltage regulator

- Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures

● Low voltage reset

- Reset is generated when supply voltage is below minimum

● Code Security

- Protects Flash Memory content from unintended read-out

● DMA

- Automatic transfer function independent of CPU, can be assigned freely to resources

● Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

I^2C

- Up to 400 kbps
- Master and Slave functionality, 7-bit and 10-bit addressing

A/D converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function
- Scan Disable Function

Source Clock Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising&falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as 2 × 8-bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture
- Start delay

Quadrature Position/Revolution Counter (QPRC)

- Edge count mode, Phase count mode, Level count mode
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

Real Time Clock

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge or Level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I^2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GP-IO-pin (either Automotive or CMOS-Schmitt trigger)
- Bit-wise programmable pull-up resistor

● Built-in OCD (On Chip Debugger)

- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - Data event: 6 points
  - Event sequencer: 2 levels
- Execution time measurement function
- Trace function: 42 branches
- Security function

● Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

■ PRODUCT LINEUP

Features			MB96F65x	Remark
Product type			Flash product	
Subclock			Subclock can be set by software	
Dual Operation Flash memory		RAM		
256.5KB + 32KB		24KB	MB96F656	
384.5KB + 32KB		28KB	MB96F657	
Package			LQFP-120 FPT-120P-M21	
DMA			4ch	
USART			6ch	LIN-USART 0/1/2/4/5/7
	with automatic LIN-Header transmisstion/reception		Yes (only 1ch)	LIN-USART 0
	with 16 byte RX- and TX-FIFO		No	
I^2C			2ch	I^2C 0/1
10-bit A/D Converter			29ch	AN 0 to 28
	with Data Buffer		No	
	with Range Comparator		Yes	
	with Scan Disable		Yes	
	with ADC Pulse Detection		No	
16-bit Reload Timer (RLT)			5ch	RLT 0/1/2/3/6 Only RLT6 can be used as PPG clock source.
16-bit Free-Running Timer (FRT)			3ch	FRT 0/1/2
16-bit Input Capture Unit (ICU)			7ch (1 channels for LIN-USART)	ICU 0/1/4/5/6/7/9 ICU 9 for LIN-USART
16-bit Output Compare Unit (OCU)			7ch	OCU 0/1/2/3/4/6/7 (OCU 4 for FRT clear)
8/16-bit Programmable Pulse Generator (PPG)			16ch (16-bit) / 32ch (8-bit)	PPG 0 to 15
	with Timing point capture		Yes	
	with Start delay		Yes	
	with Ramp		No	
Quadrature position/revolution counter (QPRC)			2ch	QPRC 0/1
CAN Interface			1ch	CAN 0 32 Message Buffers
External Interrupts (INTerrupt)			16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)			1ch	
Real Time Clock (RTC)			1ch	
I/O Ports			99 (Dual clock mode) 101 (Single clock mode)	
Clock Calibration Unit (CAL)			1ch	
Clock Output Function			2ch	
Low Voltage Reset			Yes	Low voltage reset can be disabled by software
Hardware Watchdog Timer			Yes	
On-chip RC-oscillator			Yes	
On-chip Debugger			Yes	

Notes: ・ All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use.

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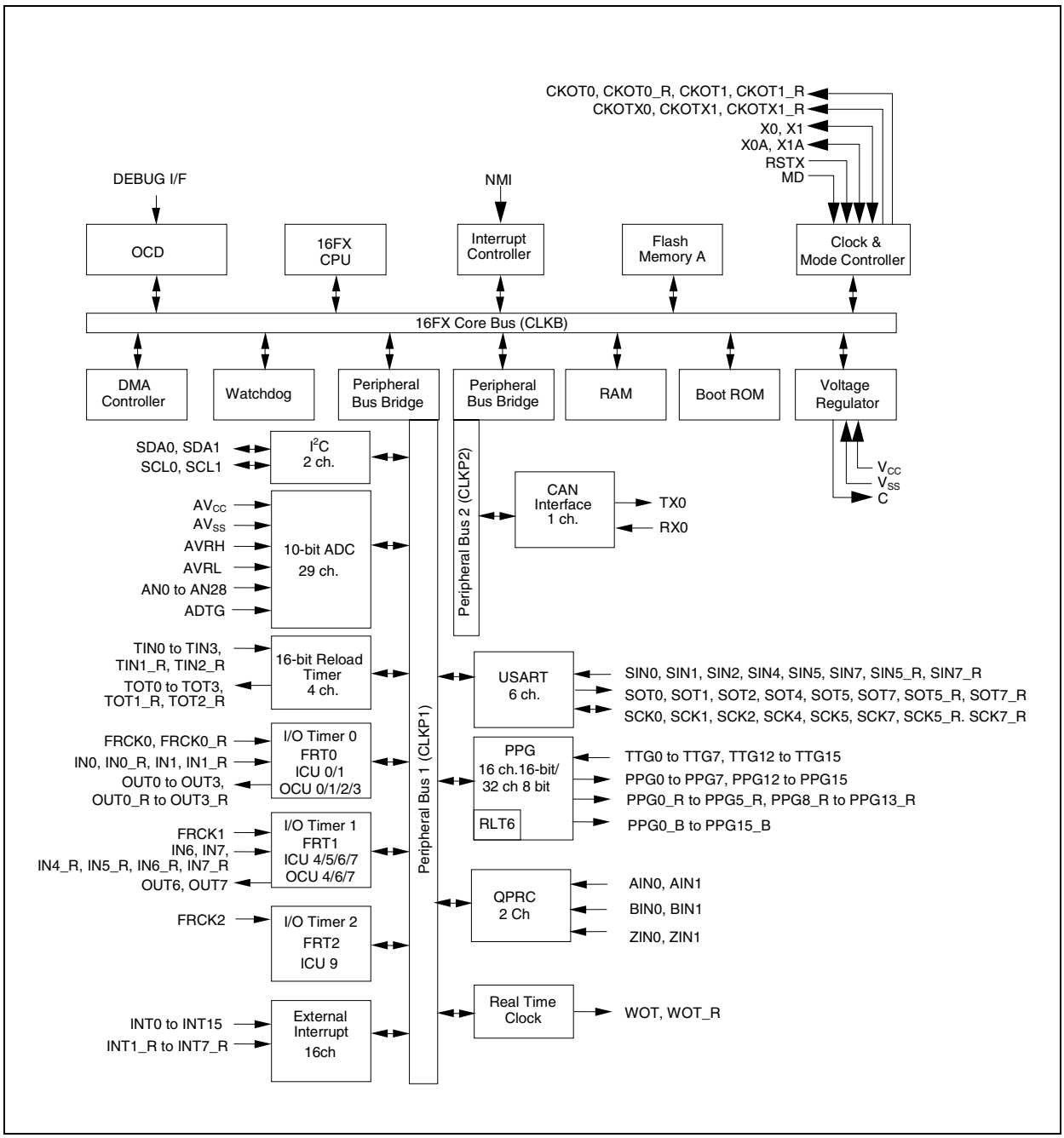
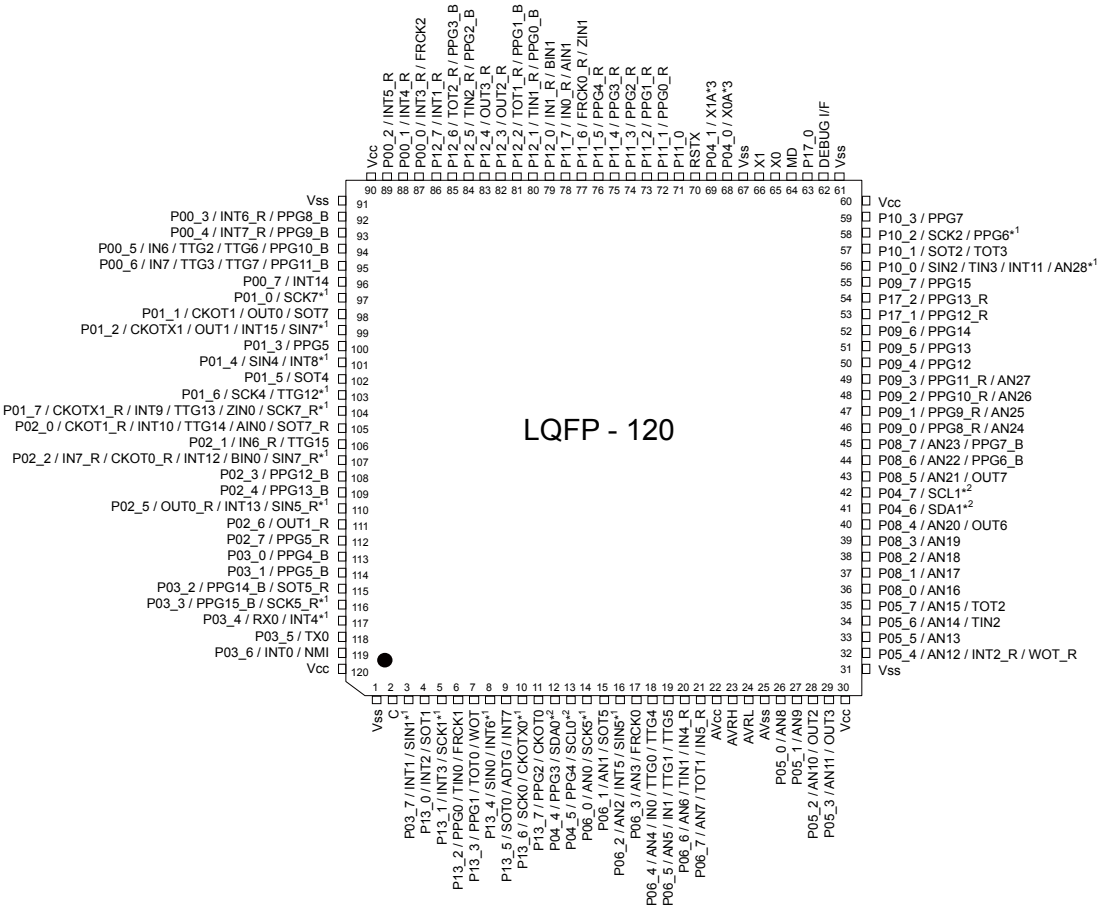
These products under development may change its specification without notice.

■ BLOCK DIAGRAM



■ PIN ASSIGNMENTS

(Top view)



(FPT-120P-M21)

*1: CMOS input level only
*2: CMOS input level only for I^2C
*3: Please set Rom Configuration Block (RCB) to use the subclock
All other general-purpose pins have only Automotive input level.

■ PIN FUNCTION DESCRIPTION

Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input
ANn	ADC	A/D converter channel n input
AVcc	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AVss	Supply	Analog circuits power supply
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input
Pnn_m	GPIO	General purpose I/O
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
PPGn	PPG	Programmable Pulse Generator n output (16bit/8bit)
PPGn_R	PPG	Relocated Programmable Pulse Generator n output (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output (8bit)
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I^2C	I^2C interface n clock I/O input/output
SDAn	I^2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOT_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
Vcc	Supply	Power supply

Pin name	Feature	Description
Vss	Supply	Power supply
WOT	RTC	Real Time clock output
WOT_R	RTC	Relocated Real Time clock output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input
DEBUG I/F	OCD	On Chip Debugger input/output

■ PIN CIRCUIT TYPE

Pin no.	I/O circuit type*	Pin name
1	Supply	Vss
2	F	C
3	M	P03_7 / INT1 / SIN1
4	H	P13_0 / INT2 / SOT1
5	M	P13_1 / INT3 / SCK1
6	H	P13_2 / PPG0 / TIN0 / FRCK1
7	H	P13_3 / PPG1 / TOT0 / WOT
8	M	P13_4 / SIN0 / INT6
9	H	P13_5 / SOT0 / ADTG / INT7
10	M	P13_6 / SCK0 / CKOTX0
11	H	P13_7 / PPG2 / CKOT0
12	N	P04_4 / PPG3 / SDA0
13	N	P04_5 / PPG4 / SCL0
14	I	P06_0 / AN0 / SCK5
15	K	P06_1 / AN1 / SOT5
16	I	P06_2 / AN2 / INT5 / SIN5
17	K	P06_3 / AN3 / FRCK0
18	K	P06_4 / AN4 / IN0 / TTG0 / TTG4
19	K	P06_5 / AN5 / IN1 / TTG1 / TTG5
20	K	P06_6 / AN6 / TIN1 / IN4_R
21	K	P06_7 / AN7 / TOT1 / IN5_R
22	Supply	AVcc
23	G	AVRH
24	G	AVRL
25	Supply	AVss
26	K	P05_0 / AN8
27	K	P05_1 / AN9
28	K	P05_2 / AN10 / OUT2
29	K	P05_3 / AN11 / OUT3
30	Supply	Vcc
31	Supply	Vss
32	K	P05_4 / AN12 / INT2_R / WOT_R
33	K	P05_5 / AN13
34	K	P05_6 / AN14 / TIN2
35	K	P05_7 / AN15 / TOT2

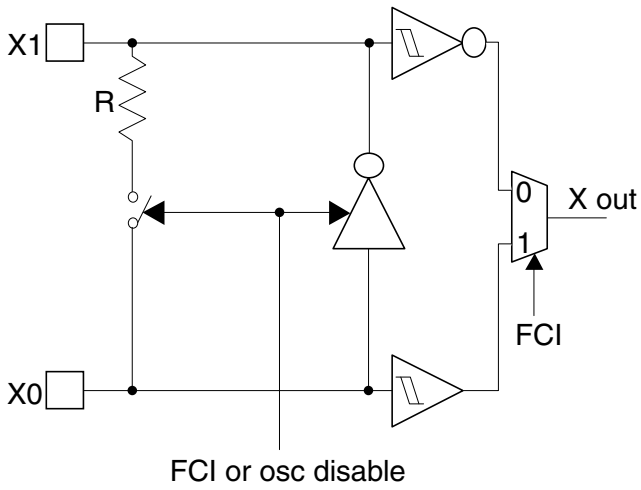
Pin no.	I/O circuit type*	Pin name
36	K	P08_0 / AN16
37	K	P08_1 / AN17
38	K	P08_2 / AN18
39	K	P08_3 / AN19
40	K	P08_4 / AN20 / OUT6
41	N	P04_6 / SDA1
42	N	P04_7 / SCL1
43	K	P08_5 / AN21 / OUT7
44	K	P08_6 / AN22 / PPG6_B
45	K	P08_7 / AN23 / PPG7_B
46	K	P09_0 / AN24 / PPG8_R
47	K	P09_1 / AN25 / PPG9_R
48	K	P09_2 / AN26 / PPG10_R
49	K	P09_3 / AN27 / PPG11_R
50	H	P09_4 / PPG12
51	H	P09_5 / PPG13
52	H	P09_6 / PPG14
53	H	P17_1 / PPG12_R
54	H	P17_2 / PPG13_R
55	H	P09_7 / PPG15
56	I	P10_0 / SIN2 / TIN3 / AN28 / INT11
57	H	P10_1 / SOT2 / TOT3
58	M	P10_2 / SCK2 / PPG6
59	H	P10_3 / PPG7
60	Supply	Vcc
61	Supply	Vss
62	O	DEBUG I / F
63	H	P17_0
64	C	MD
65	A	X0
66	A	X1
67	Supply	Vss
68	B	P04_0 / X0A
69	B	P04_1 / X1A
70	C	RSTX

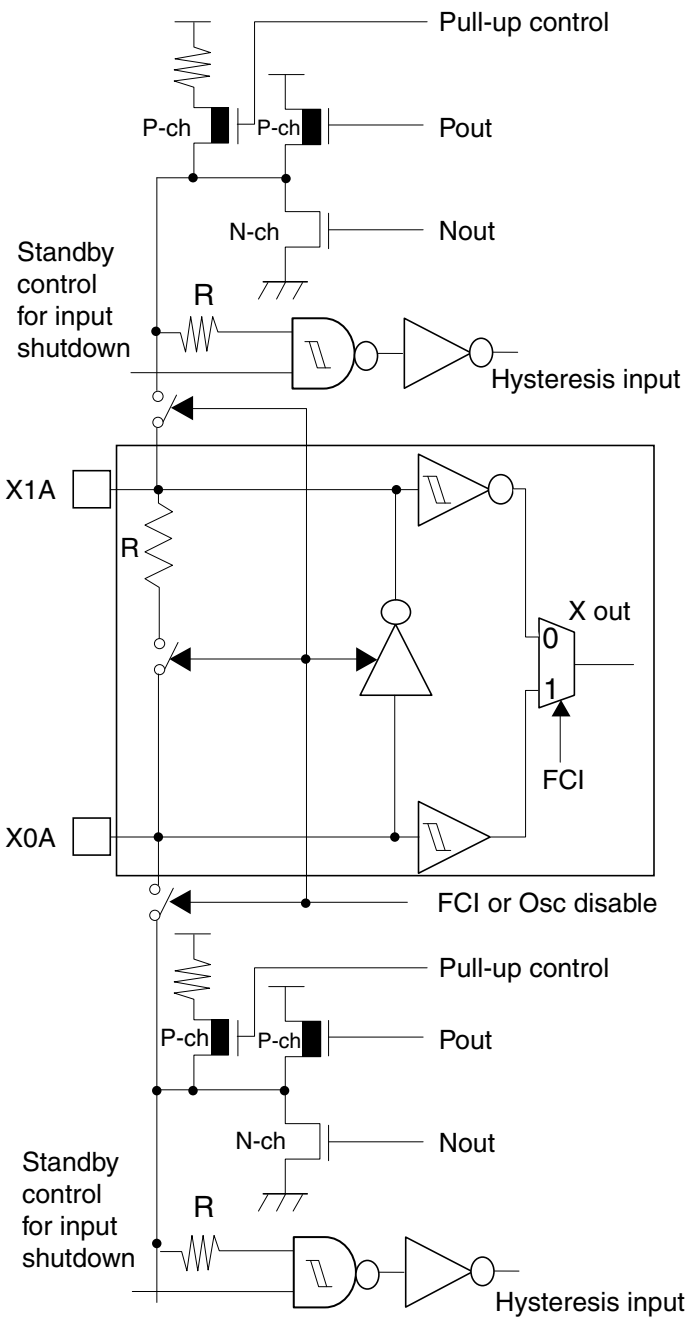
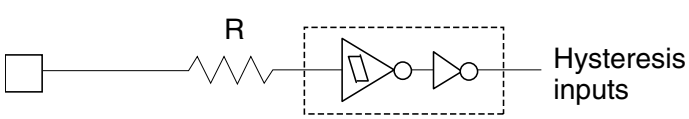
Pin no.	I/O circuit type*	Pin name
71	H	P11_0
72	H	P11_1 / PPG0_R
73	H	P11_2 / PPG1_R
74	H	P11_3 / PPG2_R
75	H	P11_4 / PPG3_R
76	H	P11_5 / PPG4_R
77	H	P11_6 / FRCK0_R / ZIN1
78	H	P11_7 / IN0_R / AIN1
79	H	P12_0 / IN1_R / BIN1
80	H	P12_1 / TIN1_R / PPG0_B
81	H	P12_2 / TOT1_R / PPG1_B
82	H	P12_3 / OUT2_R
83	H	P12_4 / OUT3_R
84	H	P12_5 / TIN2_R / PPG2_B
85	H	P12_6 / TOT2_R / PPG3_B
86	H	P12_7 / INT1_R
87	H	P00_0 / INT3_R / FRCK2
88	H	P00_1 / INT4_R
89	H	P00_2 / INT5_R
90	Supply	Vcc
91	Supply	Vss
92	H	P00_3 / INT6_R / PPG8_B
93	H	P00_4 / INT7_R / PPG9_B
94	H	P00_5 / IN6 / TTG2 / TTG6 / PPG10_B
95	H	P00_6 / IN7 / TTG3 / TTG7 / PPG11_B
96	H	P00_7 / INT14
97	M	P01_0 / SCK7
98	H	P01_1 / CKOT1 / OUT0 / SOT7
99	M	P01_2 / CKOTX1 / OUT1 / INT15 / SIN7
100	H	P01_3 / PPG5
101	M	P01_4 / SIN4 / INT8
102	H	P01_5 / SOT4
103	M	P01_6 / SCK4 / TTG12
104	M	P01_7 / CKOTX1_R / INT9 / TTG13 / ZIN0 / SCK7_R
105	H	P02_0 / CKOT1_R / INT10 / TTG14 / AIN0 / SOT7_R

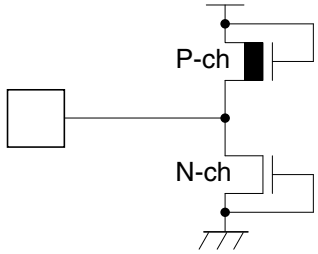
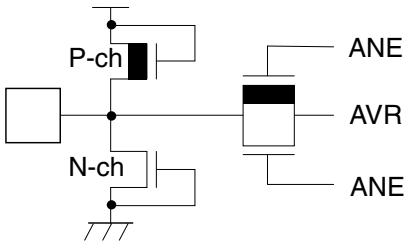
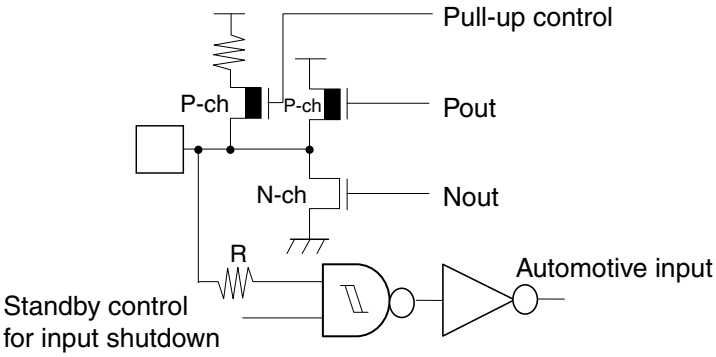
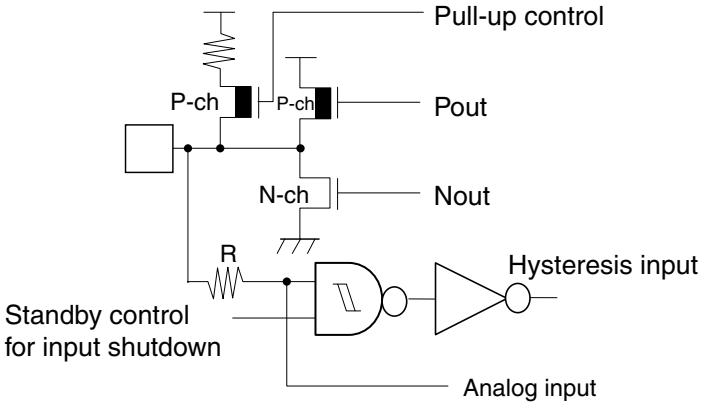
Pin no.	I/O circuit type*	Pin name
106	H	P02_1 / IN6_R / TTG15
107	M	P02_2 / IN7_R / CKOT0_R / INT12 / BIN0 / SIN7_R
108	H	P02_3 / PPG12_B
109	H	P02_4 / PPG13_B
110	M	P02_5 / OUT0_R / INT13 / SIN5_R
111	H	P02_6 / OUT1_R
112	H	P02_7 / PPG5_R
113	H	P03_0 / PPG4_B
114	H	P03_1 / PPG5_B
115	H	P03_2 / PPG14_B / SOT5_R
116	M	P03_3 / PPG15_B / SCK5_R
117	M	P03_4 / RX0 / INT4
118	H	P03_5 / TX0
119	H	P03_6 / INT0 / NMI
120	Supply	Vcc

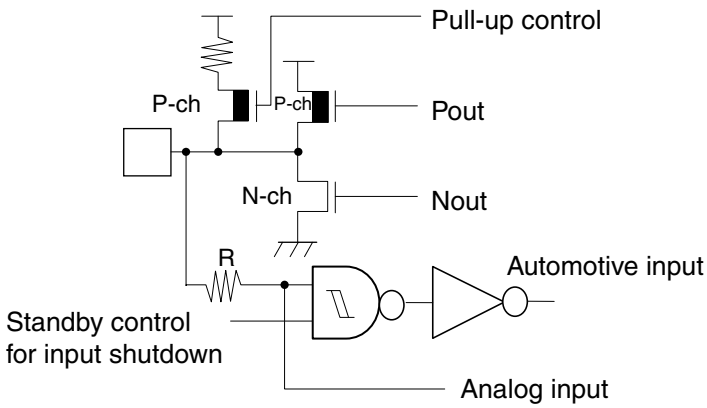
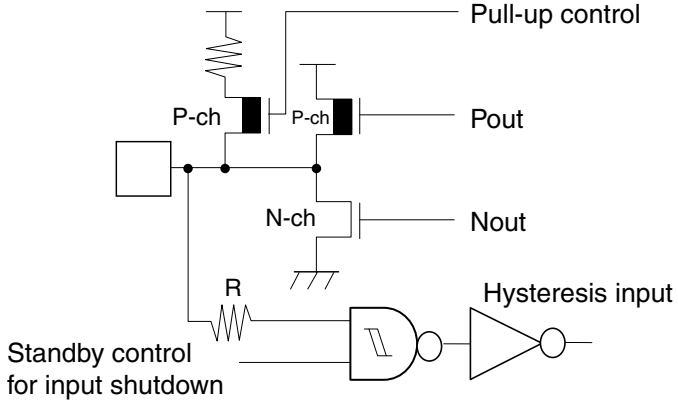
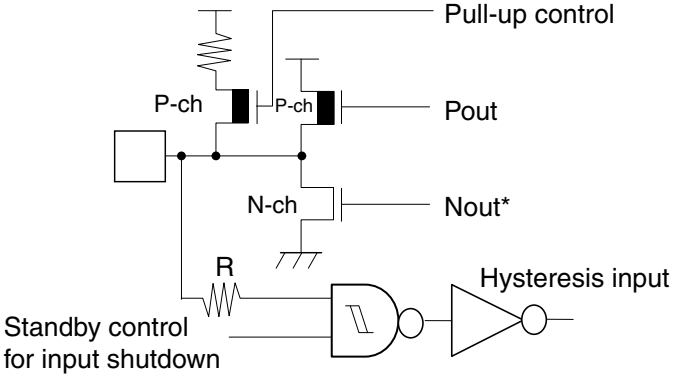
*: Please refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.

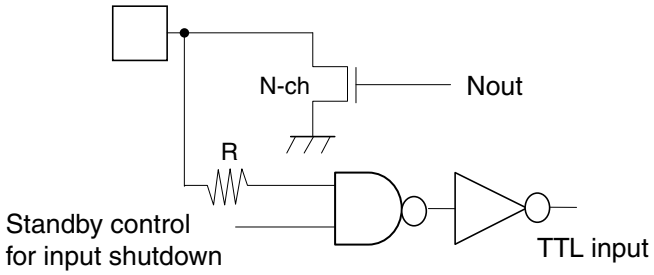
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: · Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) · Feedback resistor = approx. 1.0 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode · The amplitude: 1.8V±0.15V to operate by the internal supply voltage

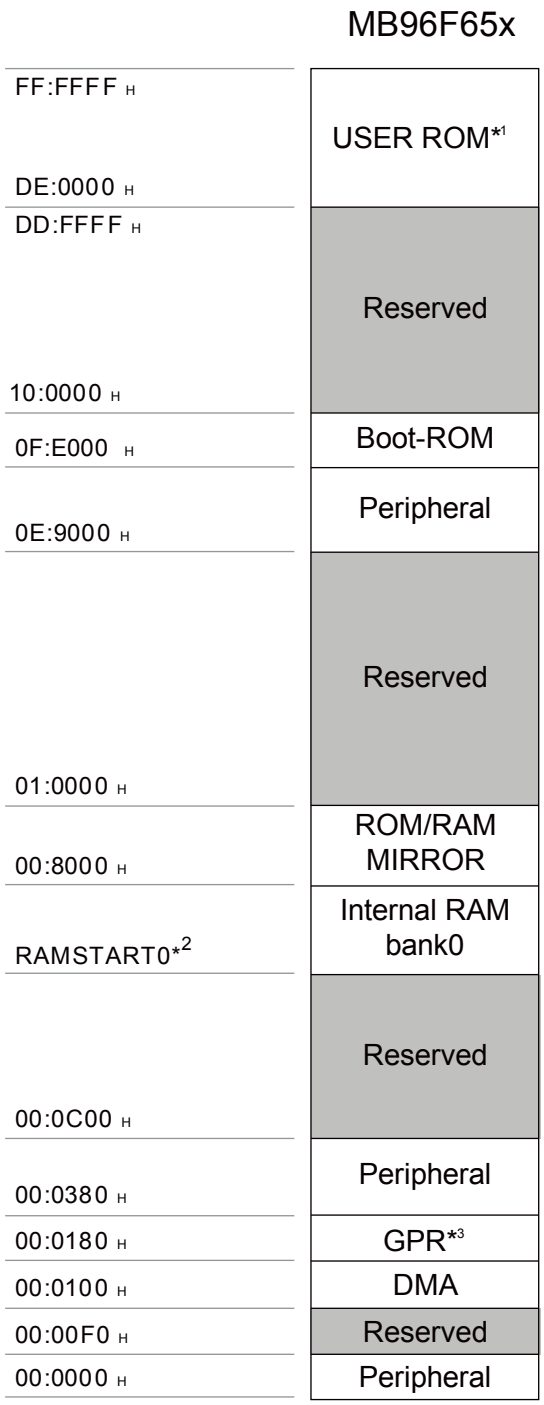
Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled • GPIO functionality selectable (CMOS hysteresis input with input shutdown function, I_{OL} = 4mA, I_{OH} = -4mA, Programmable pull-up resistor)
C		• CMOS hysteresis input pin

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH
H		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor
I		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor • Analog input

Type	Circuit	Remarks
K		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input
M		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.

Type	Circuit	Remarks
O		• I_{OL}: 25mA @ 2.7V • TTL input

■ MEMORY MAP



*1: For details about USER ROM area, see the "■USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.
*2: For RAMSTART/END addresses, please refer to the table on the next page.
*3: Unused GPR banks can be used as RAM area.

The DMA area is only available if the device contains the corresponding resource.
The available RAM and ROM area depends on the device.

■ RAMSTART ADDRESSES

Devices	Bank 0 RAM size	RAMSTART0
MB96F656	24KByte	$00:2200_H$
MB96F657	28KByte	$00:1200_H$

■ USER ROM MEMORY MAP FOR FLASH DEVICES

Alternative mode CPU address	Flash memory mode address	MB96F656 Flash size 256.5KB + 32KB	MB96F657 Flash size 384.5KB + 32KB	
FF:FFFF$_H$	3F:FFFF$_H$	SA39-64KB	SA39-64KB	Bank A of Flash A
FF:0000$_H$	3F:0000$_H$			
FE:FFFF$_H$	3E:FFFF$_H$	SA38-64KB	SA38-64KB	
FE:0000$_H$	3E:0000$_H$			
FD:FFFF$_H$	3D:FFFF$_H$	SA37-64KB	SA37-64KB	
FD:0000$_H$	3D:0000$_H$			
FC:FFFF$_H$	3C:FFFF$_H$	SA36-64KB	SA36-64KB	
FC:0000$_H$	3C:0000$_H$			
FB:FFFF$_H$	3B:FFFF$_H$	Reserved	SA35-64KB	
FB:0000$_H$	3B:0000$_H$			
FA:FFFF$_H$	3A:FFFF$_H$		SA34-64KB	
FA:0000$_H$	3A:0000$_H$			
F9:FFFF$_H$	39:FFFF$_H$		Reserved	
DF:A000$_H$	1F:A000$_H$			
DF:9FFF$_H$	1F:9FFF$_H$	SA4-8KB	SA4-8KB	Bank B of Flash A
DF:8000$_H$	1F:8000$_H$			
DF:7FFF$_H$	1F:7FFF$_H$	SA3-8KB	SA3-8KB	
DF:6000$_H$	1F:6000$_H$			
DF:5FFF$_H$	1F:5FFF$_H$	SA2-8KB	SA2-8KB	
DF:4000$_H$	1F:4000$_H$			
DF:3FFF$_H$	1F:3FFF$_H$	SA1-8KB	SA1-8KB	
DF:2000$_H$	1F:2000$_H$			
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SAS-512B*	SAS-512B*	Bank A of Flash A
DE:FFFF$_H$ DE:0000$_H$	1E:FFFF$_H$	Reserved	Reserved	

*: Phiysical address area of SAS-512B is from DF:0000$_H$ to DF:01FF$_H$.
Others (from DF:0200$_H$ to DF:1FFF$_H$) are all ROM Mirror area for SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address DF:0000$_H$ -DF:01FF$_H$.
SAS can not be used for E^2PROM emulation.

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96F65x		
Pin Number	USART Number	Normal Function
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
56	USART2	SIN2
57		SOT2
58		SCK2
101	USART4	SIN4
102		SOT4
103		SCK4

■ INTERRUPT VECTOR TABLE

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC	CALLV0	No	-	Reserved
1	3F8	CALLV1	No	-	Reserved
2	3F4	CALLV2	No	-	Reserved
3	3F0	CALLV3	No	-	Reserved
4	3EC	CALLV4	No	-	Reserved
5	3E8	CALLV5	No	-	Reserved
6	3E4	CALLV6	No	-	Reserved
7	3E0	CALLV7	No	-	Reserved
8	3DC	RESET	No	-	Reserved
9	3D8	INT9	No	-	Reserved
10	3D4	EXCEPTION	No	-	Reserved
11	3D0	NMI	No	-	Non-Maskable Interrupt
12	3CC	DLY	No	12	Delayed Interrupt
13	3C8	RC_TIMER	No	13	RC clock timer
14	3C4	MC_TIMER	No	14	Main Clock Timer
15	3C0	SC_TIMER	No	15	Sub Clock Timer
16	3BC	LVDI	No	16	Low Voltage Detector
17	3B8	EXTINT0	Yes	17	External Interrupt 0
18	3B4	EXTINT1	Yes	18	External Interrupt 1
19	3B0	EXTINT2	Yes	19	External Interrupt 2
20	3AC	EXTINT3	Yes	20	External Interrupt 3
21	3A8	EXTINT4	Yes	21	External Interrupt 4
22	3A4	EXTINT5	Yes	22	External Interrupt 5
23	3A0	EXTINT6	Yes	23	External Interrupt 6
24	39C	EXTINT7	Yes	24	External Interrupt 7
25	398	EXTINT8	Yes	25	External Interrupt 8
26	394	EXTINT9	Yes	26	External Interrupt 9
27	390	EXTINT10	Yes	27	External Interrupt 10
28	38C	EXTINT11	Yes	28	External Interrupt 11
29	388	EXTINT12	Yes	29	External Interrupt 12
30	384	EXTINT13	Yes	30	External Interrupt 13
31	380	EXTINT14	Yes	31	External Interrupt 14
32	37C	EXTINT15	Yes	32	External Interrupt 15
33	378	CAN0	No	33	CAN Controller 0
34	374	-	-	34	Reserved
35	370	-	-	35	Reserved
36	36C	-	-	36	Reserved
37	368	-	-	37	Reserved
38	364	PPG0	Yes	38	Programmable Pulse Generator 0
39	360	PPG1	Yes	39	Programmable Pulse Generator 1
40	35C	PPG2	Yes	40	Programmable Pulse Generator 2

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
41	358	PPG3	Yes	41	Programmable Pulse Generator 3
42	354	PPG4	Yes	42	Programmable Pulse Generator 4
43	350	PPG5	Yes	43	Programmable Pulse Generator 5
44	34C	PPG6	Yes	44	Programmable Pulse Generator 6
45	348	PPG7	Yes	45	Programmable Pulse Generator 7
46	344	PPG8	Yes	46	Programmable Pulse Generator 8
47	340	PPG9	Yes	47	Programmable Pulse Generator 9
48	33C	PPG10	Yes	48	Programmable Pulse Generator 10
49	338	PPG11	Yes	49	Programmable Pulse Generator 11
50	334	PPG12	Yes	50	Programmable Pulse Generator 12
51	330	PPG13	Yes	51	Programmable Pulse Generator 13
52	32C	PPG14	Yes	52	Programmable Pulse Generator 14
53	328	PPG15	Yes	53	Programmable Pulse Generator 15
54	324	-	-	54	Reserved
55	320	-	-	55	Reserved
56	31C	-	-	56	Reserved
57	318	-	-	57	Reserved
58	314	RLT0	Yes	58	Reload Timer 0
59	310	RLT1	Yes	59	Reload Timer 1
60	30C	RLT2	Yes	60	Reload Timer 2
61	308	RLT3	Yes	61	Reload Timer 3
62	304	-	-	62	Reserved
63	300	-	-	63	Reserved
64	2FC	PPGRLT	Yes	64	Reload Timer 6 can be used as PPG clock source
65	2F8	ICU0	Yes	65	Input Capture Unit 0
66	2F4	ICU1	Yes	66	Input Capture Unit 1
67	2F0	-	-	67	Reserved
68	2EC	-	-	68	Reserved
69	2E8	ICU4	Yes	69	Input Capture Unit 4
70	2E4	ICU5	Yes	70	Input Capture Unit 5
71	2E0	ICU6	Yes	71	Input Capture Unit 6
72	2DC	ICU7	Yes	72	Input Capture Unit 7
73	2D8	-	-	73	Reserved
74	2D4	ICU9	Yes	74	Input Capture Unit 9
75	2D0	-	-	75	Reserved
76	2CC	-	-	76	Reserved
77	2C8	OCU0	Yes	77	Output Compare Unit 0
78	2C4	OCU1	Yes	78	Output Compare Unit 1
79	2C0	OCU2	Yes	79	Output Compare Unit 2
80	2BC	OCU3	Yes	80	Output Compare Unit 3

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	2B8	OCU4	Yes	81	Output Compare Unit 4
82	2B4	-	-	82	Reserved
83	2B0	OCU6	Yes	83	Output Compare Unit 6
84	2AC	OCU7	Yes	84	Output Compare Unit 7
85	2A8	-	-	85	Reserved
86	2A4	-	-	86	Reserved
87	2A0	-	-	87	Reserved
88	29C	-	-	88	Reserved
89	298	FRT0	Yes	89	Free Running Timer 0
90	294	FRT1	Yes	90	Free Running Timer 1
91	290	FRT2	Yes	91	Free Running Timer 2
92	28C	-	-	92	Reserved
93	288	RTC0	No	93	Real Time Clock
94	284	CAL0	No	94	Clock Calibration Unit
95	280	-	-	95	Reserved
96	27C	IIC0	Yes	96	I^2C interface0
97	278	IIC1	Yes	97	I^2C interface1
98	274	ADC0	Yes	98	A/D Converter
99	270	-	-	99	Reserved
100	26C	-	-	100	Reserved
101	268	LINR0	Yes	101	LIN USART 0 RX
102	264	LINT0	Yes	102	LIN USART 0 TX
103	260	LINR1	Yes	103	LIN USART 1 RX
104	25C	LINT1	Yes	104	LIN USART 1 TX
105	258	LINR2	Yes	105	LIN USART 2 RX
106	254	LINT2	Yes	106	LIN USART 2 TX
107	250	-	-	107	Reserved
108	24C	-	-	108	Reserved
109	248	LINR4	Yes	109	LIN USART 4 RX
110	244	LINT4	Yes	110	LIN USART 4 TX
111	240	LINR5	Yes	111	LIN USART 5 RX
112	23C	LINT5	Yes	112	LIN USART 5 TX
113	238	-	-	113	Reserved
114	234	-	-	114	Reserved
115	230	LINR7	Yes	115	LIN USART 7 RX
116	22C	LINT7	Yes	116	LIN USART 7 TX
117	228	-	-	117	Reserved
118	224	-	-	118	Reserved
119	220	-	-	119	Reserved
120	21C	-	-	120	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218	-	-	121	Reserved
122	214	-	-	122	Reserved
123	210	-	-	123	Reserved
124	20C	-	-	124	Reserved
125	208	-	-	125	Reserved
126	204	-	-	126	Reserved
127	200	-	-	127	Reserved
128	1FC	-	-	128	Reserved
129	1F8	-	-	129	Reserved
130	1F4	-	-	130	Reserved
131	1F0	-	-	131	Reserved
132	1EC	-	-	132	Reserved
133	1E8	FLASHA	Yes	133	Flash memory A interrupt
134	1E4	-	-	134	Reserved
135	1E0	-	-	135	Reserved
136	1DC	-	-	136	Reserved
137	1D8	QPRC0	Yes	137	Quad Possition/Revolution counter 0
138	1D4	QPRC1	Yes	138	Quad Possition/Revolution counter 1
139	1D0	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	1CC	-	-	140	Reserved
141	1C8	-	-	141	Reserved
142	1C4	-	-	142	Reserved
143	1C0	-	-	143	Reserved

■ HANDLING DEVICES

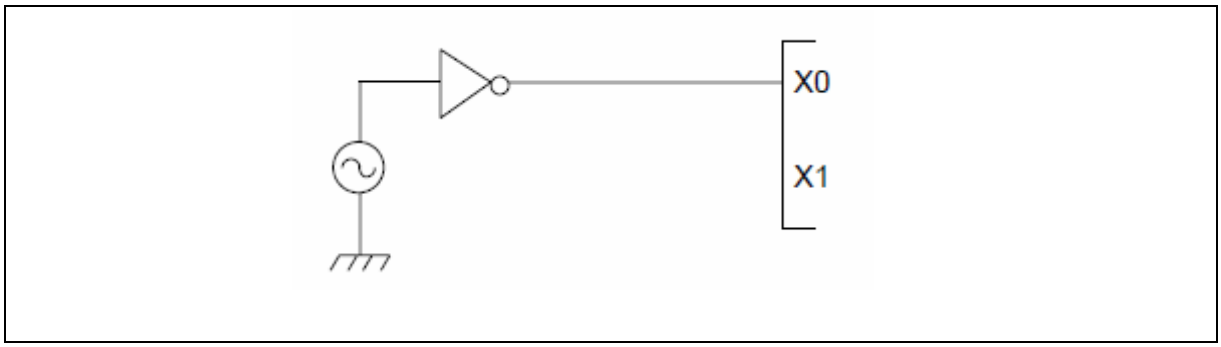
Special care is required for the following when handling the device:
• Latch-up prevention
• Unused pins handling
• External clock usage
• Notes on PLL clock mode operation
• Power supply pins (V_{CC}/V_{SS})
• Crystal oscillator circuit
• Turn on sequence of power supply to A/D converter and analog inputs
• Pin handling when not using the A/D converter
• Notes on Power-on
• Stabilization of power supply voltage
• Serial communication

1. Latch-up prevention
CMOS IC chips may suffer latch-up under the following conditions:
• A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
• A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
• The AV_{CC} power supply is applied before the V_{CC} voltage.
Latch-up may increase the power supply current dramatically, causing thermal damages to the device.
For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Unused pins handling
Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).
Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage
The permitted frequency range of an external clock depends on the oscillator type and configuration.
See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock for Main oscillator
• When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open. And supply 1.8V power to the external clock.



2. Single phase external clock for Sub oscillator

- When using a single phase external clock for the Sub oscillator, 'External clock mode' must be selected and X0A/GP04_0 must be driven. X1A/GP04_1 must be configured as GPIO.

4. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

5. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.
V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.
As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between Vcc and Vss as close as possible to Vcc and Vss pins.

6. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.
It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.
It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

7. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH,AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.
It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

8. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

9. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

10. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 Hz to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

11. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	Vcc	-	Vss - 0.3	Vss + 6.0	V	
Analog power supply voltage*1	AVcc	-	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc*2
Analog reference voltage*1	AVRH, AVRL	-	Vss - 0.3	Vss + 6.0	V	$AV_{CC} \geq AVRH$, AVcc ≥ AVRL, AVRH >AVRL, AVRL≥ AV_{SS}
Input voltage*1	V_I	-	Vss - 0.3	Vss + 6.0	V	$V_I \leq V_{CC} + 0.3V$*3
Output voltage*1	V_O	-	Vss - 0.3	Vss + 6.0	V	$V_O \leq V_{CC} + 0.3V$*3
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins *4
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	-	33	mA	Applicable to general purpose I/O pins *4
"L" level maximum output current	I_{OL}	-	-	15	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	82	mA	
"L" level average overall output current	ΣI_{OLAV}	-	-	41	mA	
"H" level maximum output current	I_{OH}	-	-	-15	mA	
"H" level average output current	I_{OHAV}	-	-	-4	mA	
"H" level maximum overall output current	ΣI_{OH}	-	-	-82	mA	
"H" level average overall output current	ΣI_{OHAV}	-	-	-41	mA	
Power consumption*5	P_D	T_A=+125°C	-	446*6	mW	
Operating ambient temperature	T_A	-	-40	125*7	°C	
Storage temperature	T_{STG}	-	-55	150	°C	

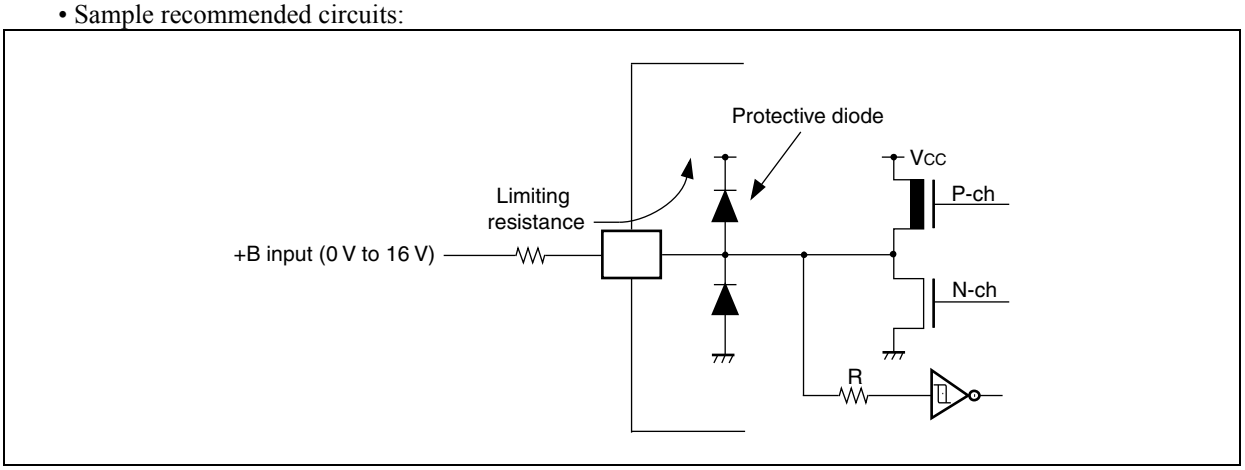
*1: This parameter is based on $V_{SS} = AV_{SS} = 0V$.

*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*4: • Applicable to all general purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +Binput is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

• Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*7: Flash Memory Write/Erase to Large Sector is guaranteed under Ta≦105℃.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	Vcc	2.7	-	5.5	V	
Smoothing capacitor at C pin	Cs	0.5	1.0	1.5	µF	(Target value) 1.0µF (Allowance within ± 50%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than Cs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

1. Current rating of MB96F650

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes*1	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	27	-	mA	T_A = +25°C
				-	-	37.5	mA	T_A = +105°C (Target value)
				-	-	39	mA	T_A = +125°C (Target value)
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	9	mA	T_A = +105°C (Target value)
				-	-	10.5	mA	T_A = +125°C (Target value)
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	6	mA	T_A = +105°C (Target value)
				-	-	7.5	mA	T_A = +125°C (Target value)
Power supply current in Sleep modes*1	I_{CCSPLL}		PLL Sleep mode with CLKS1/2 = CLKP1/2 = 32MHz (CLKRC and CLKSC stopped)	-	10	-	mA	T_A = +25°C
				-	-	15	mA	T_A = +105°C (Target value)
				-	-	16.5	mA	T_A = +125°C (Target value)
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKRC and CLKSC stopped)	-	1.0	-	mA	T_A = +25°C
				-	-	7	mA	T_A = +105°C (Target value)
				-	-	8.5	mA	T_A = +125°C (Target value)
	I_{CCSSUB}		Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz, (CLKMC, CLKPLL and CLKRC stopped)	-	0.08	-	mA	T_A = +25°C
				-	-	4	mA	T_A = +105°C (Target value)
				-	-	5.5	mA	T_A = +125°C (Target value)

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes*2	$I_{CCTMAIN}$	Vcc	Main Timer mode with CLKMC = 4MHz (CLKPLL, CLKRC and CLKSC stopped)	-	285	355	µA	T_A = +25°C
				-	-	1300	µA	T_A = +105°C (Target value)
				-	-	2310	µA	T_A = +125°C (Target value)
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz	-	160	245	µA	T_A = +25°C
				-	-	1215	µA	T_A = +105°C (Target value)
				-	-	2215	µA	T_A = +125°C (Target value)
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz	-	35	105	µA	T_A = +25°C
				-	-	1010	µA	T_A = +105°C (Target value)
				-	-	2015	µA	T_A = +125°C (Target value)
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	90	µA	T_A = +25°C
				-	-	985	µA	T_A = +105°C (Target value)
				-	-	1990	µA	T_A = +125°C (Target value)
Power supply current in Stop mode*3	I_{CCH}		-	-	20	90	µA	T_A = +25°C
				-	-	985	µA	T_A = +105°C (Target value)
				-	-	1985	µA	T_A = +125°C (Target value)
Power supply current for active Low Voltage detector*4	I_{CCLVD}		Low voltage detector enabled	-	5	15	µA	
Flash Write/ Erase current*5	$I_{CCFLASH}$		-	-	12.5	20	mA	

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control. Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode. The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.

*4: When low voltage detector is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

2. Pin characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	CMOS Hysteresis input
			-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "oscillation mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "oscillation mode"	Vcc × 0.8	-	Vcc + 0.3	V	
	V_{IHR}	RSTX	-	Vcc × 0.8	-	Vcc + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	Vcc - 0.3	-	Vcc + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	Vcc + 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	Vss - 0.3	-	V_{CC} × 0.3	V	CMOS Hysteresis input
			-	Vss - 0.3	-	V_{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "oscillation mode"	Vss	-	VD × 0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "oscillation mode"	Vss - 0.3	-	Vcc × 0.2	V	
	V_{ILR}	RSTX	-	Vss - 0.3	-	V_{CC} × 0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	Vss - 0.3	-	Vss + 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	Vss - 0.3	-	0.8	V	TTL Input
"H" level output voltage*	V_{OH4}	4mA type	4.5V ≤ Vcc ≤ 5.5V I_{OH} = -4mA 2.7V ≤ Vcc < 4.5V I_{OH} = -1.5mA	Vcc - 0.5	-	Vcc	V	
	V_{OH3}	3mA type	4.5V ≤ Vcc ≤ 5.5V I_{OH} = -3mA 2.7V ≤ Vcc < 4.5V I_{OH} = -1.5mA	Vcc - 0.5	-	Vcc	V	
"L" level output voltage*	V_{OL4}	4mA type	4.5V ≤ Vcc ≤ 5.5V I_{OL} = +4mA 2.7V ≤ Vcc < 4.5V I_{OL} = +1.7mA	-	-	0.4	V	
	V_{OL3}	3mA type	2.7V ≤ Vcc < 5.5V I_{OL} = +3mA	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	Vss < V_I < Vcc AVss,AVRL< V_I < AVcc, AVRH	- 1	-	1	µA	
Pull-up resistance value	R_{PU}	Pnn_m	Vcc = 5.0V ±10%	25	50	100	kΩ	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	Other than Vcc, Vss, AVcc, AVss, AVRH, AVRL	-	-	5	15	pF	

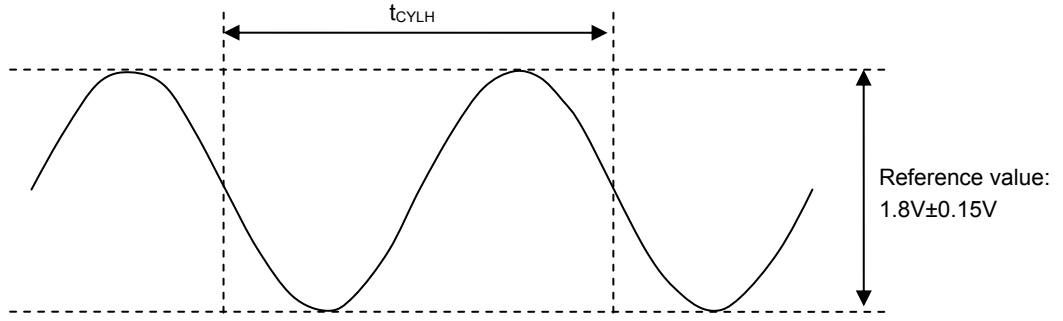
*: I_{OH} and I_{OL} are target value.

4. AC Characteristics

(1) Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			4	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Input clock cycle	t_{CYLH}	-	62.5	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	30	-	70	%	

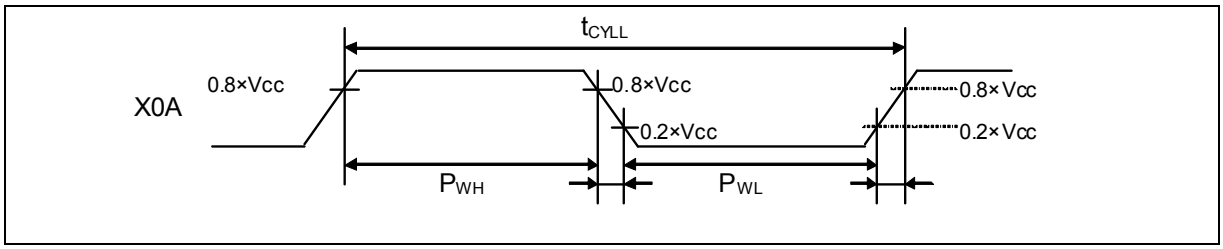


The amplitude changes by resistance, capacity which added outside or the difference of the device.

(2) Sub Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	When using an oscillation circuit
			-	-	-	100	kHz	When using an opposite phase external clock
		X0A	-	-	-	50	kHz	When using a single phase external clock
Input clock cycle	t_{CYLL}	-	-	10	-	-	µs	
Input clock pulse width	-	-	P_{WH}/t_{CYLL} P_{WL}/t_{CYLL}	30	-	70	%	



(3) Built-in RC Oscillation Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	F_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator

(4) Internal Clock timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clockfrequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

(5) Operating Conditions of PLL

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	1	-	4	ms	Time from when the PLL starts operating until the oscillation stabilizes
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL macro oscillation clock frequency	f_{PLLO}	56	-	108	MHz	

(6) Reset Input Characteristics

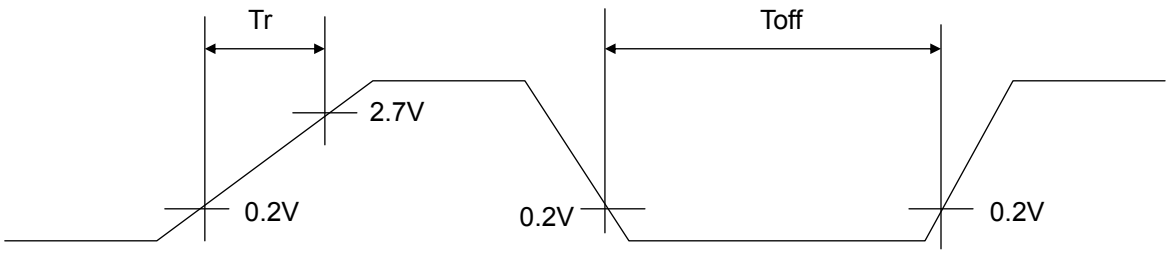
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	T_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs

(7) Power-on Reset Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power on rise time	Tr	0.05	-	30	ms
Power off time	Toff	1	-	-	ms



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

(8) USART Timing

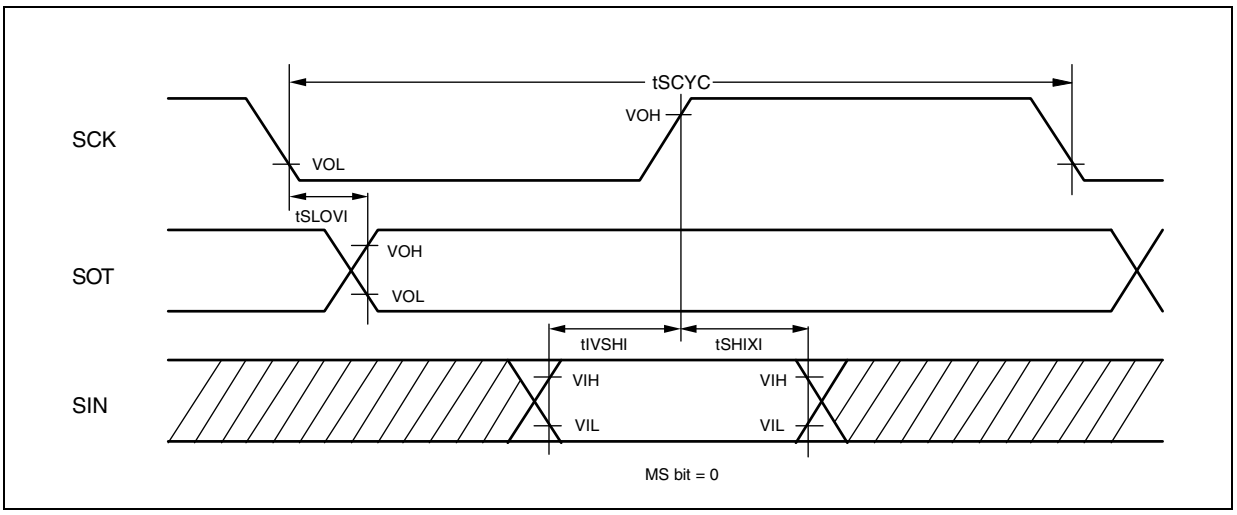
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	4.5V ≤ Vcc < 5.5V		2.7V ≤ Vcc < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCKn	Internal shift clock operation	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓ → SOT delay time	tSLOVI	SCKn SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	tOVSHI	SCKn SOTn		N×t_{CLKP1} – 20*	-	N×t_{CLKP1} – 30*	-	ns
SIN → SCK ↑ setup time	tIVSHI	SCKn SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	tSHIXI	SCKn SINn		0	-	0	-	ns
Serial clock "L" pulse width	tSLSH	SCKn	External shift clock operation	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	tSHSL	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	tSLOVE	SCKn SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
SIN → SCK ↑ setup time	tIVSHE	SCKn SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑ → SIN hold time	tSHIXE	SCKn SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	tF	SCKn		-	20	-	20	ns
SCK rise time	tR	SCKn		-	20	-	20	ns

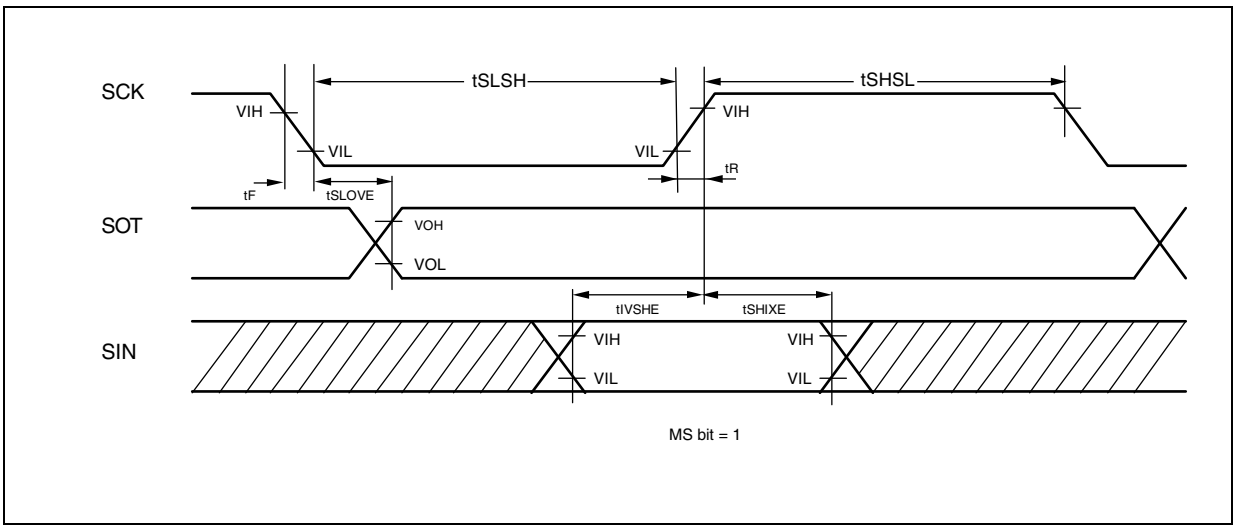
Notes:
- The above characteristics apply to CLK synchronous mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96650 series HARDWARE MANUAL”
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKn_0 and SOTn_1 is not guaranteed.

*: Parameter N depends on tSCYC and can be calculated as follows:
• If tSCYC = 2 × k × t_{CLKP1}, then N = k, where k is an integer > 2
• If tSCYC = (2 × k + 1) × t_{CLKP1}, then N = k + 1, where k is an integer > 1
Examples:

tSCYC	N
4 × t_{CLKP1}	2
5 × t_{CLKP1}, 6 × t_{CLKP1}	3
7 × t_{CLKP1}, 8 × t_{CLKP1}	4
...	...



MS bit = 0



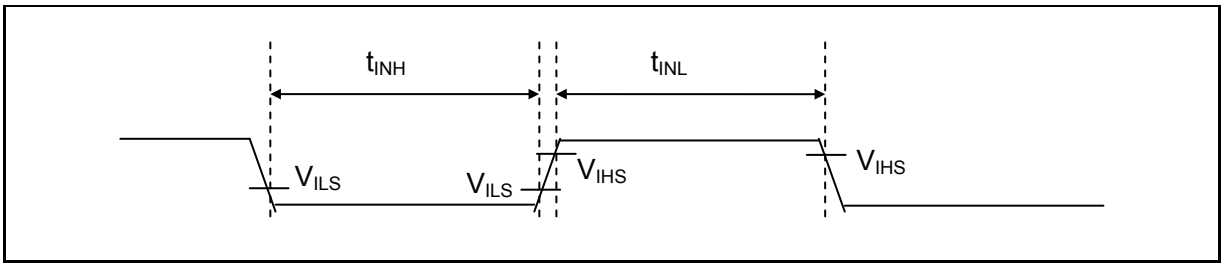
MS bit = 1

(9) External input timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH} t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG				A/D converter trigger input
		FRCKn, FRCKn_R				Free-Running Timer
		TINn, TINn_R				Reload Timer
		TTGn				PPG Trigger input
		INn, INn_R				Input capture
		AINn BINn ZINn				Quadrature position/revolution counter
		INTn, INTn_R, NMI	200	-	ns	External interrupt NMI

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



(10) I^2C timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

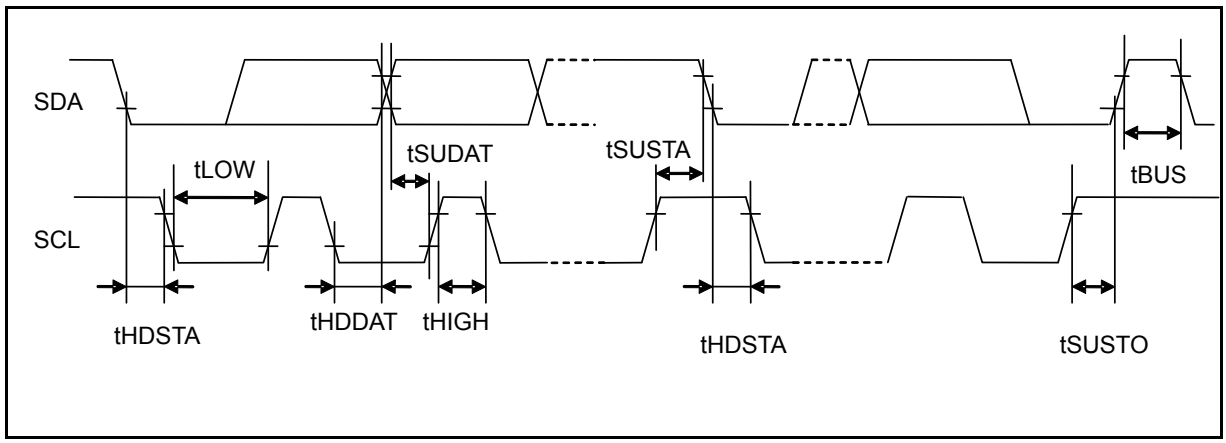
Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	fSCL	CL = 50pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	tHDSTA		4.0	-	0.6	-	µs
SCLclock "L" width	tLOW		4.7	-	1.3	-	µs
SCLclock "H" width	tHIGH		4.0	-	0.6	-	µs
(Repeated) START setup time SCL ↑ → SDA ↓	tSUSTA		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA ↓ ↑	tHDDAT		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	tSUDAT		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	tSUSTO		4.0	-	0.6	-	µs
Bus free time between "STOP condition" and "START condition"	tBUS		4.7	-	1.3	-	µs

*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum tHDDAT must satisfy that it doesn't extend at least "L" period (tLOW) of device's SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "tSUDAT ≥ 250 ns".

*4: t_{CLKP1} is the peripheral clock1 (CLKP1) cycle time. To use I^2C, set the peripheral bus clock at 6 MHz or more.



● 10bit A/D Converter

· Electrical characteristics for the A/D converter

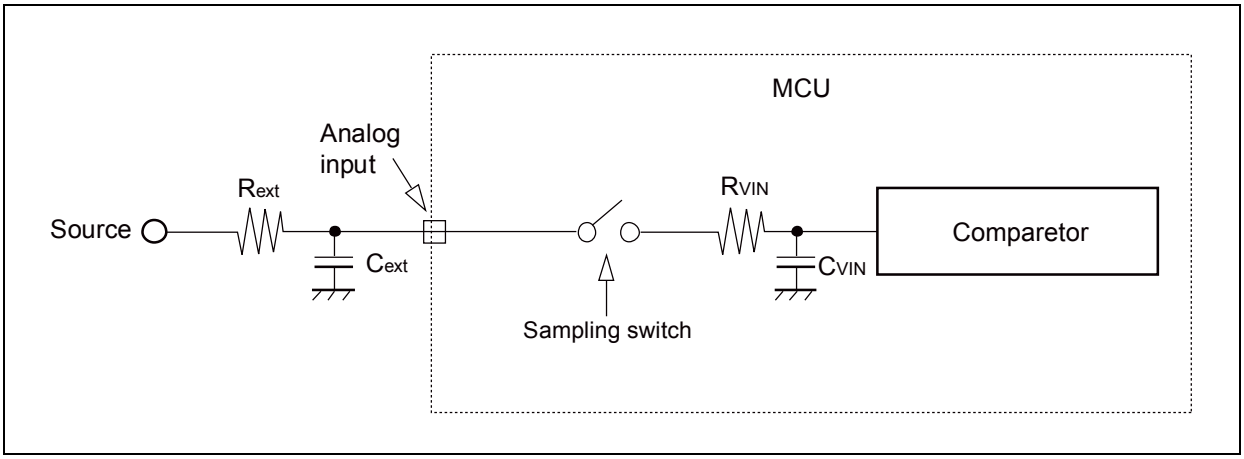
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANx	Typ - 20	AVRL + 0.5LSB	Typ + 20	mV	
Full transition voltage	V_{FST}	ANx	Typ - 20	AVRH - 1.5LSB	Typ + 20	mV	
Compare time	-	-	1.0	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.2	-	8.0	µs	2.7V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	2.7V ≤ AV_{CC} < 4.5V
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	µA	A/D Converter not operated
Reference power supply current (between AVRH to AV_{SS})	I_R	AVRH	-	520	810	µA	A/D Converter active
	I_{RH}		-	-	1.0	µA	A/D Converter not operated
Analog input capacity	C_{VIN}	ANx	-	-	15.9	pF	
Analog port input current	I_{AIN}	ANx	- 0.3	-	+ 0.3	µA	AV_{SS} ,AVRL< V_{AIN} < AV_{CC}, AVRH (T_A = +125°C)
Analog input voltage	V_{AIN}	ANx	AVRL	-	AVRH	V	
Reference voltage range	-	AVRH	AV_{CC} - 0.1	-	AV_{CC}	V	
	-	AVRL	AVss	-	AVss + 0.1	V	

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{cc} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Capacitance of MCU input pin (I/O, analog switch and ADC are contained)

R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

2050Ω (4.5V ≤ AVcc ≤ 5.5V), 3600Ω (2.7V ≤ AVcc < 4.5V)

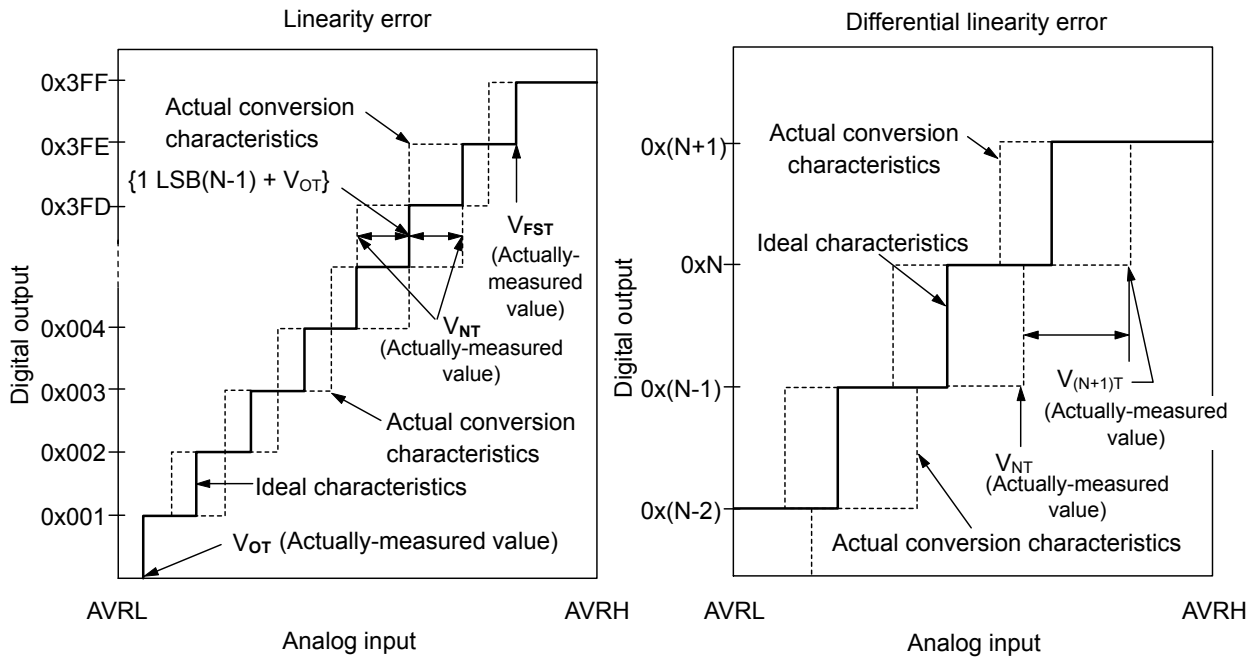
The following approximation formula for the replacement model above can be used:

$$Tsamp\ [min] = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$$

- Do not select a sampling time below the absolute minimum permitted value. (0.5µs for 4.5V ≤ AVcc ≤ 5.5V, 1.2 µs for 2.7V ≤ AVcc < 4.5V)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

• Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0b0000000000⟷ 0b0000000001) and the full-scale transition point (0b1111111110 ⟷ 0b1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linearity error.

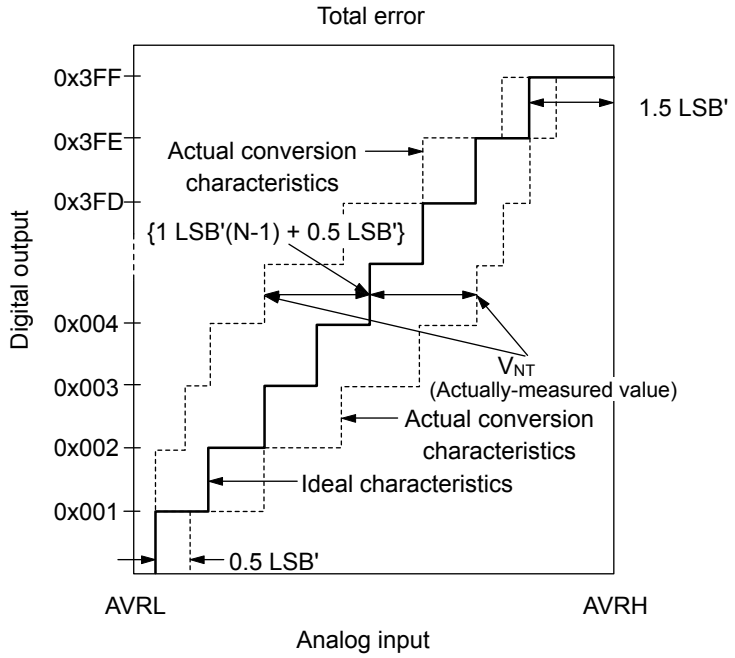


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB'} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.



$$1LSB' \text{ (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

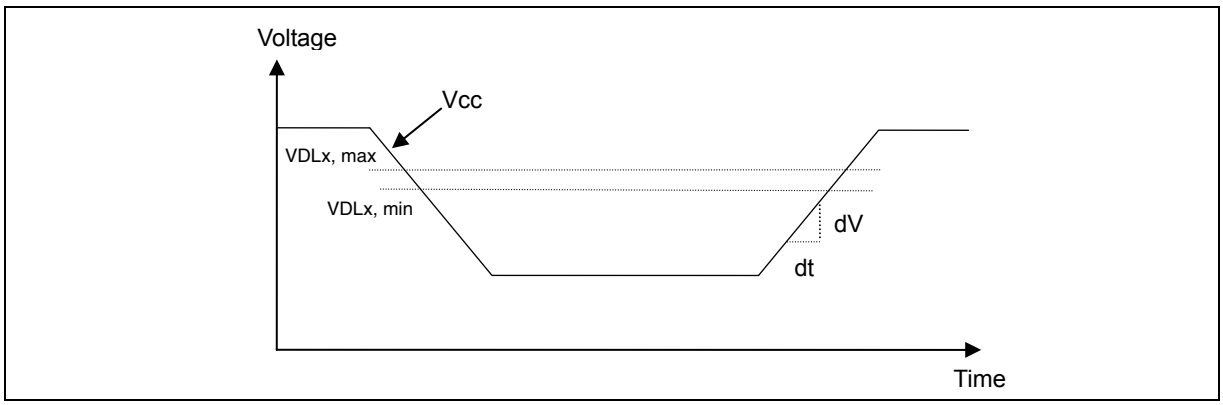
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB' \times (N - 1) + 0.5LSB'\}}{1LSB'}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT}' (Ideal value) = AVRL + 0.5LSB[V]
V_{FST}' (Ideal value) = AVRH - 1.5LSB[V]

● Low voltage detection characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL0	CILCR:LVL = 0000_B	2.70	2.90	3.10	V	
	VDL1	CILCR:LVL = 0001_B	2.79	3.00	3.21	V	
	VDL2	CILCR:LVL = 0010_B	2.98	3.20	3.42	V	
	VDL3	CILCR:LVL = 0011_B	3.26	3.50	3.74	V	
	VDL4	CILCR:LVL = 0100_B	3.45	3.70	3.95	V	
	VDL5	CILCR:LVL = 0111_B	3.73	4.00	4.27	V	
	VDL6	CILCR:LVL = 1001_B	3.91	4.20	4.49	V	
Change ration of power supply voltage	dV/dt	-	-0.004	-	-	V/µs	Detected voltage (VDL) must be within standards.



● Flash Memory Write/Erase Characteristics(Target value)

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Value			Unit	Conditions	Remarks
		Min	Typ	Max			
Sector erase time	Large Sector	-	0.6	3.1	s	$T_A \leq$ + 105°C	Excludes write time prior to internal erase
	Small Sector		0.3	1.6	s	-	
Half word(16 bit) write time	Large Sector	-	25	400	µs	$T_A \leq$ + 105°C	Not including system-level overhead time.
	Small Sector	-	25	400	µs	-	
Chip erase time		-	2.7	14.2	s	$T_A \leq$ + 105°C	Excludes write time prior to internal erase

Erase / write cycles and data hold time (targeted value)

Erase / write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

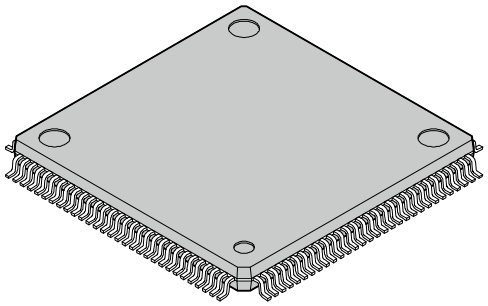
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

■ ORDERING INFORMATION

Part number	Flash memory	Package
MB96F656RAPMC-GSE1*	Flash A (288.5KB)	120-pin plastic LQFP (FPT-120P-M21)
MB96F656RAPMC-GSE2*		
MB96F657RAPMC-GSE1*	Flash A (416.5KB)	
MB96F657RAPMC-GSE2*		

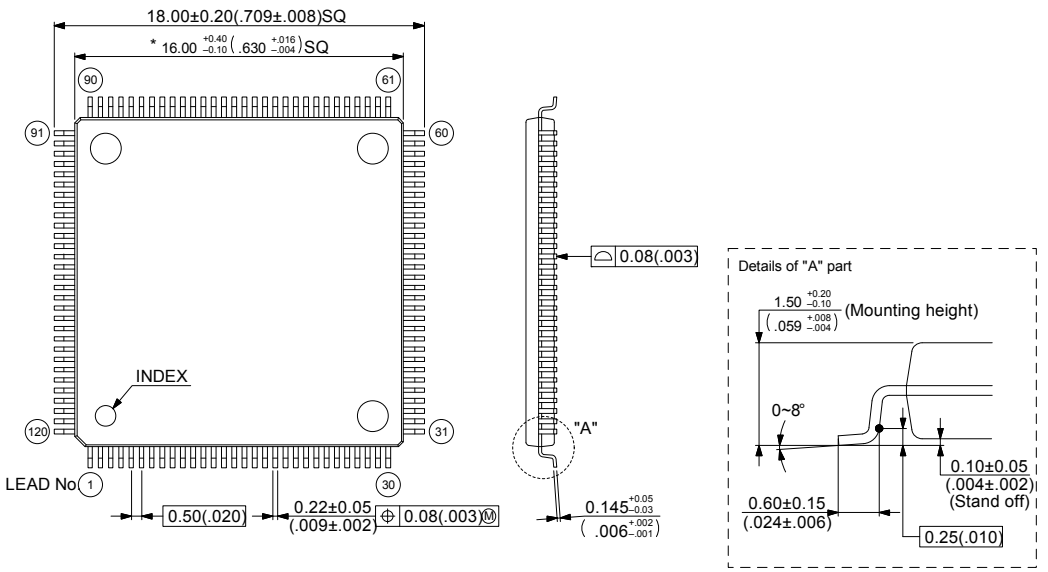
*: These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ REVISION HISTORY

Revision	Date	Modification
Prelim 1	29-Jul-2011	Creation

MEMO

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://sg.fujitsu.com/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fsp/

Edited: Sales Promotion Department