FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13718-2E

16-Bit Original Microcontroller

CMOS

F²MC-16LX MB90M405 Series

Built in FL Display Controller Circuit

MB90MF408/M408/M407/MF408A/ MB90M408A/M407A

■ DESCRIPTION

The MB90M405 series is a general-purpose 16-bit microcontroller, developed for applications requiring fluorescent display tube panel control. Each microcontroller is equipped with 60 highly voltage-resistant output pins, needed for fluorescent display control. The command structure inherits the same AT architecture as the F²MC-8L and F²MC-16L, in order to provide enhanced C-language support, improved extended/signed multiplication/division instructions in addressing mode, and enhanced bit processing. In addition, an onboard 32-bit accumulator allows long word processing.

Note : F²MC stands for FUJITSU Flexible MicroController, and is a registered trademark of Fujitsu Limited.

■ FEATURES

- **Clock**
  - Internal PLL clock multiplication circuit
  - Oscillation clock
    - 1/2 main oscillation clock
    - 1 × to 4 × PLL oscillation clock (2 MHz to 16 MHz at 4 MHz oscillation) , can be set from machine clock
  - Minimum instruction execution time : 62.5 ns (operating at 4 MHz oscillation, 4 × PLL clock, V_{CC} = 3 V)
  - Oscillation clock can generate 1/32, 1/64, 1/128, and 1/256 external clock outputs.
- **Maximum memory space : 16 Mbytes**
  - Can also use 24-bit addressing

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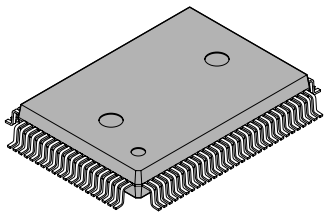
■ PACKAGE

100-pin plastic QFP



(FPT-100P-M06)

- **Command structure optimized for controller applications**
  - Able to handle following data types : bit, byte, word, and long word
  - 23 types of addressing mode
  - High code efficiency (compiler)
  - Enhanced calculation precision using a 32-bit accumulator
  - Enhanced signed multiplication and division instructions and RETI instructions
- **Command structure supports C language/multitasking**
  - Employs system stack pointers
  - Instruction set had symmetry and barrel shift instruction functions
- **Program patch functions (2-address pointers)**
- **Improved execution speed**
  - 4-byte built-in instruction queue allows instructions to be read ahead of time, speeding up execution.
  - Interrupt function
  - 8 programmable priority level settings
  - Incorporates powerful 32-factor interrupt function
- **Data transfer function**
- **Extended intelligent I/O service function : allows up to 16 channels to be set**
- **Low-power consumption modes**
  - Sleep mode (CPU operation clock stops)
  - Timebase timer mode (oscillation clock and timebase timer operate)
  - Stop mode (oscillation clock stops)
  - CPU intermittent operation mode (CPU operates intermittently at the specified intervals)
- **Package**
  - QFP-100 (FPT-100P-M06 : 0.65 mm pin pitch)
- **Process**
  - CMOS technology
- **I/O ports : Maximum 26 (26 ports, also used for internal resources)**
- **Timebase timer : 1 channel**
- **Watchdog timer : 1 channel**
- **16-bit reload timer : 3 channels**
- **16-bit freerun timers : 1 channel**
- **Output compare : 1 channel**
  - If the count value of the 16-bit freerun timer and compare register setting match, an interrupt request can be output
- **Input capture : 2 channels**
  - By detecting a valid edge in a signal input from the external input pin, it is possible to read the 16-bit freerun timer count into the input capture data register, and output an interrupt request.
- **Serial I/O : 2 channels**
- **UART : 2 channels**
  - Includes full-duplex double buffer (8 bits length)
  - Can be set to clock-asynchronous transfer or clock-synchronized serial transfer (I/O extended serial)
- **DTP/external interrupt (4 channels)**
  - Extended intelligent I/O service can be started via external input
  - It is possible to generate an internal hardware interrupt via external input
- **Delayed interrupt generation module**
  - It is possible to output task switching interrupt requests
- **8/10 bit A/D converter (16 channels)**
  - Choice of 8 and 10-bit resolution selectable

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- **FL control circuit**
  - FL driver control enabled (up to 32 digits and up to 60 segments with automatic display control)
    - Any number between 1 and 32 digits can be set
    - Dimmer setting possible
  - LED driver control enabled (up to 16 with automatic display control)
    - Up to 16 automatic display control possible at 1/2 duty
- **Time clock output circuit**
  - Can be set to 1/32, 1/64, 1/128, or 1/256 of oscillation clock

■ PRODUCT LINEUP

Part Number	MB90MF408*1 MB90MF408A*2	MB90M408*1 MB90M408A*2	MB90M407*1 MB90M407A*2	MB90MV405
Classification	Internal flash memory type	Internal mask ROM type		Evaluation
ROM size	128 Kbytes		96 Kbytes	None onboard
RAM size	4 Kbytes		4 Kbytes	4 Kbytes
Emulator power supply*3	—			Included
CPU functions	Number of basic instructions : 351 Minimum instruction execution time : 62.5 ns/4 MHz (with x4 multiplier) Addressing modes : 23 Program patch function : 2 address pointers Maximum memory space : 16 Mbytes			
Ports	26 (CMOS) I/O ports (26 ports, also used for resources)			
FL-control circuit	60 FL outputs possible (during LED control, 43 FL output and 17 LED control) FL and LED driver control enabled During FL driver control, both digit and segment dimmer setting possible			
Serial I/O (UART)	Includes full-duplex double buffer Clock-synchronized/asynchronous settings available Can also be used as clock synchronized extended I/O serial Also equipped with dedicated baud rate generator Serial I/O: 2 channels, UART: 2 channels			
16-bit reload timers	16-bit reload timer operation (can be set to toggle or one-shot output) Event count function can be set 3 channels built in			
16-bit I/O timer	One 16-bit output comparison channel (for clearing freerun timer) Two 16-bit input capture channels			
8/10 bit A/D converter	16 channels (input multiplex) Choice of 8 and 10-bit resolution available Conversion time : 6.125 µs (when machine clock operating at 16 MHz)			
Time clock output circuit	Possible to divide external input oscillation clock and output externally Programmable divisions : 32/64/128/256			
I^2C*4 Bus	One I^2C interface channel built in			
DTP/external interrupt	4 independent channels (also used with A/D input) Interrupt factors : can be set to “L”→“H” edge/“H”→“L” edge/“L” level/“H” level			
Low-power modes	Sleep mode/timebase timer mode, stop mode, and intermittent CPU mode			
Process	CMOS			
Package	QFP-100 (0.65 mm pitch)			PGA256
Operating voltage	3.3 V ± 0.3 V (16 MHz : 4 MHz 4x)			

*1 : All FL-output pins (FIP0 to FIP59) have pull downs

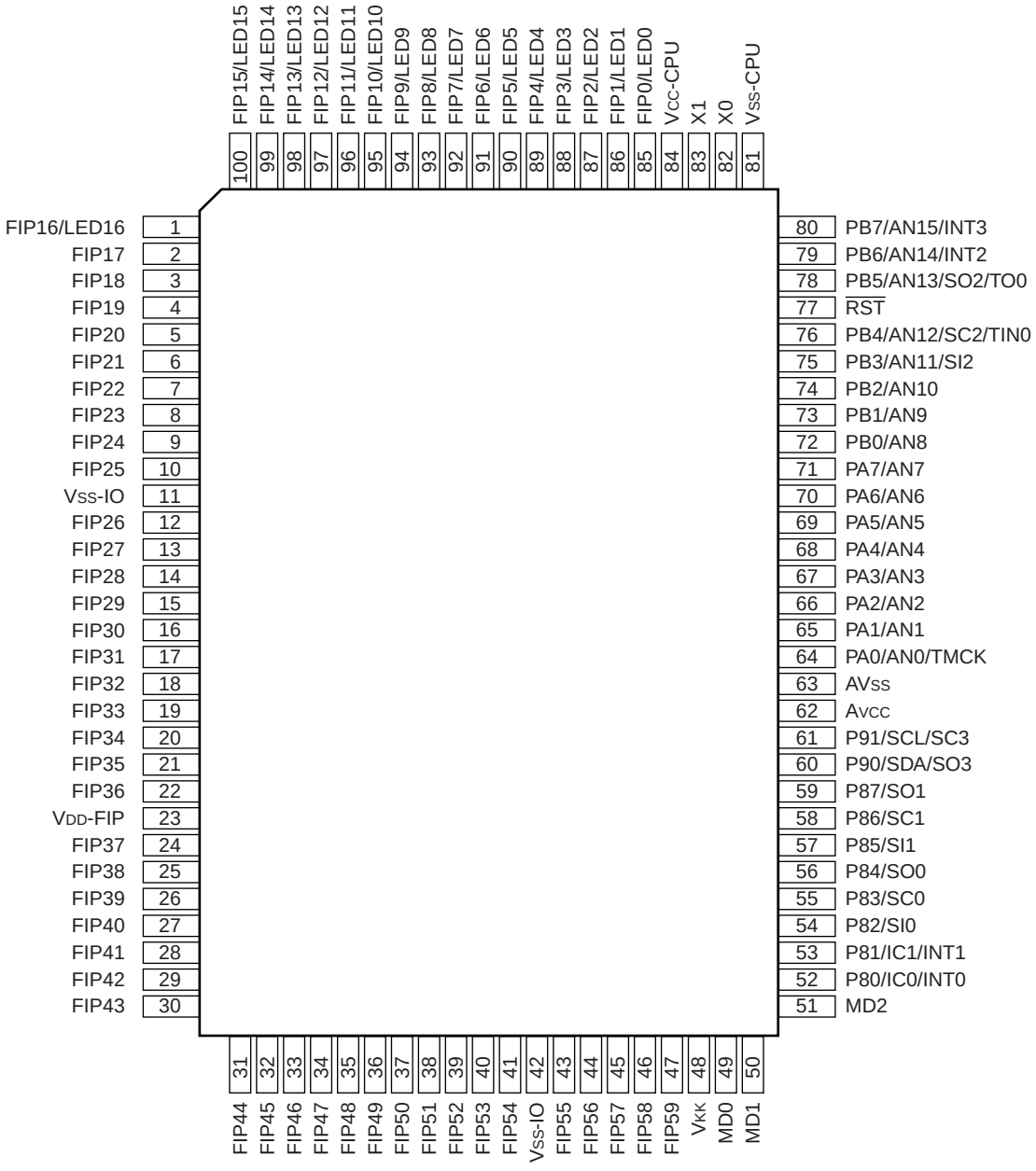
*2 : Some FL-output pins (FIP0 to FIP16) do not have pull downs. The remaining FL-output pins (FIP17 to FIP59) have pull downs.

*3 : Setting of DIP Switch (S2) when using emulation pod (MB2145-507) . Refer to “2.7 Dedicated Emulator Power Supply” in the “MB2145-507 Hardware Manual” for details.

*4 : Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent Rights to use, these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

■ PIN ASSIGNMENTS

(TOP VIEW)



(FPT-100P-M06)

■ PIN DESCRIPTIONS

Pin No. QFP-100	Pin Name	Circuit Type	State/ Function at Reset	Description
82, 83	X0, X1	A	Oscillating	Oscillation Input/Output pin When connected to external clock, please free pin X1
77	$\overline{RST}$	B	Reset input	External reset input pin
85 to 100	FIP0 to FIP15	C	V_{KK} Pull-down output (If pull-down resistance is set)	Set when FL driver authorized
	LED0 to LED15			Set when LED driver authorized
1	FIP16			Set when FL driver authorized
	LED16			Set when LED driver authorized
2 to 10 12 to 19	FIP17 to FIP33			Dedicated FL driver output pin
20 to 22 24 to 41 43 to 47	FIP34 to FIP59	D		
52	P80	E	Port input (Hi-z)	I/O port
	IC0			Input capture ch 0 is external trigger input pin
	INT0			External interrupt input ch 0 is external factor input pin Accepted when bit EN0 set to enabled
53	P81			I/O port
	IC1			Input capture ch 1 is external trigger input pin
	INT1			External interrupt input ch 1 is external factor input pin Accepted when bit EN1 set to enabled
54	P82			I/O port
	SI0			Serial data input pin for serial I/O ch 0 During input operation by serial I/O ch 0, pin is used continuously, so do not use as a different pin
55	P83			I/O port
	SC0			Serial clock I/O pin for serial I/O ch 0 Effective when serial clock output for serial I/O ch 0 enabled
56	P84			I/O port
	SO0			Serial data output pin for serial I/O ch 0 Effective when serial data output for serial I/O ch 0 enabled
57	P85			I/O port
	SI1			Serial data input pin for serial I/O ch 1 During input operation by serial I/O ch 1, pin is used continuously, so do not use as a different pin

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Pin No. QFP-100	Pin Name	Circuit Type	State/ Function at Reset	Description
58	P86	E	Port input (Hi-z)	I/O port
	SC1			Serial clock I/O pin for serial I/O ch 1 Effective when serial clock output for serial I/O ch 1 enabled
59	P87			I/O port
	SO1			Serial data output pin for serial I/O ch 1 Effective when serial data output for serial I/O ch 1 enabled
60	P90	G		I/O port (however, Nch open drain)
	SDA			I^2C interface data I/O pin. This function is effective when I^2C interface operation is enabled. While the I^2C interface is operating, set the port to input (DDR9 : bit 8 = 0) .
	SO3			Serial data output pin for serial I/O ch 3 Effective when serial data output for serial I/O ch 3 enabled
61	P91	G		I/O port (however, Nch open drain)
	SCL			I^2C interface clock I/O pin. This function is effective when I^2C interface operation is enabled. While the I^2C interface is operating, set the port to input (DDR9 : bit 9 = 0) .
	SC3			Serial clock I/O pin for serial I/O ch 3 Effective when serial clock output for serial I/O ch 3 enabled
64	PA0	F	Analog input	I/O port
	AN0			Ch 0 of A/D converter analog input pin Effective when analog input setting enabled (set with ADER)
	TMCK			Time clock output pin. Effective when output enabled. Note that this is not effective when analog input enabled via ADER.
65 to 74	PA1 to PB2			I/O port
	AN1 to AN10			Ch 1 to ch 10 of A/D converter analog input pin Effective when analog input setting enabled (set with ADER)
75	PB3			I/O port
	AN11			Ch 11 of A/D converter analog input pin Effective when analog input setting enabled (set with ADER)
	SI2			Serial data input pin for serial I/O ch 2 During input operation by serial I/O ch 2, pin is used continuously, so do not use as a different pin

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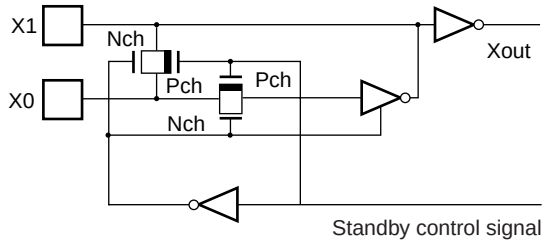
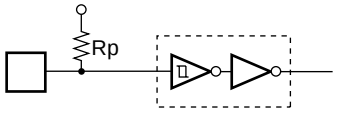
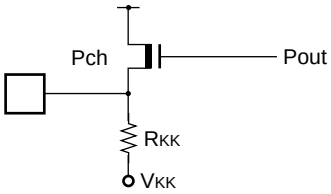
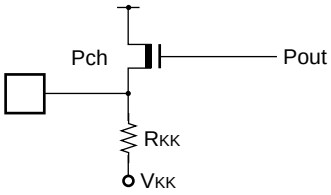
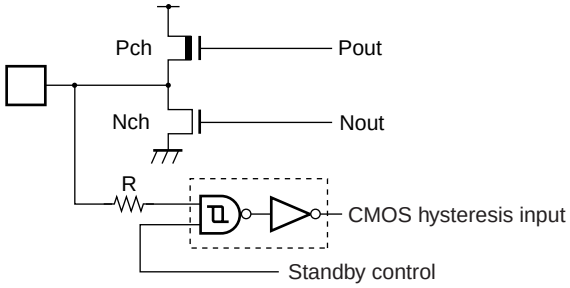
Pin No. QFP-100	Pin Name	Circuit Type	State/ Function at Reset	Description
76	PB4	F	Analog input	I/O port
	AN12			Ch 12 of A/D converter analog input pin Effective when analog input setting enabled (set with ADER)
	SC2			Serial clock I/O pin for serial I/O ch 2 Effective when serial clock output for serial I/O ch 2 enabled
	TIN0			External clock input pin of reload timer ch 0 Effective when external clock input enabled (ADER is prioritized)
78	PB5			I/O port
	AN13			Ch 13 of A/D converter analog input pin Effective when analog input setting enabled (set with ADER)
	SO2			Serial data output pin for serial I/O ch 2 Effective when serial data output for serial I/O ch 2 enabled
	TO0			External event output pin of reload timer ch 0 Effective when external event output enabled (ADER is prioritized)
79, 80	PB6, PB7			I/O port
	AN14, AN15			Ch 14 and ch 15 of A/D converter analog input pin Effective when analog input setting enabled (set with ADER)
	INT2, INT3			External interrupt input ch 2 and ch 3 are external factor input pins Accepted when bits EN2 and EN3 set to enabled
62	AV_{CC}	H	Power input	Vcc power input pin of analog macro
63	AV_{SS}			Vss power input pin of analog macro
48	V_{KK}	—		Power pin of pull-down side during high voltage resistant output
49	MD0	B	Mode pins	Input pin for specifying operating mode. Connect to V_{CC}. Additionally, when flash boot program is being used, be sure to switch to V_{SS}.
50	MD1			Input pin for specifying operating mode. Connect to V_{CC}.
51	MD2			Input pin for specifying operating mode. Connect to V_{SS}. Additionally, when flash boot program is being used, be sure to switch to V_{CC}.
11, 42	V_{SS}–IO	—	Power input	I/O power (0 V : GND) input pin
23	V_{DD}–FIP			FIP power (3 V : V_{CC}) input pin
81	V_{SS}–CPU			Control circuit power (0 V : GND) input pin
84	V_{CC}–CPU			Control circuit power (3 V : V_{CC}) input pin

■ I/O CIRCUITS

Type	Circuit	Remarks
A		• Oscillation circuit Oscillation return resistance = approx. 1 MΩ
B		• Hysteresis input pin Built-in pull-up resistance (Rp)
C		• Pch open drain output - High voltage resistance port output I_{OL} = –23 mA When used as normal port, connect a diode clamp or the like to prevent voltage V_{KK} from being applied to the pin during “L” level output. (See “■ HANDLING DEVICES”)
D		• Pch open drain output - High voltage resistance port output I_{OL} = –12 mA When used as normal port, connect a diode clamp or the like to prevent voltage V_{KK} from being applied to the pin during "L" level output. (See "■ HANDLING DEVICES")
E		• CMOS hysteresis I/O pin - CMOS output - CMOS hysteresis input (Equipped with function to block input during standby) I_{OL} = 4 mA

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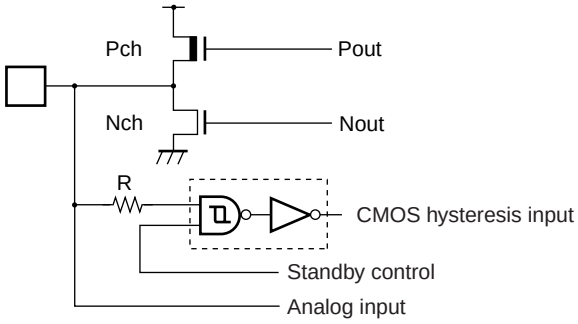
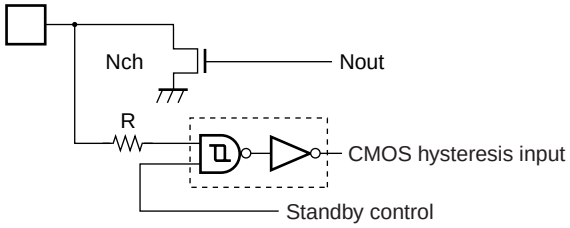
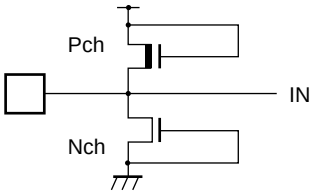
Type	Circuit	Remarks
F		• Analog/CMOS hysteresis I/O pin - CMOS output - CMOS hysteresis input (Equipped with function to block input during standby) - Analog input (When ADER-compatible bit is “1” analog input is enabled) I_{OL} = 4 mA
G		• Nch open drain output - CMOS hysteresis input (Equipped with function to block input during standby) Unlike the CMOS I/O pin, there is no Pch transistor. Therefore, when the device power is shut off, there will be no flow of current to the device power (V_{CC}-IO/V_{CC}-CPU) , even if external voltage is applied to the pin.
H		• Analog power input protection circuit

■ HANDLING DEVICES

This section contains important information on handling the device, regarding the following :

- Do not exceed maximum rated voltage (to prevent latch-up)
- Supply voltage stability
- Power-on precautions
- Treatment of unused pins
- Treatment of A/D converter power supply pin
- Notes on using external clock
- Power supply pin
- Sequence for applying power analog input of A/D converter
- Output of high-voltage output pin (circuit types C & D)

- **Do not exceed maximum rated voltage (to prevent latch-up)**
- With a CMOS IC, if voltage above V_{CC} or below V_{SS} is applied to an output or input pin other than a medium/high voltage resistance pin, or if voltage between V_{CC} and V_{SS}, but exceeding the rated voltage, is applied, a latch-up state could be generated. In the event of a latch-up, the power current will increase drastically, possibly destroying the chip due to overheating. For this reason, make sure not to exceed the maximum rating.
- When applying or shutting off analog power, make sure that the analog power (AV_{CC}) and analog input voltage do not exceed the digital power voltage (V_{CC}) .

- **Supply voltage stability**

Even within the scope of operational protection for V_{CC} power voltage, a sudden increase in power voltage could cause the unit to malfunction. For this reason, please stabilize the V_{CC} power voltage.

The standard for stabilizing voltage is a V_{CC} ripple fluctuation (peak to peak value) of no more than 10% of standard V_{CC} power voltage at commercial power frequencies (50 Hz to 60 Hz) , and an excess fluctuation rate of no more than 0.1 V/ms for instantaneous changes when switching power.

- **Power-on precautions**

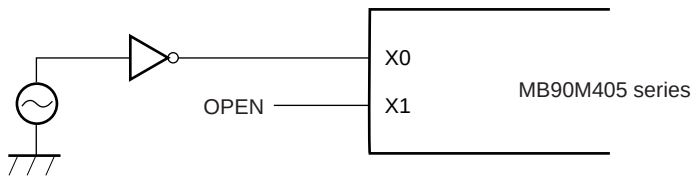
When turning on the power, ensure that the power voltage (V_{CC}) power-up time is at least 50 µs (0.2 V to 2.7 V) , in order to keep the built-in step-down circuit from malfunctioning.

- **Treatment of unused pins**

Leaving unused input pins free could cause permanent damage due to malfunctions and latch-ups. For this reason, set unused input pins to pull-up or pull-down via resistance of 2 kΩ or more. Additionally, if there are unused I/O pins, either set them to output and leave them free, or set them to input and treat them as input pins.

- **Notes on using external clock**

When using an external clock, please drive pin X1 only, and free pin X1. An example of using an external clock is shown in the figure below:



- **Power supply pin**
- When there are multiple V_{CC}/V_{SS}, in order to prevent latch-ups and other malfunctions, then from design considerations, although pins of the same potential are connected device-internally, make sure to connect the V_{CC} and V_{SS} pins to power and grounds, in order to reduce unneeded radiation, and prevent strobe signal malfunctions due to rises in ground level.
- Connect V_{CC} and V_{SS} to MB90M405 series devices from a current supply source at low impedance.
- Connect an approximately 0.1 µF capacitor as a bypass capacitor between the V_{CC} and V_{SS}, near the V_{CC} and Vss pins, in order to combat power-source noise in MB90M405 series devices.

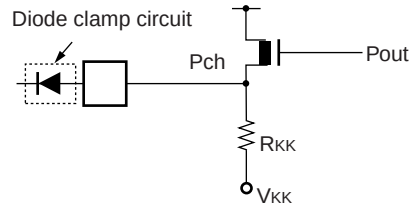
- **Crystal Oscillation Circuit**
- Noise to the X0 and X1 pins can cause MB90M405 series devices to malfunction. Design the printed circuit board so that pins X0 and X1, and the crystal oscillator (or ceramic oscillator) and the capacitor to the ground, are near pins X0 and X1, and not crossing the X0 and X1, or other wiring.
- Stable operation can be expected from PCB artwork that surrounds pins X0 and X1 with grounds.

- **Sequence for applying power analog input of A/D converter**
- Always make sure to apply voltage to the digital power pin (V_{CC}) before applying voltage to the A/D converter power pin (AV_{CC}) and analog input pins (AN0 to AN15) .
- When shutting off the power, shut off digital power (V_{CC}) after shutting off A/D converter power and analog input.
- If a port pin also used for analog input is used as an input port, make sure that the analog input voltage does not exceed AV_{CC} (there is no problem with simultaneously applying and cutting analog and digital power) .

- **Pin handling when not using A/D converter**
- When not using the A/D converter, connect so that $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$.

- **Output of high-voltage resistance output pin (circuit types C & D)**

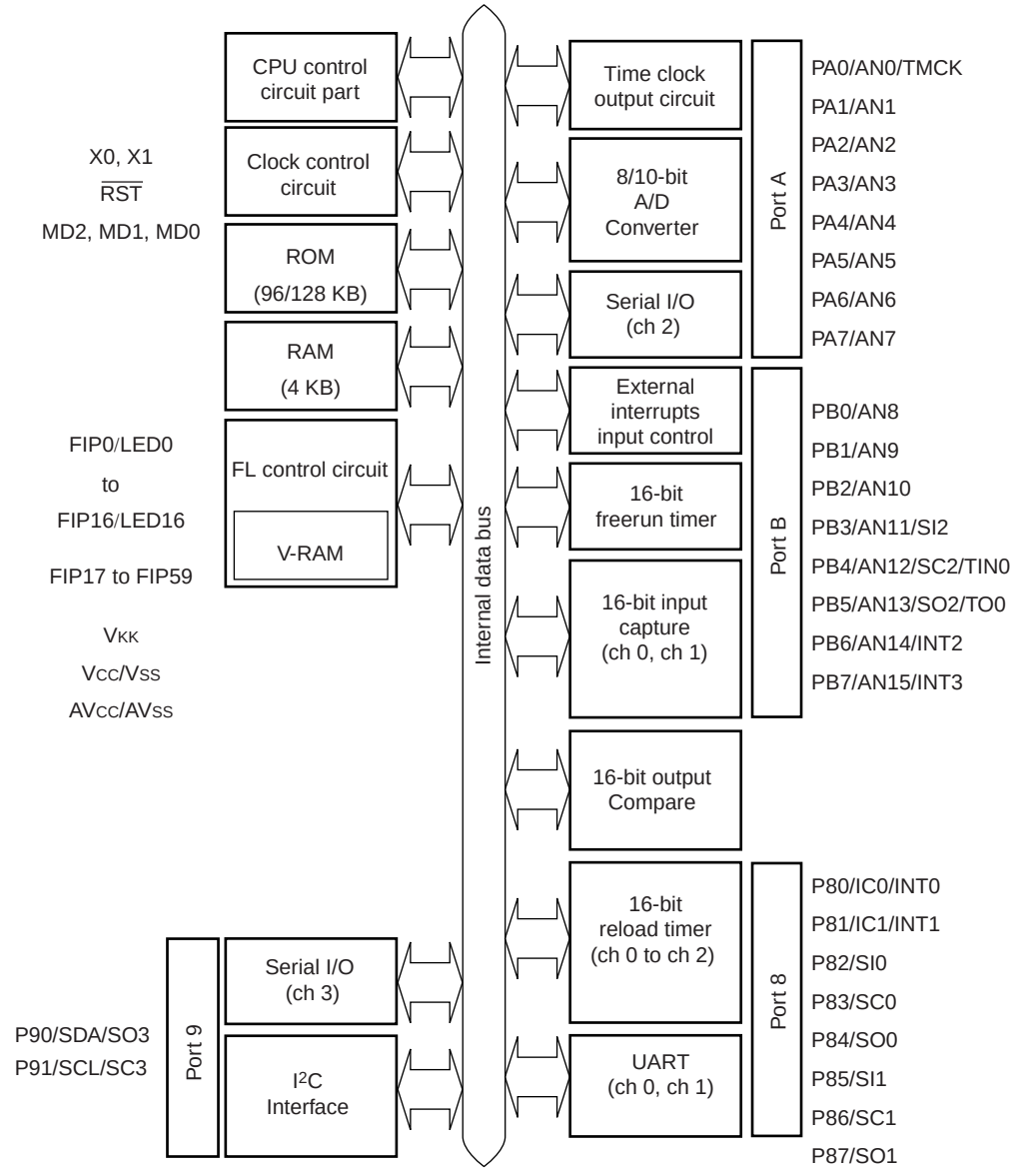
If using high voltage-resistance output (circuit types C & D) as the ordinary output port, when outputting “L” level, a value of pull-down for V_{KK} pin voltage is output. In this case, the V_{KK} level voltage is applied to the external circuit, so add a diode clamp circuit as shown in the figure below:



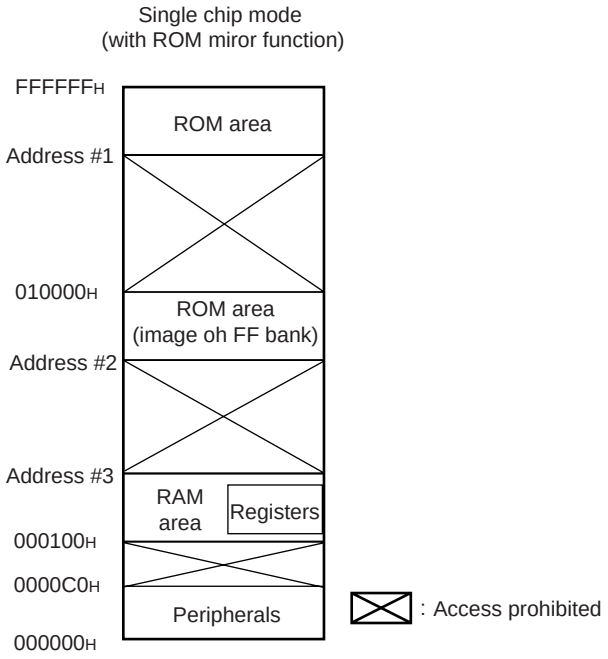
- **Notes on PLL clock mode**

If the oscillator is disconnected, or clock input stops, when the PLL clock is selected on the microcontroller, the microcontroller may continue to operate, using the free-run frequency of the PLL-internal self-exciting oscillation circuit. This operation is not guaranteed.

■ BLOCK DIAGRAM



■ MEMORY MAP



Model	Address #1	Address #2	Address #3
MB90M407/A	FE8000H	004000H	001100H
MB90M408/A	FE0000H	004000H	001100H
MB90MF408/A	FE0000H	004000H	001100H
MB90MV405	F80000H*	004000H	001100H

* : V products have no built-in ROM. Show the ROM decode area on the tool side.

The purpose of the ROM mirror function is to use a small C compiler model.

The lower 16-bit address of the FF bank is the same as the lower 16-bit address of the 00 bank. However, as the ROM area of the FF bank exceeds 48 Kbytes, a mirror image of all the data in the ROM area cannot be shown in the 00 bank.

When using a small C compiler model, storing a data table in “FF4000H to FFFFFFH” allows a mirror image of the data table to be shown in “004000H to 00FFFFH”. Consequently, it is possible to refer to the data table in the ROM area without declaring a far pointer.

- When setting the ROM mirror function register, a mirror image of the data in the upper side of bank FF (“FF4000H to FFFFFFH”) can be seen in the upper side of bank 00 (“004000H to 00FFFFH”) .
- See “■ PERIPHERAL FUNCTIONS 15. ROM Mirror Function Selection Module” for details on setting the ROM mirror function.

■ I/O MAP

Address	Abbreviated Register Name.	Register name	Read/ Write	Resource Name	Initial Value
000000_H to 000007_H	Access prohibited				
000008_H	PDR8	Port 8 data register	R/W	Port 8	$XXXXXXXX_B$
000009_H	PDR9	Port 9 data register	R/W	Port 9	$XXXXXXXX_B$
$00000A_H$	PDRA	Port A data register	R/W	Port A	$XXXXXXXX_B$
$00000B_H$	PDRB	Port B data register	R/W	Port B	$XXXXXXXX_B$
$00000C_H$ to 000017_H	Access prohibited				
000018_H	DDR8	Port 8 direction register	R/W	Port 8	$0\ 0\ 0\ 0\ 0\ 0\ 0\ 0_B$
000019_H	DDR9	Port 9 direction register	R/W	Port 9	$XXXXXX\ 0\ 0_B$
$00001A_H$	DDRA	Port A direction register	R/W	Port A	$0\ 0\ 0\ 0\ 0\ 0\ 0\ 0_B$
$00001B_H$	DDRB	Port B direction register	R/W	Port B	$0\ 0\ 0\ 0\ 0\ 0\ 0\ 0_B$
$00001C_H$ to $00001D_H$	Access prohibited				
$00001E_H$	ADER0	Analog input enable register 0	R/W	Port A, A/D	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1_B$
$00001F_H$	ADER1	Analog input enable register 1	R/W	Port B, A/D	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1_B$
000020_H	SMR0	Mode register ch 0	R/W	UART ch0	$0\ 0\ 0\ 0\ 0\ X\ 0\ 0_B$
000021_H	SCR0	Control register ch 0	R/W		$0\ 0\ 0\ 0\ 0\ 1\ 0\ 0_B$
000022_H	SIDR0	Input data register ch 0	R		$0\ 0\ 0\ 0\ 0\ 0\ 0\ 0_B$
	SODR0	Output data register ch 0	W		$XXXXXXXX_B$
000023_H	SSR0	Status register ch 0	R/W		$0\ 0\ 0\ 0\ 1\ 0\ 0\ 0_B$
000024_H	SMR1	Mode register ch 1	R/W	UART ch1	$0\ 0\ 0\ 0\ 0\ X\ 0\ 0_B$
000025_H	SCR1	Control register ch 1	R/W		$0\ 0\ 0\ 0\ 0\ 1\ 0\ 0_B$
000026_H	SIDR1	Input data register ch 1	R		$XXXXXXXX_B$
	SODR1	Output data register ch 1	W		
000027_H	SSR1	Status register ch 1	R/W		$0\ 0\ 0\ 0\ 1\ 0\ 0\ 0_B$
000028_H	CDCR0	Communication prescaler control register ch 0	R/W	Communication prescaler 0	$0\ XXX\ 0\ 0\ 0\ 0_B$
000029_H	CDCR1	Communication prescaler control register ch 1	R/W	Communication prescaler 1	$0\ XXX\ 0\ 0\ 0\ 0_B$

(Continued)

Address	Abbreviated Register Name.	Register name	Read/ Write	Resource Name	Initial Value
00002A$_H$	IBSR	I^2C status register	R	I^2C interface	0 0 0 0 0 0 0 0$_B$
00002B$_H$	IBCR	I^2C control register	R/W		0 0 0 0 0 0 0 0$_B$
00002C$_H$	ICCR	I^2C clock control register	R/W		XX 0 XXXXX$_B$
00002D$_H$	IADR	I^2C address register	R/W		XXXXXXXX$_B$
00002E$_H$	IDAR	I^2C data register	R/W		XXXXXXXX$_B$
00002F$_H$	ISEL	I^2C port selection register	R/W		XXXXXXX 0$_B$
000030$_H$	ENIR	DTP/external interrupt enable register	R/W	DTP/external interrupt circuit	XXXX 0 0 0 0$_B$
000031$_H$	EIRR	DTP/external interrupt factor register	R/W		XXXXXXXX$_B$
000032$_H$	ELVR	Request level setting register	R/W		0 0 0 0 0 0 0 0$_B$
000033$_H$	Access prohibited				
000034$_H$	ADCS0	A/D control status register 0 (low-order)	R/W	8/10 bit A/D converter	0 0 XXXXXX$_B$
000035$_H$	ADCS1	A/D control status register 1 (high-order)	R/W		XXXXXXXX$_B$
000036$_H$	ADCR0	A/D data register 0(low-order)	R/W		XXXXXXXX$_B$
000037$_H$	ADCR1	A/D data register 1 (high-order)	R/W		0 0 0 0 0 XXX$_B$
000038$_H$	Access prohibited				
000039$_H$	ADMR	A/D conversion channel setting register	R/W	8/10 bit A/D converter	0 0 0 0 0 0 0 0$_B$
00003A$_H$ to 00003F$_H$	Access prohibited				
000040$_H$	TCCS	Timer counter control status register	R/W	16-bit free-run timer	0 0 0 0 0 0 0 0$_B$
000041$_H$	Access prohibited				
000042$_H$	TCDT	Timer counter data register	R/W	16-bit free-run timer	0 0 0 0 0 0 0 0$_B$
000043$_H$					0 0 0 0 0 0 0 0$_B$
000044$_H$	IPC0	Input capture data register ch 0	R	Input capture	XXXXXXXX$_B$
000045$_H$					XXXXXXXX$_B$
000046$_H$	IPC1	Input capture data register ch 1	R		XXXXXXXX$_B$
000047$_H$					XXXXXXXX$_B$
000048$_H$	ICS01	Input capture control status register	R/W		0 0 0 0 0 0 0 0$_B$
000049$_H$	Access prohibited				
00004A$_H$	OCCP0	Output compare register	R/W	Output compare	XXXXXXXX$_B$
00004B$_H$					XXXXXXXX$_B$
00004C$_H$	OCS0	Output compare control status register	R/W		XX 0 0 XXX 0$_B$
00004D$_H$	Reserved				
00004E$_H$, 00004F$_H$	Access prohibited				

(Continued)

Address	Abbreviated Register Name.	Register name	Read/Write	Resource Name	Initial Value
000050H	TMCSR0	Timer control status register ch 0	R/W	16-bit reload timer ch 0	0 0 0 0 0 0 0 0B
000051H					XXXX 0 0 0 0B
000052H	TMR0/ TMRLR0	16-bit timer register ch 0 (R) 16-bit reload register ch 0 (W)	TMR0 : R TMRLR0 : W		XXXXXXXXB
000053H					XXXXXXXXB
000054H	TMCSR1	Timer control status register ch 1	R/W	16-bit reload timer ch 1	0 0 0 0 0 0 0 0B
000055H					XXXX 0 0 0 0B
000056H	TMR1/ TMRLR1	16-bit timer register ch 1 (R) 16-bit reload register ch 1 (W)	TMR1 : R TMRLR1 : W		XXXXXXXXB
000057H					XXXXXXXXB
000058H	TMCSR2	Timer control status register ch 2	R/W	16-bit reload timer ch 2	0 0 0 0 0 0 0 0B
000059H					XXXX 0 0 0 0B
00005AH	TMR2/ TMRLR2	16-bit timer register ch 2 (R) 16-bit reload register ch 2 (W)	TMR2 : R TMRLR2 : W		XXXXXXXXB
00005BH					XXXXXXXXB
00005CH to 00005FH	Access prohibited				
000060H	SMCS2	Serial mode control status register ch 2	R/W	Serial I/O ch 2	XXXX 0 0 0 0B
000061H					0 0 0 0 0 0 1 0B
000062H	SDR2	Serial shift data register ch 2	R/W		XXXXXXXXB
000063H	Access prohibited				
000064H	SMCS3	Serial mode control status register ch 3	R/W	Serial I/O ch 3	XXXX 0 0 0 0B
000065H					0 0 0 0 0 0 1 0B
000066H	SDR3	Serial shift data register ch 3	R/W		XXXXXXXXB
000067H	Access prohibited				
000068H	FLC1	Display control register 1	W	FL control circuit	XXXXXX 0 0B
000069H	FLC2	Display control register 2	W		0 0 0 0 0 0 0 0B
00006AH	FLDG	Digit setting register	W		0 0 0 0 0 0 0 0B
00006BH	FLDC	Digit number register	W		0 0 0 0 0 0 0 0B
00006CH	Access prohibited				
00006DH	FLST	Status register/definition register	R	FL control circuit	XX 1 XXX 0 0B
			W		0 0 XXXXXXB
00006EH	Access prohibited				
00006FH	ROMM	ROM mirror function selection register	W	ROM mirror function selection module	XXXXXXX 1B

(Continued)

Address	Abbreviated Register Name.	Register name		Read/ Write	Resource Name	Initial Value
000070H to 000077H	SEGD0 to 7	Segment dimmer setting register		W	FL control circuit	XXXXXXXXB
000078H	FLPD0	Port register	FIP36 to 43	W		0 0 0 0 0 0 0 0B
000079H	FLPD1		FIP44 to 51	W		0 0 0 0 0 0 0 0B
00007AH	FLPD2		FIP52 to 59	W		0 0 0 0 0 0 0 0B
00007BH to 00009DH	Access prohibited					
00009EH	PACSR	Program address detection control status register		R/W	Address match detection function	0 0 0 0 0 0 0 0B
00009FH	DIRR	Delayed interrupt factor generation/cancel register		R/W	Delayed interrupt generation module	XXXXXXX 0B
0000A0H	LPMCR	Low-power mode control register		R/W	Low-power control circuit	0 0 0 1 1 0 0 0B
0000A1H	CKSCR	Clock selection register		R/W		1 1 1 1 1 1 0 0B
0000A2H to 0000A7H	Access prohibited					
0000A8H	WDTC	Watchdog timer control register		R/W	Watchdog timer	XXXXX 1 1 1B
0000A9H	TBTC	Timebase timer control register		R/W	Timebase timer	1 XX 0 0 1 0 0B
0000AAH to 0000AD	Access prohibited					
0000AEH	FMCS	Flash memory control status register		R/W	1 Mbit flash memory	0 0 0 0 0 0 0 0B
0000AFH	TMCS	Time clock output control register		R/W	Clock division for time clock	XXXXX 0 0 0B
0000B0H	ICR00	Interrupt control register 00 (for writing)		W, R/W	Interrupt	0 0 0 0 0 1 1 1B
		Interrupt control register 00 (for reading)		R, R/W		XX 0 0 0 1 1 1B
0000B1H	ICR01	Interrupt control register 01 (for writing)		W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 01 (for reading)		R, R/W		XX 0 0 0 1 1 1B
0000B2H	ICR02	Interrupt control register 02 (for writing)		W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 02 (for reading)		R, R/W		XX 0 0 0 1 1 1B
0000B3H	ICR03	Interrupt control register 03 (for writing)		W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 03 (for reading)		R, R/W		XX 0 0 0 1 1 1B
0000B4H	ICR04	Interrupt control register 04 (for writing)		W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 04 (for reading)		R, R/W		XX 0 0 0 1 1 1B
0000B5H	ICR05	Interrupt control register 05 (for writing)		W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 05 (for reading)		R, R/W		XX 0 0 0 1 1 1B

(Continued)

Address	Abbreviated Register Name.	Register name	Read/ Write	Resource Name	Initial Value
0000B6H	ICR06	Interrupt control register 06 (for writing)	W, R/W	Interrupt	0 0 0 0 0 1 1 1B
		Interrupt control register 06 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000B7H	ICR07	Interrupt control register 07 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 07 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000B8H	ICR08	Interrupt control register 08 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 08 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000B9H	ICR09	Interrupt control register 09 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 09 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BAH	ICR10	Interrupt control register 10 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 10 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BBH	ICR11	Interrupt control register 11 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 11 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BCH	ICR12	Interrupt control register 12 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 12 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BDH	ICR13	Interrupt control register 13 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 13 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BEH	ICR14	Interrupt control register 14 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 14 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BFH	ICR15	Interrupt control register 15 (for writing)	W, R/W		0 0 0 0 0 1 1 1B
		Interrupt control register 15 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000C0H to 0000FFH	Unused area				
000100H to 0010FFH	RAM area				
001100H to 0011FFH	FL000 to 255	Data RAM for display	R/W	FL control circuit	XXXXXXXXB
001200H to 001FEFH	Reserved area				

(Continued)

(Continued)

Address	Abbreviated Register Name.	Register name	Read/ Write	Resource Name	Initial Value
001FF0H	PADR0	Program address detection register (low-order)	R/W	Address match detection function	XXXXXXXXB
001FF1H		Program address detection register (middle-order)	R/W		XXXXXXXXB
001FF2H		Program address detection register (high-order)	R/W		XXXXXXXXB
001FF3H	PADR1	Program address detection register (low-order)	R/W		XXXXXXXXB
001FF4H		Program address detection register (middle-order)	R/W		XXXXXXXXB
001FF5H		Program address detection register (high-order)	R/W		XXXXXXXXB
001FF6H to 001FFFH	Unused area				

Read/Write symbols used :
R/W : Read/write enabled
R : Read only
W : Write only
Default value symbols used :
0 : Default value is “0”
1 : Default value is “1”
X : Default value is undefined

■ INTERRUPT, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt	EI²OS Support	Interrupt Vector			Interrupt Control Register		Priority
		NO.*		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception	×	#10	0AH	FFFFD4H	—	—	
DTP/external interrupt ch 0	○	#11	0BH	FFFFD0H	ICR00	0000B0H	
DTP/external interrupt ch 1	○	#13	0DH	FFFFC8H	ICR01	0000B1H	
Serial I/O ch 2	△	#15	0FH	FFFFC0H	ICR02	0000B2H	
DTP/external interrupt ch 2/3	○	#16	10H	FFFFCCH			
Serial I/O ch 3	△	#17	11H	FFFFB8H	ICR03	0000B3H	
16-bit free-run timer	△	#18	12H	FFFFB4H			
Reserved	—	#20	—	FFFFACH	ICR04	0000B4H	
16-bit reload timer ch 2	△	#21	15H	FFFFA8H	ICR05	0000B5H	
16-bit reload timer ch 0	△	#23	17H	FFFFA0H	ICR06	0000B6H	
16-bit reload timer ch 1	△	#24	18H	FFFF9CH			
Input capture ch 0	△	#25	19H	FFFF98H	ICR07	0000B7H	
Input capture ch 1	△	#26	1AH	FFFF94H			
Reserved	—	#27	—	FFFF90H	ICR08	0000B8H	
Output comparison match	×	#29	1DH	FFFF88H	ICR09	0000B9H	
Reserved	—	#31	—	FFFF80H	ICR10	0000BAH	
Timebase timer	×	#33	21H	FFFF78H	ICR11	0000BBH	
Reserved	—	#34	—	FFFF74H			
UART0 reception complete	◎	#35	23H	FFFF70H	ICR12	0000BCH	
UART0 transmission complete	△	#36	24H	FFFF6CH			
A/D converter conversion complete	○	#37	25H	FFFF68H	ICR13	0000BDH	
I²C interface	△	#38	26H	FFFF64H			
UART1 reception complete	◎	#39	27H	FFFF60H	ICR14	0000BEH	
UART1 transmission complete	△	#40	28H	FFFF6CH			
Flash memory status	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delayed interrupt output module	×	#42	2AH	FFFF54H			Low

○ : Supported
× : Not supported
◎ : Supported, includes EI²OS stop function
△ : Available if interrupt that shares the same ICR is not used

* : If two interrupts of the same level are output simultaneously, the interrupt with the lower interrupt vector number has priority.

■ PERIPHERAL FUNCTIONS

1. I/O Ports

There are a maximum of 26 I/O ports (parallel I/O ports) , which are also used as resource I/O pins (peripheral function I/O pins) .

• I/O Port Functions

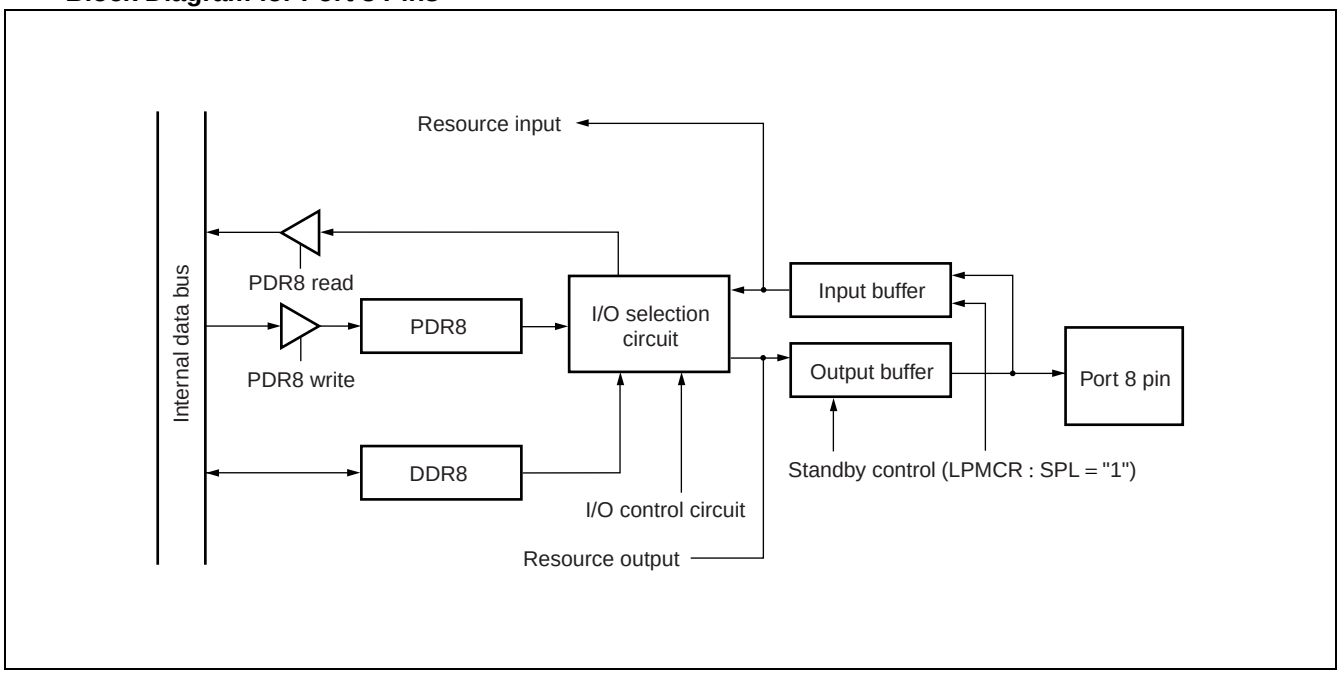
There are two kinds of I/O port : port direction registers (DDRs) and port data registers (PDRs) . The port direction register (DDR) can set port pin I/O at the bit level. The port data register (PDR) sets output data to the port pins. If the port direction register (DDR) sets the I/O port pin to input, the port pin level value can be read by reading the port data register (PDR) . If the port direction register (DDR) sets the I/O port pin to output, the port data register (PDR) value is output to the port pin. Below is a list of the functions of each I/O port, and dual use resources.

- Port 8 : I/O port/resource use (external interrupt input pin, ICU, UART)
- Port 9 : I/O port/resource use (I^2C, serial I/O ch3)
- Port A : I/O port/resource use (A/D converter, time clock output)
- Port B : I/O port/resource use (A/D converter, serial I/O ch2, external interrupt input pin, reload timer ch0)

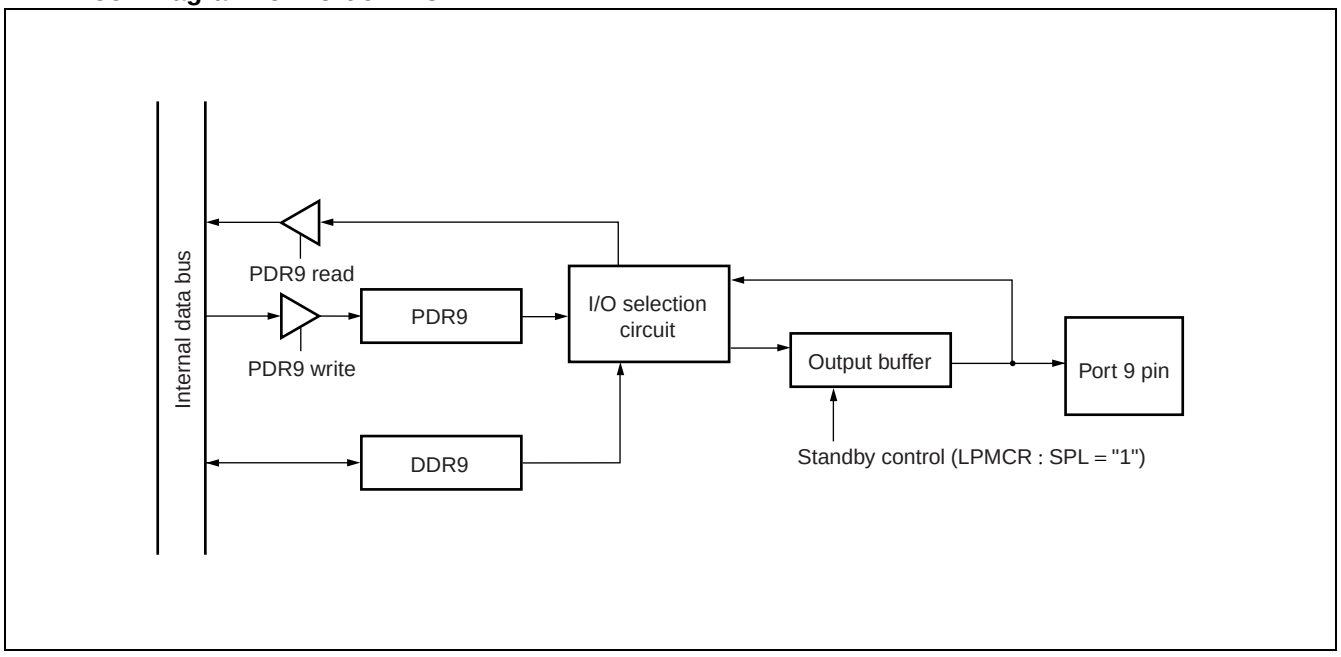
I/O Port Name	Pin Name	Input Format	Output Format	Function								
Port 8	P80 to P87	CMOS (hysteresis)	CMOS	I/O Port	P87	P86	P85	P84	P83	P82	P81	P80
				Resource	SO1	SC1	SI1	SO0	SC0	SI0	IC1	IC0
											INT1	INT0
Port 9	P90/SDA/ SO3, P91/ SCL/SC3		N-ch open drain	I/O Port	—	—	—	—	—	—	P91	P90
				Resource	—	—	—	—	—	—	SCL	SDA
											SC3	SO3
Port A	PA0/AN0/ TMCK to PA7/AN7		CMOS	I/O Port	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
				Resource	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
												TMCK
Port B	PB0/AN8 to PB7/AN15/ INT3			I/O Port	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
				Resource	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8
					INT3	INT2	SO2	SC2	SI2	—	—	—
							TO0	TIN0				

Note: If port A and port B are also used as analog input pins, and are being used as I/O ports, then in addition to the ports A and B direction registers (DDR A/B) and ports A and B data registers (PDR A/B) , set both analog input enable register 0 and 1 (ADER 0/1) to “00_H”. Upon reset, analog input enable registers 0 and 1 are set to “FF_H” by default.

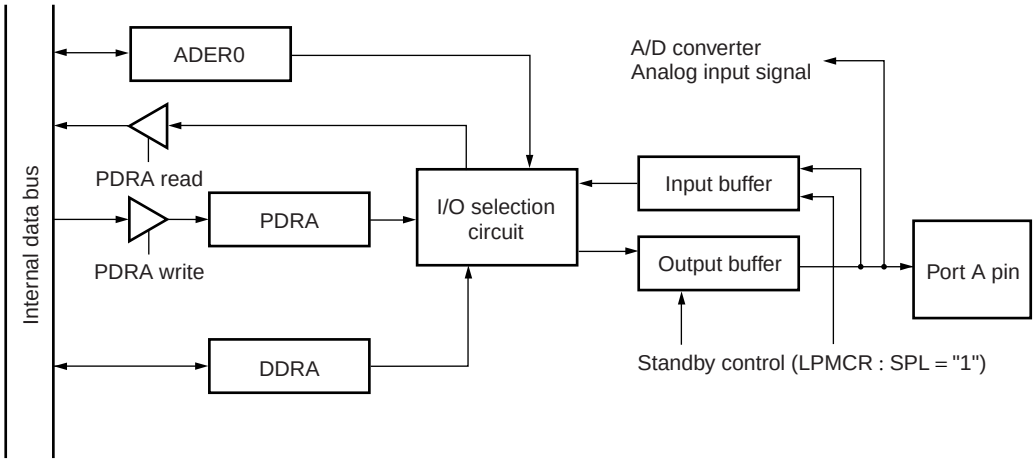
- **Block Diagram for Port 8 Pins**



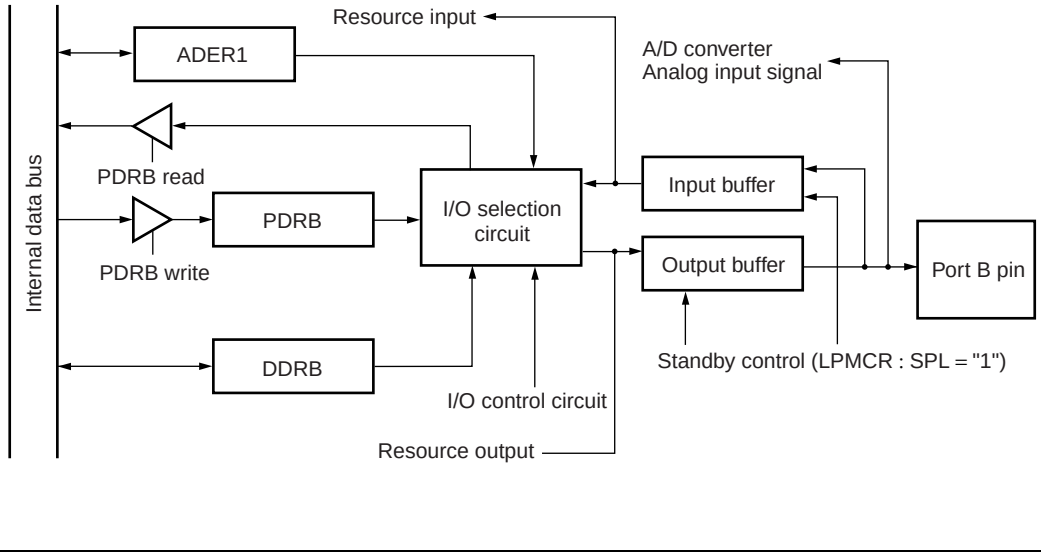
- **Block Diagram for Port 9 Pins**



- **Block Diagram for Port A Pins**



- **Block Diagram for Port B Pins**



2. Serial I/O

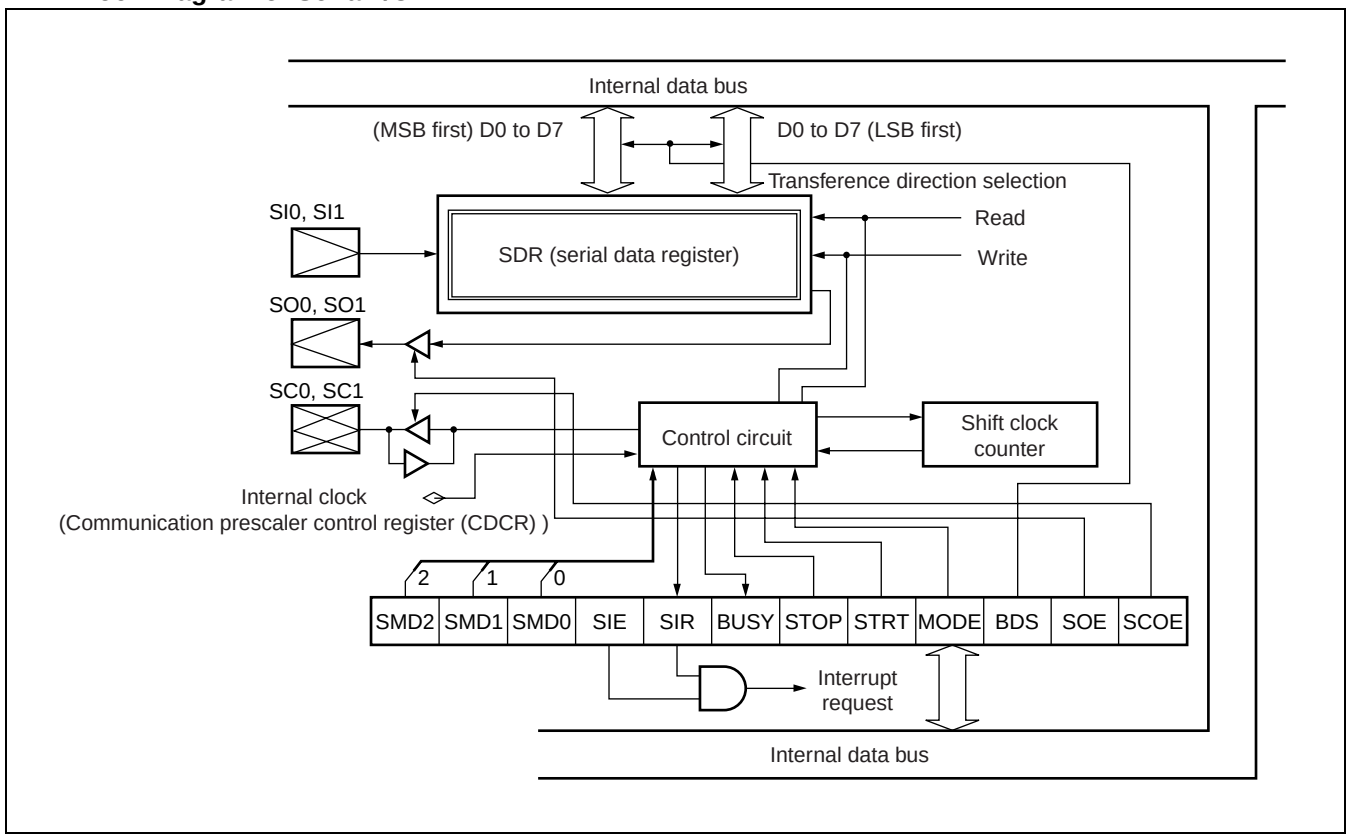
Serial I/O allows data transfer via synchronization with a clock consisting of two 8-bit channels. In addition, LSB first or MSB first can be selected for data transfer.

- **Overview of Serial I/O**

There are two types of serial I/O operation mode :

- Internal shift clock mode
  Data is transferred in synchronization with internal clock (communication prescaler)
- External shift clock mode
  Data is transferred in synchronization with clock input from external pin (SC) . In this mode, it is also possible to transfer data via CPU instructions (port inversion instruction execution timing) by manipulating the general-purpose port sharing the external pin (SC) .

- **Block Diagram of Serial I/O**



3. Timebase Timer

The timebase timer is a 18-bit free-run counter that counts up in synchronization with the main clock. The timer has an interval timer function capable of setting four different intervals, and a function for supplying clocks to the oscillator stabilization standby timer, watchdog timer, and time clock output circuit.

- **Interval timer function**

The interval timer function sends an interrupt request at set intervals.

- When the timebase timer counter's interval timer counter overflows, an interrupt request is output.
- One of four intervals can be set for the interval timer.

Main Clock Cycle	Interval Times
2/HCLK (0.5 µs)	2^{12}/HCLK (Approx. 1.02 ms)
	2^{14}/HCLK (Approx. 4.09 ms)
	2^{16}/HCLK (Approx. 16.38 ms)
	2^{19}/HCLK (Approx. 131.1 ms)

HCLK : Oscillator clock frequency
Values in parentheses ( ) are when oscillator clock frequency is 4 MHz.

- **Clock Supply Function**

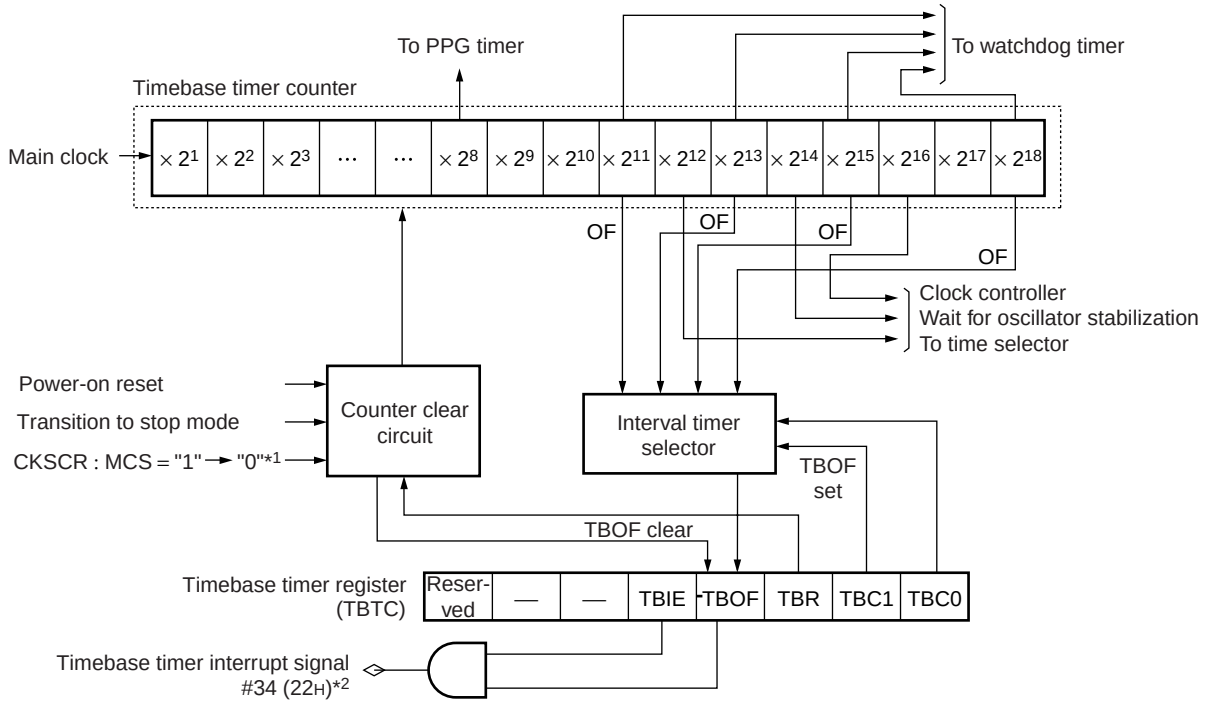
The clock supply function supplies operation clocks to the oscillation stabilization standby timer and some peripheral functions.

Clock Supply Destination	Clock Cycles	Remarks
Oscillation stabilization standby	2^{13}/HCLK (Approx. 2.05 ms)	Oscillation stabilization standby for ceramic oscillator
	2^{15}/HCLK (Approx. 8.2 ms)	Oscillation stabilization standby for crystal oscillator
	2^{18}/HCLK (Approx. 65.53 ms)	
Watchdog timer	2^{12}/HCLK (Approx. 1.02 ms)	Count-up clock for watchdog timer
	2^{14}/HCLK (Approx. 4.1 ms)	
	2^{16}/HCLK (Approx. 16.38 ms)	
	2^{19}/HCLK (Approx. 131.07 ms)	

HCLK : Oscillator clock frequency
Values in parentheses ( ) are when oscillator clock frequency is 4 MHz.

Reference : Immediately after oscillation begins, the oscillation cycles are unstable; oscillation stabilization standby is a rough measure of the time for oscillation to become stable.

- **Block Diagram of Timebase Timer**



— : Undefined bit
OF : Overflow
*1 : Switching of machine clock from main clock to PLL clock
*2 : Interrupt number

4. Watchdog Timer

The watchdog timer is a two-bit timer that uses the output of the timebase timer as a count clock. When the watchdog timer is started, if it is not cleared within the set interval, the CPU is reset.

- **Watchdog Timer Function**

The watchdog timer detects runaway programs. When the watchdog timer is started, it must be cleared within a set interval. If a program enters an infinite loop, or for some other reason the watchdog timer is not cleared within the minimum time, a watchdog reset is generated to the CPU, sending it to a reset state. The watchdog timer interval is set by the interval time setting bits (WT1 and WT0) of the watchdog timer control register (WDTC) .

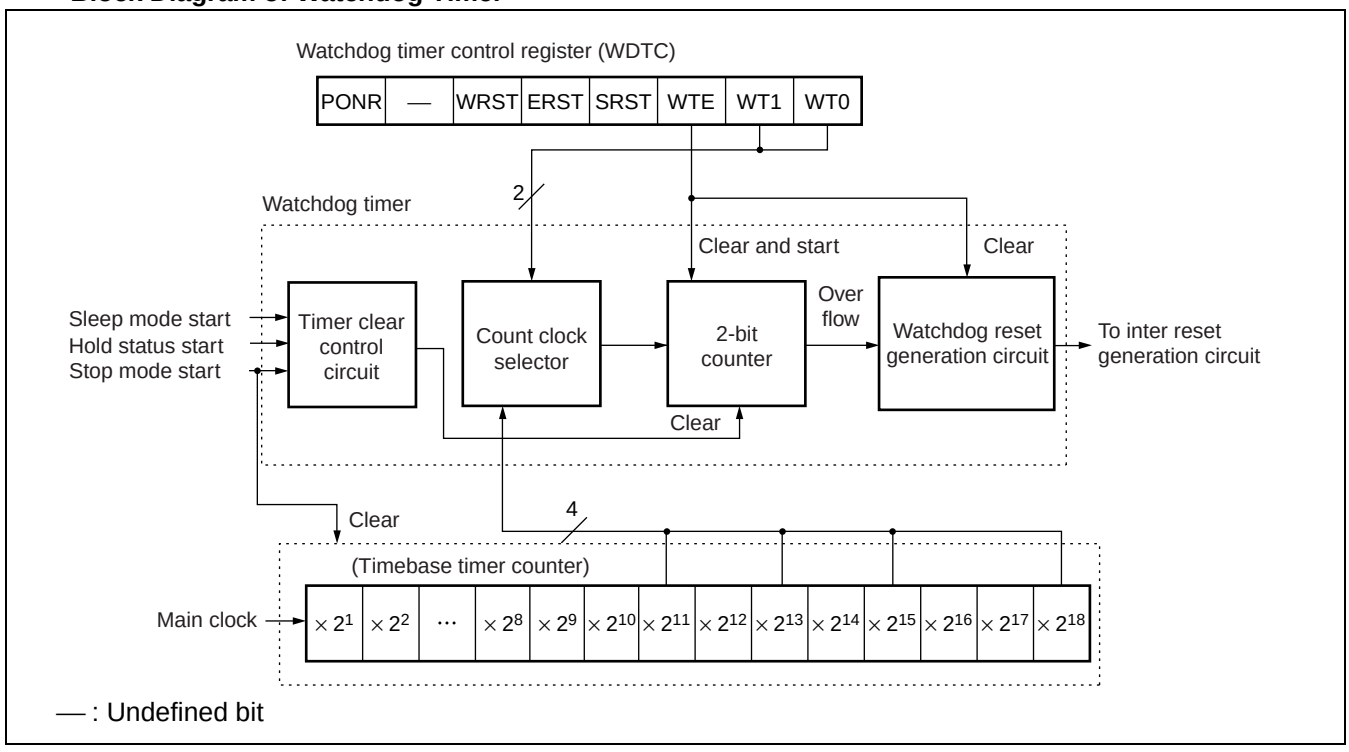
WT1	WT0	Interval Times		
		Minimum*	Maximum*	Oscillator clock cycles
0	0	Approx. 3.59 ms	Approx. 4.61 ms	$2^{14} \pm 2^{11}$ cycles
0	1	Approx. 14.33 ms	Approx. 18.43 ms	$2^{16} \pm 2^{13}$ cycles
1	0	Approx. 57.34 ms	Approx. 73.74 ms	$2^{18} \pm 2^{15}$ cycles
1	1	Approx. 458.76 ms	Approx. 589.82 ms	$2^{21} \pm 2^{18}$ cycles

* : When oscillator clock frequency is 4 MHz.

Reference : After the watchdog timer is started, it can be halted via a power-on reset, or a reset by the watchdog timer. While an external reset, internal reset, setting the watchdog control bit (WTE) of the watchdog timer control register (WDTC) , or going to sleep or stop mode can clear the watchdog timer, these actions will not change the watchdog function setting, or halt the watchdog timer.

Note: The watchdog timer is made up of a two-bit timer that counts the carry signal of the timebase timer. Because the watchdog timer uses the carry signal of the timebase timer, if the timebase timer is cleared, then the watchdog reset interval may be longer than the set time.

- **Block Diagram of Watchdog Timer**



— : Undefined bit

5. 16-bit Reload Timer

The MB90M405 series has 3 built-in 16-bit reload timer channels. They can be configured with the following clock modes and counter operation modes :

- **Clock Modes**
- Internal Clock Mode : In this mode, the timer counts down in synchronization with the internal clock
- Event Count Mode : In this mode, the timer counts down in accordance with external input pulses
- **Counter Operation Modes**
- Reload Mode : In this mode, the count setting is reloaded, and the count is repeated
- One-shot Mode : In this mode, the count is halted due to an underflow
- **16-bit Reload Timer Operation Modes**

Clock Mode	Counter Operation Mode	Operation Mode
Internal Clock Mode	Reload mode	Software trigger operation External trigger operation External gate input operation
	One-shot mode	
Event Count Mode (External Clock Mode)	Reload mode	Software trigger operation
	One-shot mode	

- **Internal Clock Mode**

When the count clock setting bits (CSL1, CSL0) of the timer control status register (TMCSR) are set to "00_B", "01_B", or "10_B", the mode is set to internal clock mode. In internal clock mode, the following operation modes can be set :

- Software trigger operation
  If the count enable bit (CNTE) of the timer control status register (TMCSR) is set to "1", setting the software trigger bit (TRG) to "1" will initiate count operation.
- External trigger input operation
  If the count enable bit (CNTE) of the timer control status register (TMCSR) is set to "1", then when a valid edge (rising, falling, or both edges can be set) set beforehand in the operation mode setting bits (MOD2, MOD1, MOD0) is input to the TIN pin, count operation is initiated.
- External gate input operation
  If the count enable bit (CNTE) of the timer control status register (TMCSR) is set to "1", then count operation is conducted while a valid gate input level ("L" or "H" can be set) set beforehand in the operation mode setting bits (MOD2, MOD1, MOD0) is input to the TIN pin.

- **Event Count Mode (External Clock Mode)**

When the count clock setting bits (CSL1, CSL0) of the timer control status register (TMCSR) are set to "11_B", the mode is set to event count mode (external clock) . If the count enable bit (CNTE) is set to "1", then when a valid edge (rising, falling, or both edges can be set) set in the operation mode setting bits (MOD2, MOD1, MOD0) is input to the TIN pin, count operation is initiated. If an external clock is input at set intervals, then it can also be used as an interval timer.

- **Counter Operation**
- Reload mode

  When the 16-bit down counter underflows (“0000_H” to “$FFFF_H$”) , the value of the 16-bit reload register (TMRLR) is loaded into the 16-bit down counter, and count operation is conducted. In addition, when an underflow occurs an interrupt request is output, so this can also be used as an interval timer. It is possible to output the inverted toggle waveform from the TO pin with each underflow.

Count Clock	Count Clock Cycle	Interval Time
Internal Count Clock	$2^1/\phi$ (0.125 µs)	0.125 µs to 8.192 ms
	$2^3/\phi$ (0.5 µs)	0.5 µs to 32.768 ms
	$2^5/\phi$ (2.0 µs)	2.0 µs to 131.1 ms
External Count Clock	$2^3/\phi$+ (0.5 µs)	0.5 µs +

ϕ : Machine clock frequency
Values in parentheses ( ) are when machine clock frequency is 16 MHz.

- One-shot mode

When the 16-bit down counter underflows (“0000_H” to “$FFFF_H$”) , count operation is halted.

Reference :

- 16-bit reload timer 0 can be used to create the UART baud rate.
- 16-bit reload timer 1 can be used as the start trigger for the A/D converter.

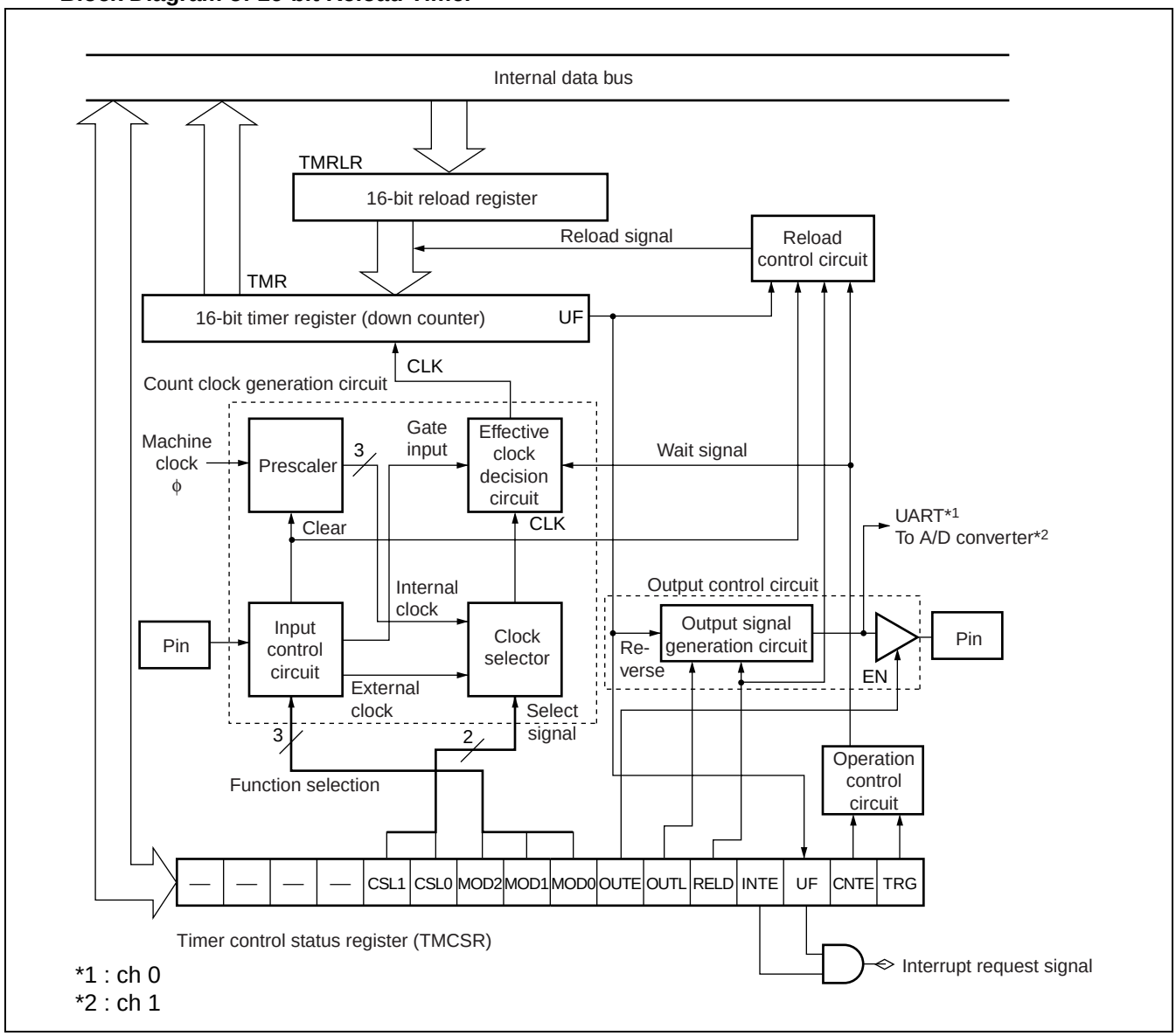
- **16-bit Reload Timer Interrupts and EI²OS**

When the 16-bit down counter underflows (“0000_H” to “$FFFF_H$”) , an interrupt request is output.

Channel	Interrupt No.	Interrupt Control Register		Vector Table Address			EI²OS
		Register Name	Address	Lower	Upper	Bank	
16-bit reload timer 0	#23 (17_H)	ICR06	$0000B6_H$	$FFFFA0_H$	$FFFFA1_H$	$FFFFA2_H$	△
16-bit reload timer 1	#24 (18_H)			$FFFF9C_H$	$FFFF9D_H$	$FFFF9E_H$	
16-bit reload timer 2	#21 (15_H)	ICR05	$0000B5_H$	$FFFFA8_H$	$FFFFA9_H$	$FFFFAA_H$	

△ : Available if interrupt factors sharing ICR are not used

- **Block Diagram of 16-bit Reload Timer**



6. 16-bit I/O Timers

The 16-bit I/O timer can perform dual independent waveform output, input pulse width measurement, and external clock cycle measurement, based on the 16-bit freerun timer.

- **16-bit freerun timer (1 channel)**

The 16-bit freerun timer is made up of a 16-bit up counter (timer counter data register (TCDT)) , timer counter control status register (TCCS) , and prescaler. The counter output value of the 16-bit freerun timer is used as the base timer for output comparison and input capture.

- Counter operation clock (4 different settings available)
  4 internal clock types : ϕ/4, ϕ/16, ϕ/32, ϕ/64
  ϕ : Machine clock frequency
- Interrupt
  An interrupt can be output to the CPU when the counter value overflows, or when it matches the value of comparison register 0.
- Initialize
  When a reset is input, if the software reset bit is cleared to “0”, or if the values of comparison register 0 and the freerun timer count match, the counter value can be initialized to “0000_H”.

- **Output compare (1 channel)**

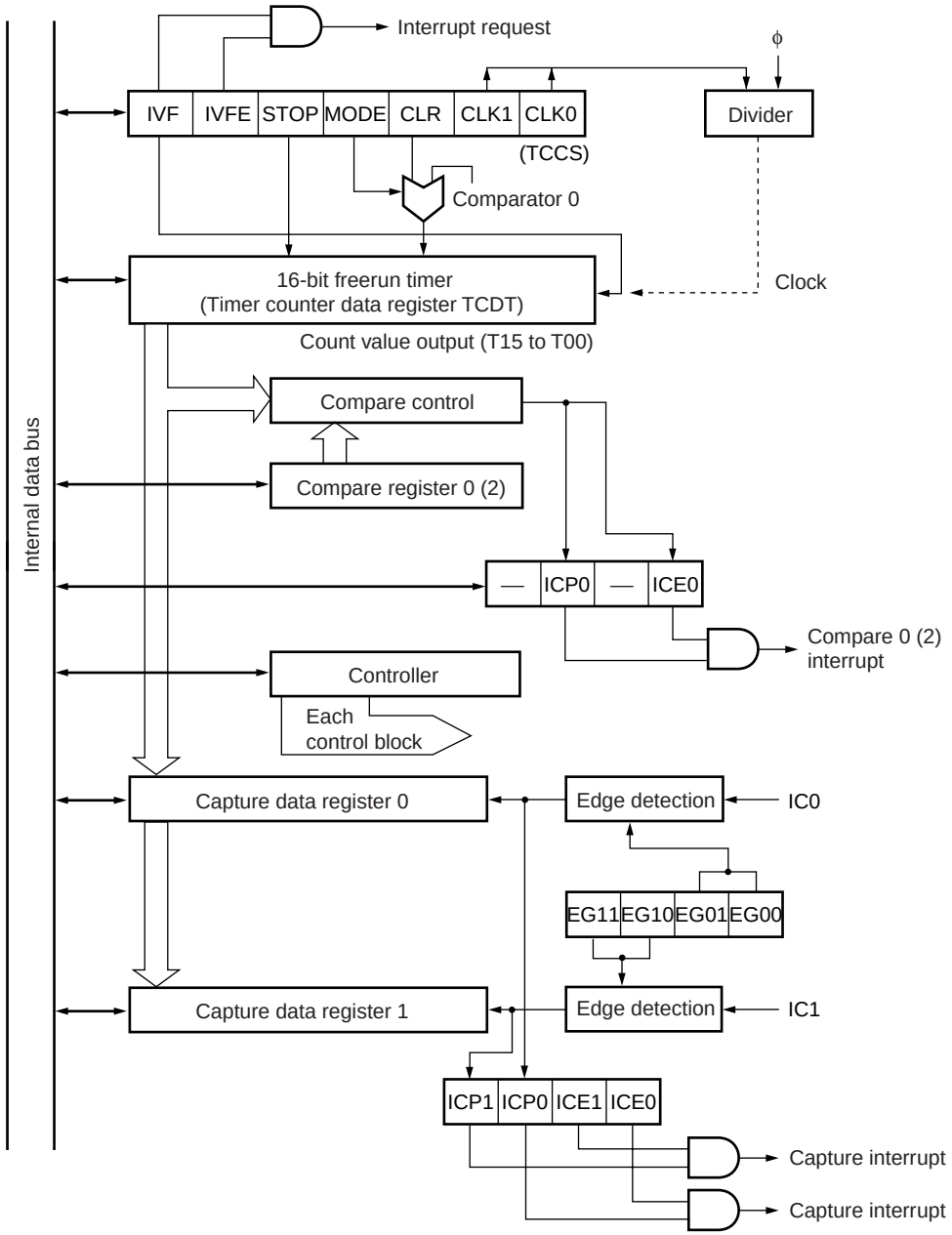
The output comparison module consists of a 1-channel 16-bit comparison register, and control register. If the value of the 16-bit freerun timer and that of the compare register match, an interrupt request can be output to the CPU.

- **Input capture (2 channels)**

The input capture module consists of a capture register and a control register. Both support two independent external input pin channels. The capture register can store the value of the 16-bit freerun timer. Additionally, the register can detect signal input edges from external pins, and simultaneously output interrupts to the CPU.

- The detection edge of the external input signal can be configured (rising edge, falling edge, both edges)
- The two input capture channels can operate independently
  Interrupts can be output upon detection of a valid edge in an external input signal
- Input capture interrupts start the extended intelligent I/O service

- **Block Diagram of 16-bit I/O Timer**



7. UART

The UART is a general-purpose serial data communications interface for both synchronous and asynchronous (start-stop synchronization) communications with external devices. Two types of communication are available: two-way communication (normal mode) and master/slave communication (multiprocessor mode; only the master side is supported) .

• UART Functions

The UART is a general-purpose serial data communications interface for sending and receiving serial data to and from other CPUs and peripheral devices. It provides the following functions:

	Function
Data Buffer	Full-duplex double buffer
Transfer Mode	• Clock-synchronous (no start/stop bit) • Clock-asynchronous (start-stop synchronization)
Baud Rate	• Max 2 MHz (with machine clock at 16 MHz) • Baud rate via dedicated baud rate generator • Baud rate via external clock (SC pin input clock) • Baud rate via internal clock (clock supplied from 16-bit reload timer) • Total of 8 types of baud rate may be set
Data Length	• 7 bits (in asynchronous normal mode only) • 8 bits
Signal Format	NRZ (Non Return to Zero)
Receive Error Detection	• Framing errors • Overrun errors • Parity errors (undetectable in multiprocessor mode)
Interrupt Requests	• Receive interrupts (receive complete, receive error detection) • Send interrupts (send complete) • Extended intelligent I/O service (EI^{2}OS) supported for both sending and receiving
Master/Slave Communications Function (Multiprocessor Mode)	Enables 1 (master) to n (slave) communication (Only master side supported)

Note : The UART does not add a start or stop bit during clock-synchronous transfer. Only the data is forwarded.

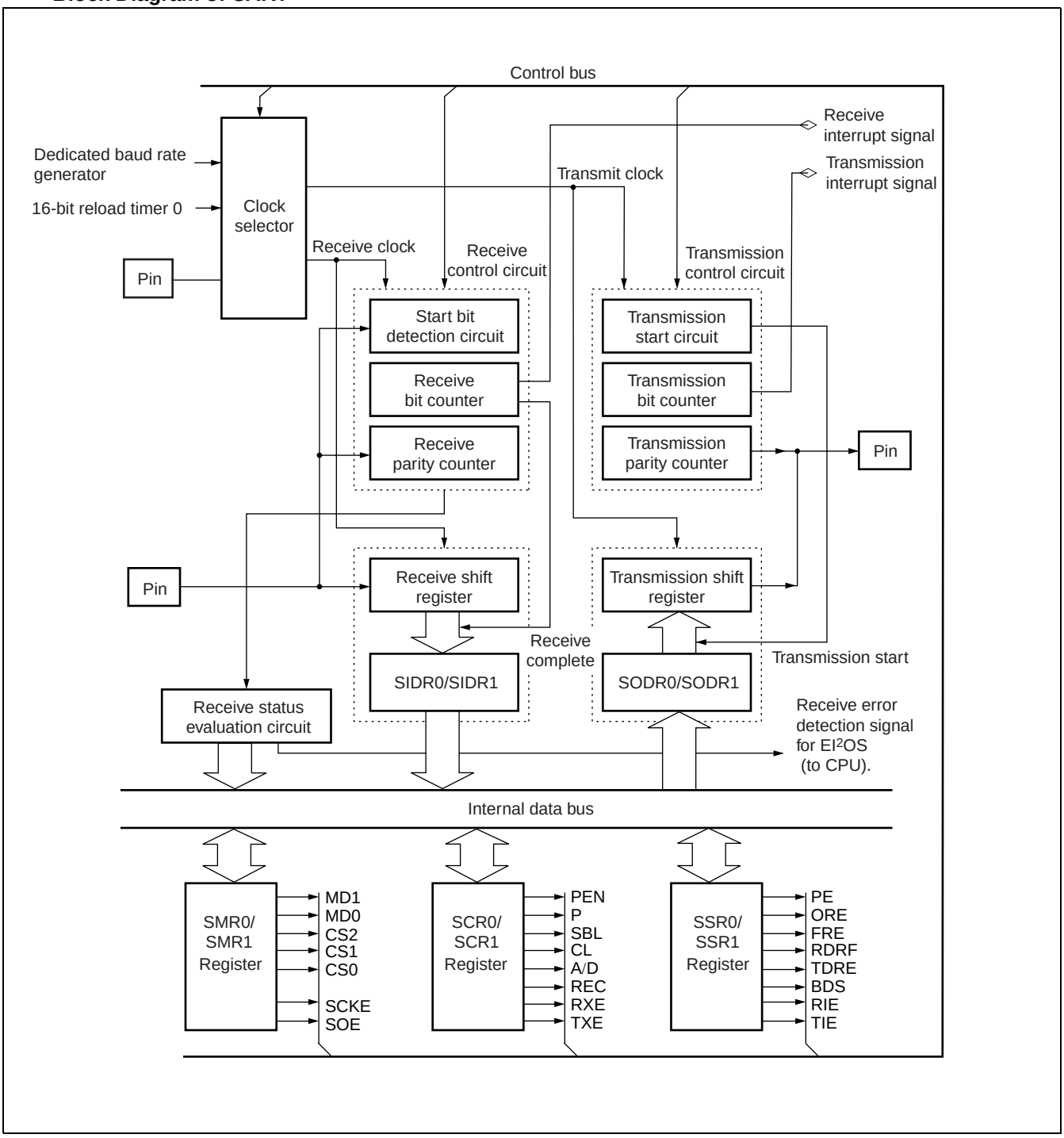
Operation Mode		Data Length		Synchronization	Stop Bit Length
		No Parity	With Parity		
0	Normal Mode	7 bits or 8 bits		Asynchronous	1 bit or 2 bits*2
1	Multiprocessor Mode	8 + 1*1	—	Asynchronous	
2	Normal Mode	8	—	Synchronous	None

— : Not available

*1 : “+1” is the address/data setting bit (A/D) used for communications control.

*2 : During reception, only a stop bit length of 1 can be detected.

- **Block Diagram of UART**



8. DTP/External Interrupt Circuit

The DTP (Data Transfer Peripheral) /external interrupt circuit detects interrupt requests input from the external interrupt input pin, and outputs interrupt requests.

- **DTP/External Interrupt Function**

The DTP/external interrupt circuit outputs interrupt requests upon detection of an edge input from the external interrupt input pin, or a level signal. Interrupt requests are accepted by the CPU, and if extended intelligent I/O service (EI²OS) is enabled, the CPU conducts automated data transfer (DTP function) via EI²OS, then branches into an interrupt processing routine. If EI²OS is disabled, the CPU branches into an interrupt processing routine, without starting automated data transfer (DTP function) via EI²OS.

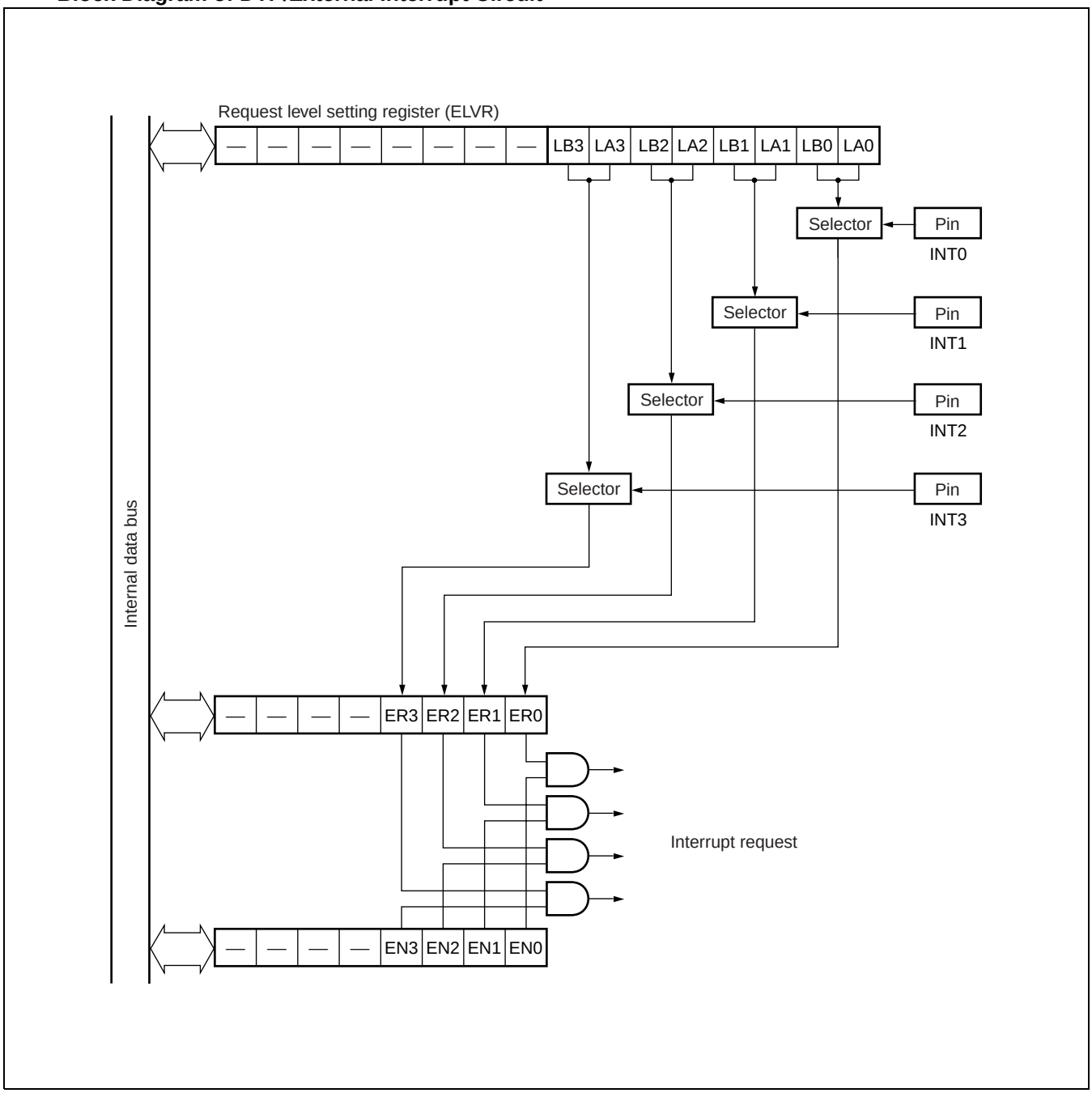
	External Interrupt Function	DTP Function
Input pins	4 channels (P80/INT0, P81/INT1, PB6/INT2, PB7/INT3)	
Interrupt conditions	The level or edge to detect can be set independently for each pin in the detection level setup register (ELVR)	
	"L" level/"H" level input	Rising edge/falling edge input
Interrupt number	#11 ($0B_H$), #13 ($0D_H$) , #16(10_H)	
Interrupt control	Enable/disable interrupt request output in the DTP/external interrupt enable register (ENIR)	
Interrupt flag	The DTP/interrupt factor register (EIRR) stores interrupt conditions.	
Processing selection	Set EI²OS to disabled (ICR : ISE = "0")	Set EI²OS to enabled (ICR : ISE = "1")
Operation	Branch to interrupt processing routine	Branch to interrupt processing routine after automatic data transfer by EI²OS completes.

ICR : Interrupt Control Register

- **DTP/External Interrupt Circuit Interrupts and EI²OS**

Channel	Interrupt No.	Interrupt Control Register		Vector Table Address			EI²OS
		Register Name	Address	Lower	Upper	Bank	
INT0	#11 ($0B_H$)	ICR00	$0000B0_H$	$FFFFD0_H$	$FFFFD1_H$	$FFFFD2_H$	○
INT1	#13 ($0D_H$)	ICR01	$0000B1_H$	$FFFFC8_H$	$FFFFC9_H$	$FFFFCA_H$	
INT2	#16 (10_H)	ICR02	$0000B2_H$	$FFFFBC_H$	$FFFFBD_H$	$FFFFBE_H$	
INT3							

- **Block Diagram of DTP/External Interrupt Circuit**



- DTP/External Interrupt Input Detection Circuit
  If a signal input to the external interrupt input pin matches the level set in the request level setting register (ELVR) or edge, the DTP/external interrupt factor flag bit (EIRR : ER3 to ER0) corresponding to the external interrupt input pin is set to “1”.
- Request Level Setting Register (ELVR)
  The interrupt request detection conditions (level or edge) are set for each external interrupt input pin
- DTP/External Interrupt Factor Register (EIRR)
  Stores and clears interrupt factors
- DTP/External Interrupt Enable Register (ENIR)
  Interrupt requests are enabled/disabled for each external interrupt input pin.

9. I²C Interface

The I²C interface is a serial I/O port that supports the Inter IC BUS. It operates as a master/slave device on an I²C bus, with the following features :

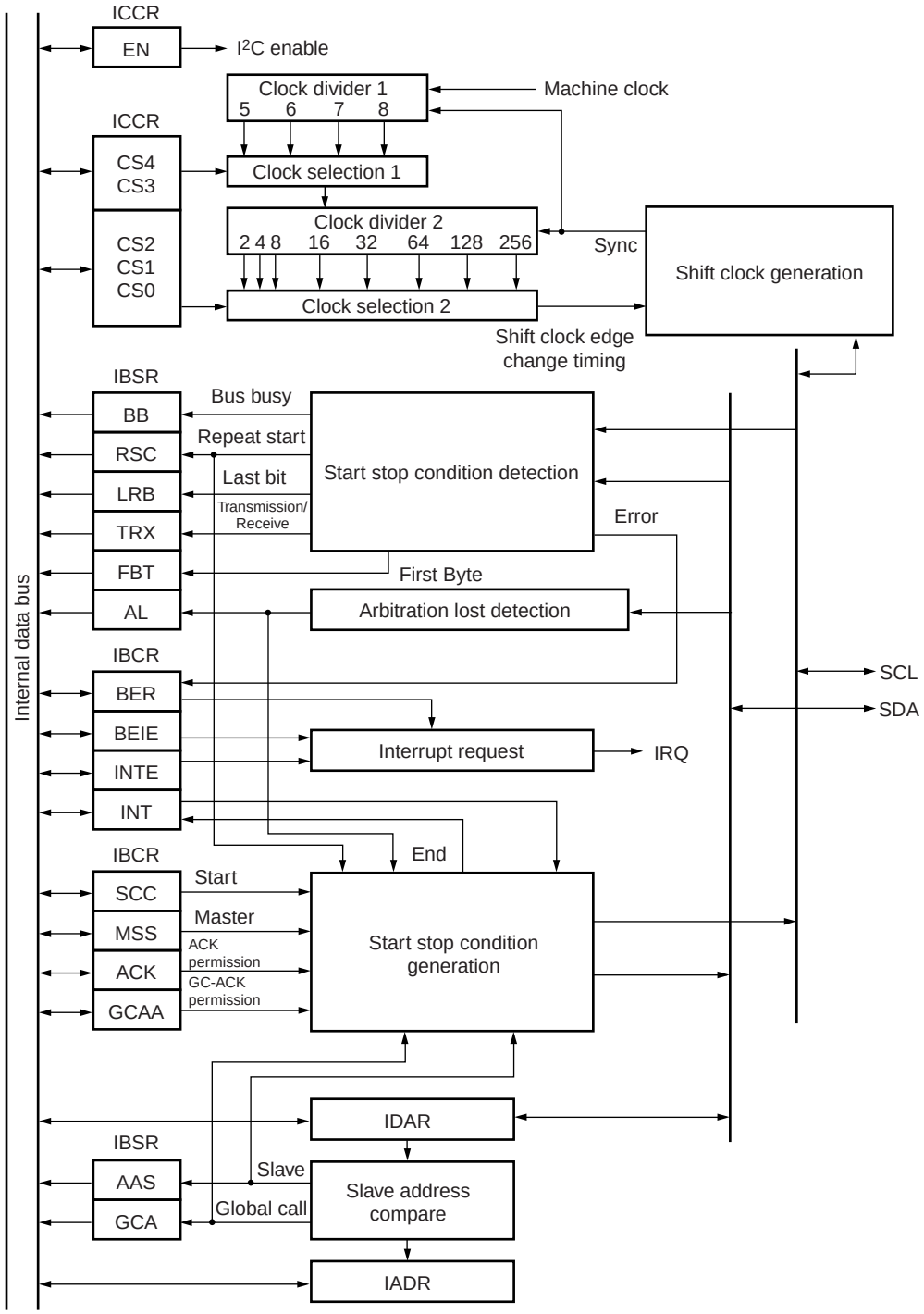
- **I²C Interface Features**

The MB90M405 series has one I²C interface channel.

Below are features of the I²C interface :

- Master/slave send/receive
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transfer direction detection function
- Start condition loop generation and detection function
- Bus error detection function
- Transfer rates of up to 100 Kbps supported

- **Block Diagram of I²C Interface**



10. 8/10 Bit A/D Converter

The 8/10 bit A/D converter has a function to convert analog input voltage to a 10 or 8-bit value using the RC successive approximation conversion method.

- **8/10 Bit A/D Converter Functions**

Below are the functions of the 8/10 bit A/D converter :

- The minimum conversion time is 6.125 µs (with machine clock frequency of 16 MHz, including sampling time)
- The minimum sampling time is 2 µs (with machine clock frequency of 16 MHz)
- The RC successive approximation conversion method with sample-hold circuit is used for conversion
- Resolution can be set to 10 or 8 bits
- Input signal programmable from 8-channel analog input pins
- When A/D conversion is completed, it is possible to output an interrupt request, and start EI^{2}OS
- In an interrupt-enabled state, when A/D conversion is executed, a conversion data protection function is invoked
- The conversion start factor can be set to software or 16-bit reload timer 1 output (rising edge)

The following 4 conversion modes are available :

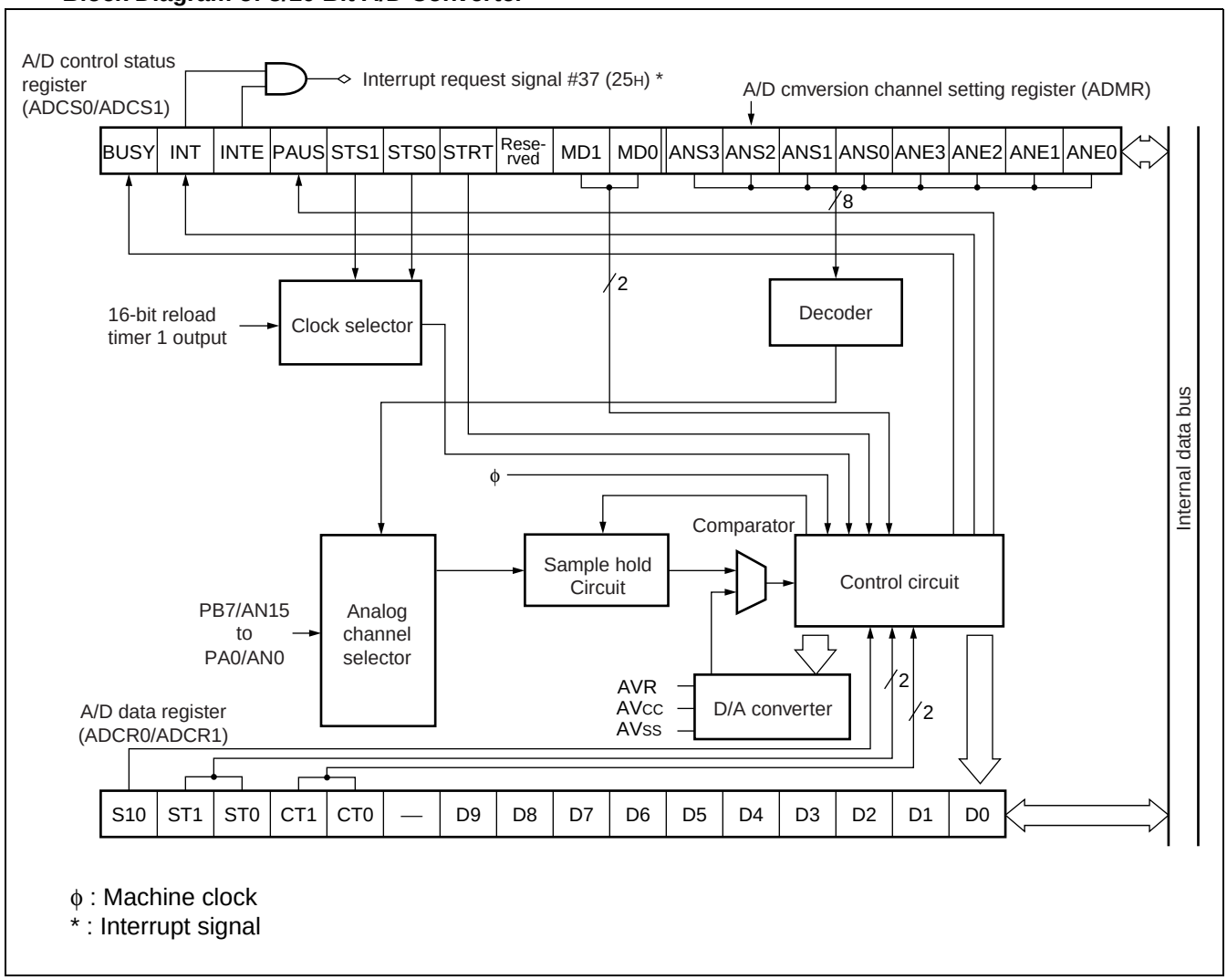
Conversion Mode	Single Conversion Operation	Scan Conversion Operation
One-shot Conversion Mode 1 One-shot Conversion Mode 2	The set channel performs conversion once, then stops	Multiple linked channels (up to 16 channels can be set) perform conversion once, then stop
Continuous Conversion Mode	The set channel performs conversion repeatedly	Multiple linked channels (up to 16 channels can be set) perform conversion repeatedly
Stop Conversion Mode	The set channel performs conversion once, then pauses, and goes into standby until started again	Multiple linked channels (up to 16 channels can be set) perform conversion once, then pause, and go into standby until started again

- **8/10 Bit A/D Converter Functions Interrupts and EI^{2}OS**

Interrupt No.	Interrupt Control Register		Vector Table Address			EI^{2}OS
	Register Name	Address	Lower	Upper	Bank	
#37 (25$_H$)	ICR13	0000BD$_H$	FFFF68$_H$	FFFF69$_H$	FFFF6A$_H$	○

○ : Available

- **Block Diagram of 8/10 Bit A/D Converter**



ϕ : Machine clock
* : Interrupt signal

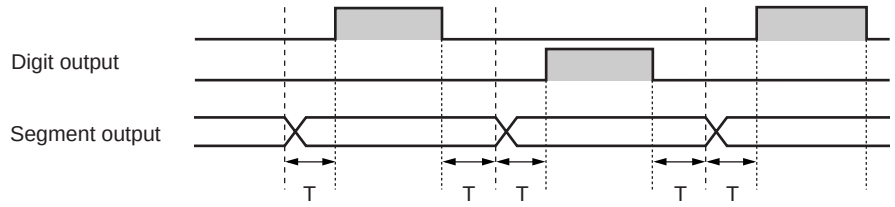
- A/D control status register 0/1 (ADCS0/ADCS1)
  The A/D control status register 1 (ADCS1) has functions to set the A/D conversion start factor, enable/disable interrupt requests, check the status of interrupt requests, and check whether A/D conversion is halted/ongoing.
- A/D data register (ADCR0/ADCR1)
  This register stores the results of A/D conversion. It has functions to set the A/D conversion resolution, A/D conversion sampling time, and A/D conversion comparison time.
- A/D conversion channel setting register (ADMR)
  Provides a function to set the A/D conversion start/stop channel
- Clock selector
  This selector sets the A/D conversion start clock. The 16-bit reload timer 1 output can be set in the start clock.
- Decoder
  This circuit sets the analog input pin to use from the setting of the A/D conversion end channel setting bit (ANE0 to ANE3) and A/D conversion start channel setting bit (ANS0 to ANS3) of the A/D control status register (ADCS0) .

11. FL-control Circuit

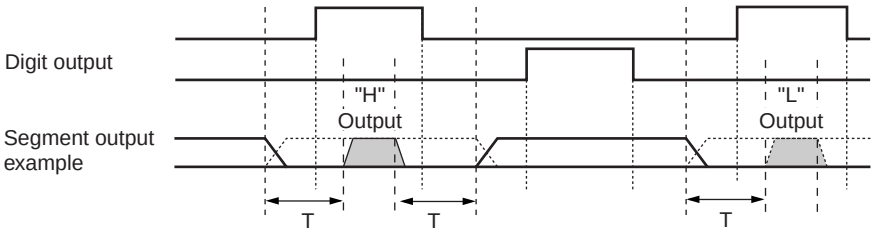
The FL control circuit has a fluorescent tube automated display function and an LED automated display function. The fluorescent tube automated display function is capable of up to 32 digits, and 60 combined segment and digit automated display. The LED automated display function can output LED1 pin to LED16 pin at 1/2 duty, with LED0 pin as common output.

- **High voltage resistance output pins**
- There are 60 onboard high voltage resistance output pins (FIP0 pin to FIP59 pin) .
- There are 34 high-current output pins (FIP0 pin to FIP33 pin) and 26 mid-current output pins (FIP34 pin to FIP59 pin) .
- Pull-down resistance can be set for all high voltage-resistance output. Alternately, they can be combined.
- **Fluorescent tube automated display function**
- Has 32 × 60-bit display data RAM.
- The display timing can be set to between 1 and 32.
- 60 bits can be set for both digits and segments for each timing.
- The digit pins are FIP0 pin to FIP31 pin; from the pin set for digit start, the digits can be set in series for the number of pins set in the digit number register.
- Segments can control up to 59 outputs.
- There are 4 types of display scan cycle (segment width) .
- Digit dimmer control controls the T on both sides of the digit for segment output. Adjustment is available in 7 steps (dimmer applied to all digits) .
- All digit and segment can be inverted.
- Segment output of an arbitrary timing is capable of gradated display (segment dimmer) . The T of both sides of the segment are as follows :

Digit Dimmer Control



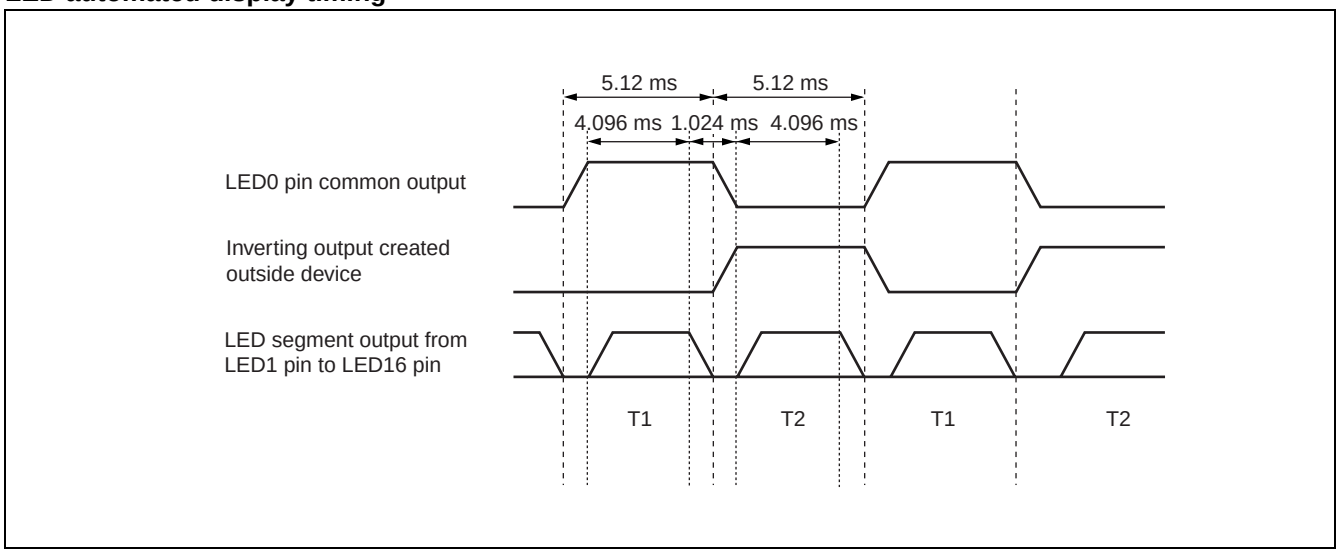
Segment Dimmer Control



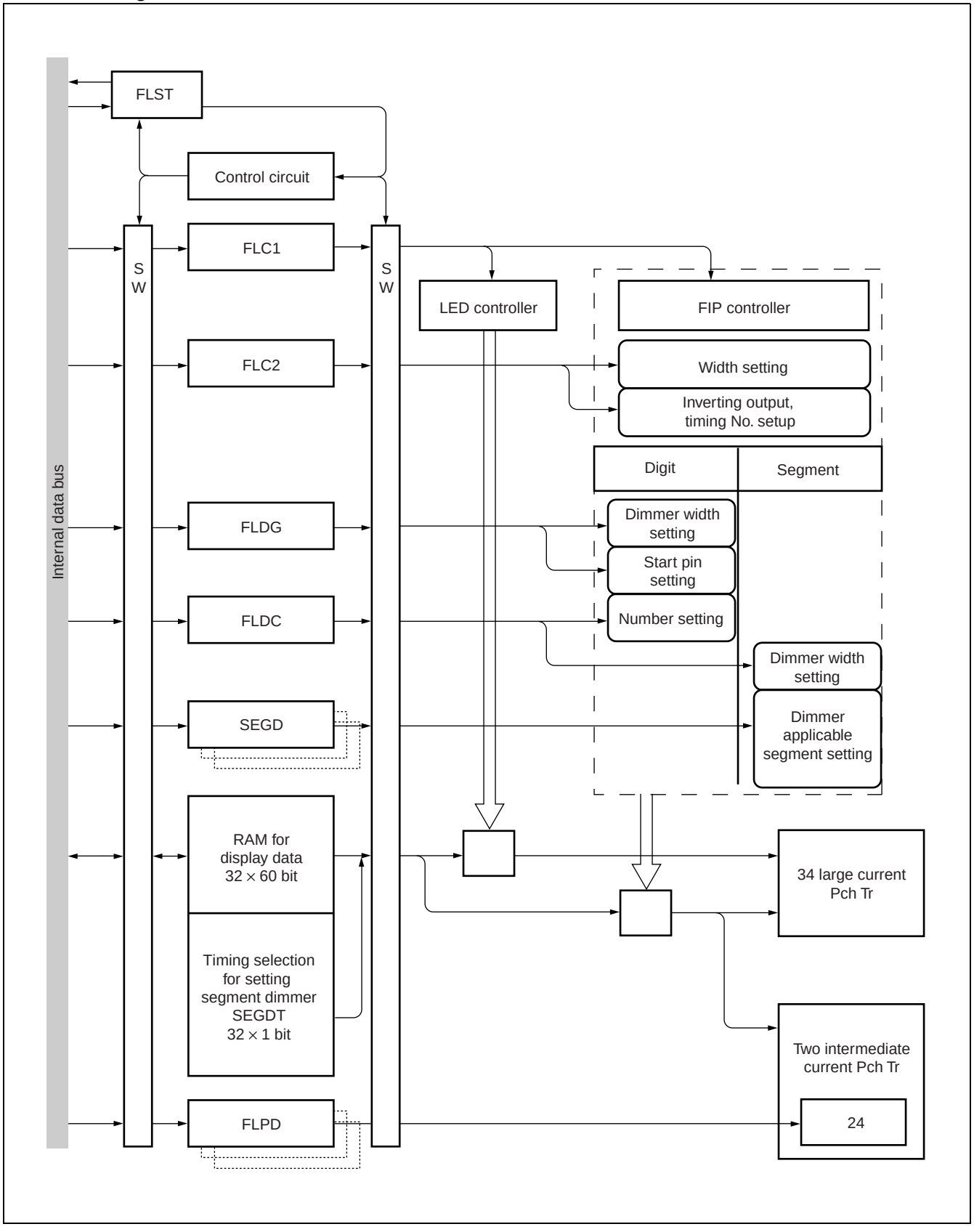
Note : Dimmer can be applied to a defined segment in the setup timing.

- **LED automated display function**
- Pins between LED0 pin and LED16 pin not set to digits can be set as LED pins.
- As shown in the figure below, LED0 pin becomes common output, and LED1 pin to LED16 pin become LED segment output.
- When LED0 pin is set to “H”, the values corresponding to LED1 pin to LED16 pin are output at the timing T1 in display data RAM; when LED0 pin is set to “L”, the values corresponding to LED1 pin to LED16 pin are output at the timing T2 in display data RAM.
- 1/2 duty LED output can be obtained by externally inverting the LED0 pin common output.
- As shown below, the output timing of LED1 pin to LED16 pin from LED0 pin and the inverted signal of LED0 pin is 5.12 ms for LED0 pin, and 4.096 ms for LED1 pin to LED16 pin (when machine clock (peripheral operation clock) frequency is 16 MHz) .

LED automated display timing



- **Block Diagram of FL Control Circuit**



12. Time Clock Output

The time clock output circuit divides the oscillator clock by means of the timebase timer, and outputs the set division clock. Can be set to 1/32, 1/64, 1/128, or 1/256 of oscillator clock.

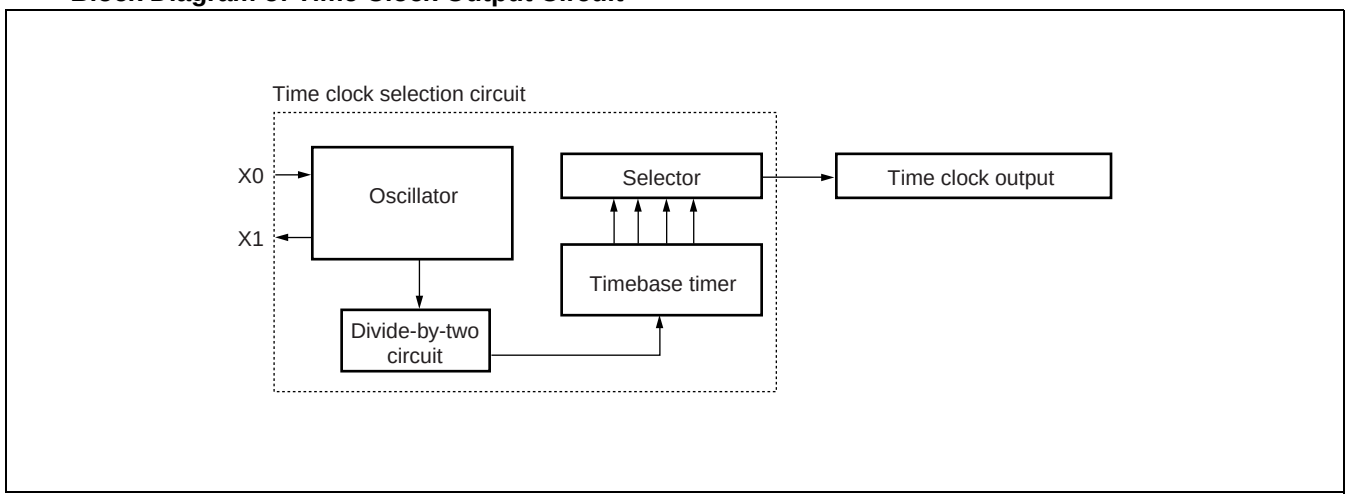
- **Time clock output circuit**

The timer clock output circuit is disabled in reset and stop modes. It is enabled in normal run modes, sleep mode, and pseudo clock mode.

	PLL_Run	Main_Run	Sleep	Pseudo Clock	STOP	Reset
Operating State	○	○	○	○	×	×

If the timebase timer is cleared while the time clock output circuit is in use, clock output cannot be conducted normally.

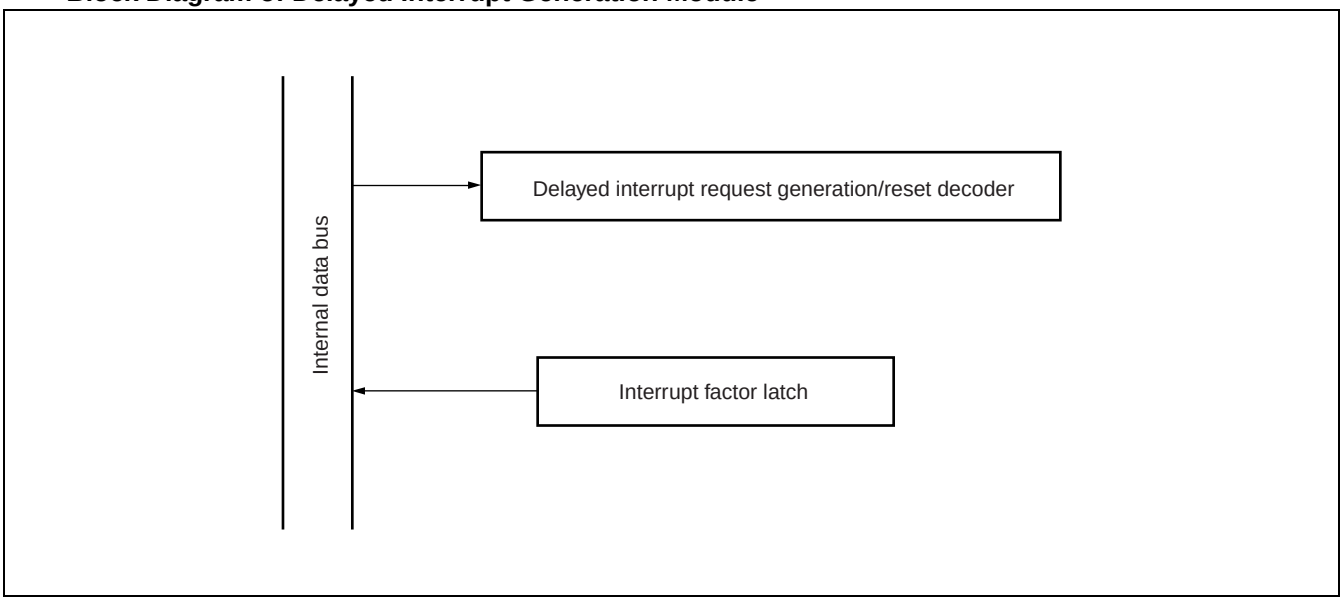
- **Block Diagram of Time Clock Output Circuit**



13. Delayed Interrupt Generation Module

The delayed interrupt generation module outputs task switching interrupt requests. When the delayed interrupt generation module is used, it is possible to output interrupt requests and releases to an MB90M405 series CPU via the software for task switching.

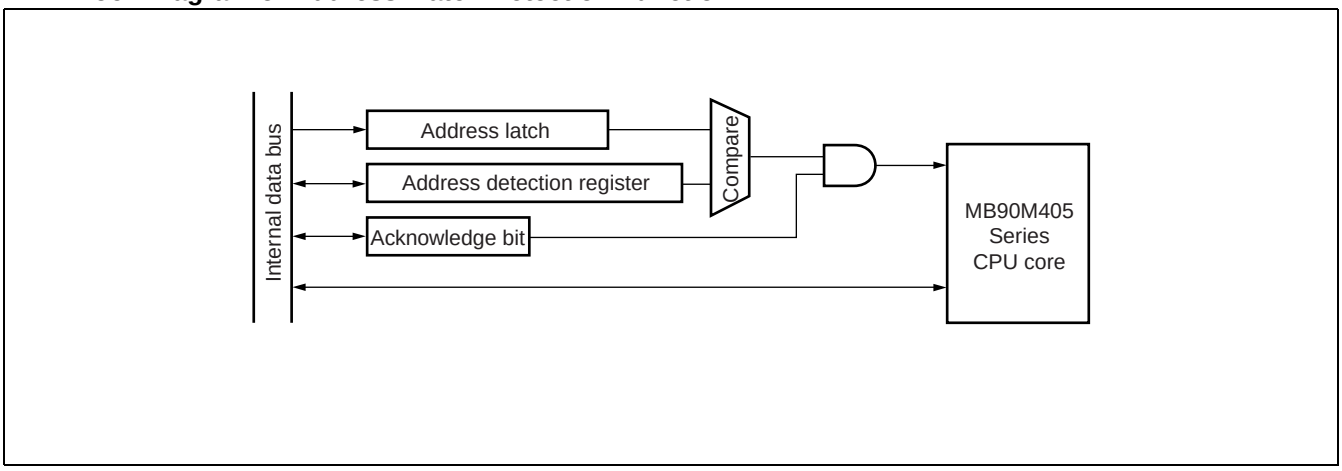
- **Block Diagram of Delayed Interrupt Generation Module**



14. Address Match Detection Function

If a program address matches the value set in the address match detection register, the instruction code read into the CPU is changed to an INT9 instruction code. It is possible to realize a program patch assignment function by processing an INT #9 interrupt routine.

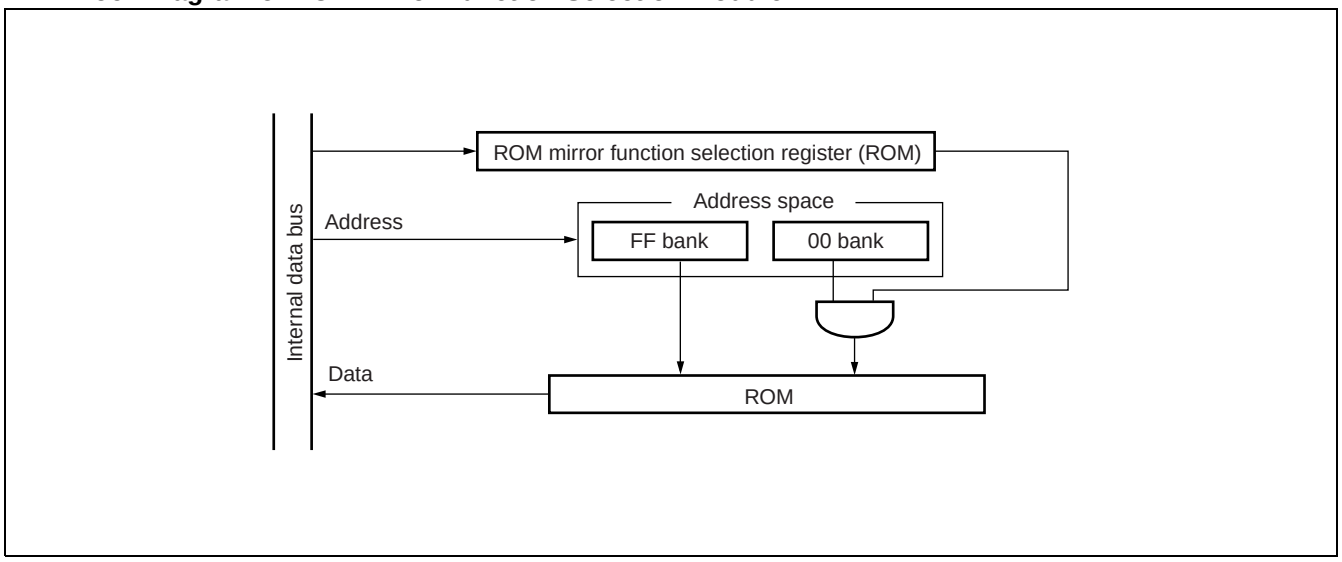
- **Block Diagram of Address Match Detection Function**



15. ROM Mirror Function Selection Module

The ROM Mirror Function Selection Module allows the ROM data of bank FF to be viewed from bank 00, by setting the ROM mirror function selection module register. Using the ROM mirror function makes it possible to access the corresponding area (“FF4000$_H$” to “FFFFFF$_H$”) from the I/O and RAM areas, without crossing banks.

- **Block Diagram of ROM Mirror Function Selection Module**



16. 1 Mbit Flash Memory

The 1 Mbit flash memory is arrayed on the CPU memory map in banks FE_H to FF_H. It allows read and program access from the CPU in the same manner as mask ROM. Data is written to and deleted from flash memory by means of instructions from the CPU, via the flash memory interface circuit. This allows the implementation state to be overwritten via onboard CPU control, allowing programs and data to be modified efficiently.

- **1 Mbit Flash Memory Length**
- 128 Kword × 8/64 Kword × 16 bit (16 K + 8 K + 8 K + 32 K + 64 K) sector configuration.
- Automated program algorithm (same as Embedded Algorithm* : MBM29F400TA)
- Built-in deletion pause/resume function
- Write/deletion completion detection by CPU interrupt
- JEDEC standard command compatible
- Sector-by-sector deletion possible (sectors can be combined freely)
- Write/deletion guaranteed through 10,000 iterations

* : Embedded Algorithm is a trademark of Advanced Micro Device.

- **Method for Writing to and Deleting Flash Memory**

There are two methods for writing to/deleting from flash memory :

1. Dedicated serial writer
   (YDC AF220)
   YDC: Yokogawa Digital Computer

2. Writing/deletion via program execution

It is not possible to simultaneously write to and read from flash memory. When writing to/deleting from flash memory, programs in flash memory are temporarily copied to RAM, and run from there; this allows data to be written to flash memory.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS}-CPU = V_{SS}-IO = AV_{SS} = 0.0 V)

Parameter	Signal	Rating		Unit	Remarks
		Min	Max		
Power Supply Voltage	V_{CC}-CPU	V_{SS} – 0.3	V_{SS} + 4.0	V	Control circuit power pin
	V_{DD}-FIP	V_{SS} – 0.3	V_{SS} + 4.0	V	FIP power pin
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	$V_{CC} \geq AV_{CC}$*1
	V_{KK}	V_{CC} – 45	V_{CC} + 0.3	V	Power supply pin of pull-down side during high voltage resistant output
Input Voltage	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
	V_{I2}	V_{SS} – 0.3	V_{SS} + 5.5	V	*3
Output Voltage	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
	V_{O2}	V_{SS} – 0.3	V_{SS} + 5.5	V	*3 (open drain output)
“L” Level Maximum Output Current	I_{OL}	—	15	mA	*4, *5
“L” Level Average Output Current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate) *5
“L” Level Maximum Overall Output Current	ΣI_{OL}	—	100	mA	*5
“L” Level Average Overall Output Current	ΣI_{OLAV}	—	50	mA	Average value (operating current × operating rate) *5
“H” Level Maximum Output Current	I_{OH}	—	–15	mA	*4, *5
	I_{OHFIP1}	—	–27	mA	FIP0 to FIP33 pins
	I_{OHFIP2}	—	–14	mA	FIP34 to FIP59 pins
“H” Level Average Output Current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate) *5
“H” Level Maximum Overall Output Current	ΣI_{OH}	—	–100	mA	*5
“H” Level Average Overall Output Current	ΣI_{OHAV}	—	–50	mA	Average value (operating current × operating rate) *5
	$\Sigma I_{OHFIPAV}$	—	–180	mA	Average value (operating current × operating rate) *6
Consumption Power	P_{D_CPU}	—	300	mW	During CPU_Chip independent operation
	P_{D_FL}	—	1176	mW	During FL_Chip independent operation
Operating Temperature	Ta	–40	+85	°C	
Storage Temperature	Tstg	–55	+150	°C	

*1 : Make sure that AVcc does not exceed V_{CC} when applying power, etc.

*2 : V_I, V_O must not exceed V_{CC} + 0.3 V.

*3 : 5 V voltage resistant pin for I^2C. Only applies to P90/SDA and P91/SCL.

*4 : The standard for maximum output current is the peak value of a single corresponding pin.

*5 : Excludes current at pins FIP0 to FIP59.

*6 : Corresponds to pins FIP0 to FIP59.

Note : V_{CC} in the standard signifies V_{DD}-FIP = V_{CC}-CPU. Also, use the 3 pins on the left at the same power level. Here, V_{SS} signifies V_{SS}-IO = V_{SS}-CPU. Please connect this pin to GND as well.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0.0 V)

Parameter	Symbol	Values		Unit	Remarks
		Min	Max		
Power Voltage	V_{CC}-CPU	3.0	3.6	V	During normal operation
	V_{DD}-FIP	3.0	3.6	V	During normal operation
	V_{CC}	2.5	3.6	V	Save stop operation status
Input “H ” Voltage	V_{HIS}	0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input pin except I^2C
	V_{HIS2}	0.8 V_{CC}	V_{SS} + 5.0	V	I^2C CMOS hysteresis input pin (5 V voltage resistant)
	V_{HIM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
Input “ L” Voltage	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin except I^2C
	V_{ILS2}	V_{SS} – 0.3	0.2 V_{CC}	V	I^2C CMOS hysteresis input pin (5 V voltage resistant)
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
Operating Temperature	Ta	–40	+85	°C	

Note : V_{CC} in the standard signifies V_{DD}-FIP = V_{CC}-CPU. Also, use the 3 pins on the left at the same power level. Here, Vss signifies V_{SS}-IO = V_{SS}-CPU. Please connect this pin to GND as well.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Standard

($Ta = -40$ °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

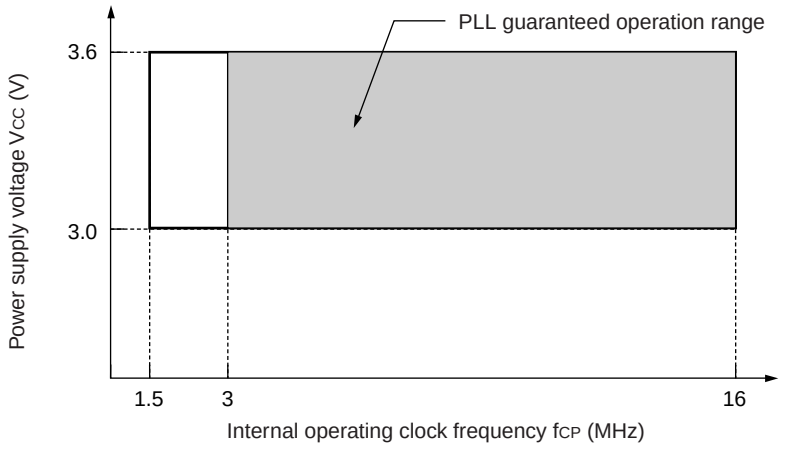
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output "H" Voltage	V_{OH5}	FIP0 - FIP33	I_{OH5} = –23 mA	V_{CC} – 2.5	—	—	V	
	V_{OH4}		I_{OH4} = –12 mA	V_{CC} – 1.3	—	—	V	
	V_{OH3}	FIP34 - FIP59	I_{OH3} = –12 mA	V_{CC} – 2.0	—	—	V	
	V_{OH2}		I_{OH2} = –5 mA	V_{CC} – 1.0	—	—	V	
	V_{OH1}	SDA/SCL	I_{OH1} = –4 mA	—	—	5.5	V	Open drain pin
	V_{OH0}	All output pins except for the above	I_{OH} = –2.0 mA	V_{CC} – 0.5	V_{CC} – 0.3	—	V	
Output "L" Voltage	V_{OL1}	SDA/SCL	I_{OL} = 15 mA	—	0.5	0.8	V	
	V_{OL}	All output pins except for the above	I_{OL} = 2.0 mA	—	0.2	0.4	V	
Input Leak Voltage	I_{IL}	All input pins except FIP0 - FIP59	V_{CC} = 3.0 V ($V_{SS} < V_I < V_{CC}$)	–5	–1	+5	µA	
Output Leak Voltage	I_{LO3}	FIP0 - FIP33	V_{KK} = V_{CC} to V_{CC} – 43	—	—	20	µA	
	I_{LO2}	FIP34 - FIP59	V_{KK} = V_{CC} to V_{CC} – 43	—	—	10	µA	
Power Current	I_{CC}	V_{CC}	V_{CC} = 3.3 V Internal frequency 16 MHz During normal operation	—	32	40	mA	MB90M407/A* MB90M408/A*
			V_{CC} = 3.3 V Internal frequency 16 MHz During A/D operation	—	37	45	mA	MB90M407/A* MB90M408/A*
			V_{CC} = 3.3 V Internal frequency 16 MHz During normal operation	—	40	50	mA	MB90MF408/A MB90MV405*
			V_{CC} = 3.3 V Internal frequency 16 MHz During A/D operation	—	45	55	mA	MB90MF408/A MB90MV405*
			Flash memory During write/deletion	—	40	50	mA	MB90MF408/A
	I_{CCS}		V_{CC} = 3.3 V Internal frequency 16 MHz During sleep	—	15	20	mA	*
	I_{CCH}		During stop, Ta = +25 °C	—	15	20	µA	
Pull-up Resistance	R_{UP}	$\overline{RST}$	—	20	65	200	kΩ	
Pull-down Resistance	R_{DW1}	MD2	—	20	65	200	kΩ	
	R_{DW1}	FIP0 - FIP59	When set	80	120	160	kΩ	

* : The standard current values do not include current consumption by the high voltage resistance pins. This indicates the current consumption of the internal circuit.

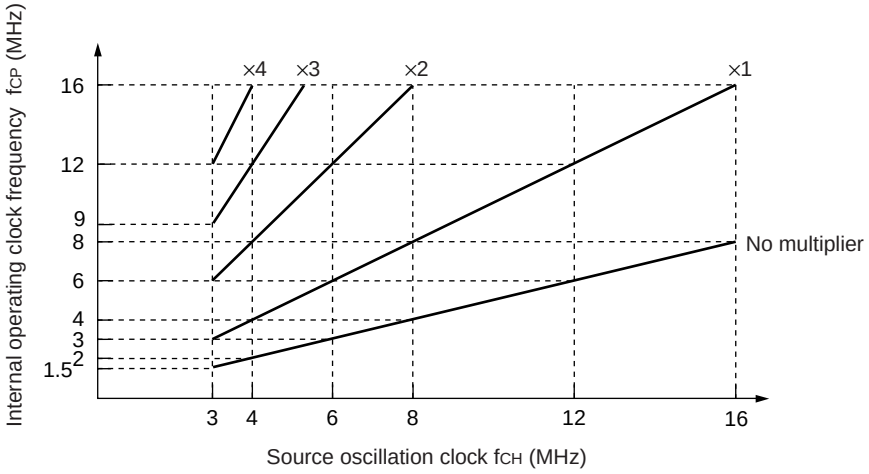
Notes: • V_{CC} in the standard signifies V_{DD}-FIP = V_{DD}-VFT = V_{CC}-CPU. Also, use the 3 pins on the left at the same power level. Here, V_{SS} signifies V_{SS}-IO = V_{SS}-CPU. Please connect this pin to GND as well.
• Current values are subject to change without notice, in order to affect improvements in characteristics, etc. The power current measurement condition is the external clock.

• **Scope of Guaranteed PLL Operation**

Relationship between Internal Operation Clock Frequency and Power Voltage



Relationship between Source Oscillation Clock Frequency and Internal Operating Clock Frequency



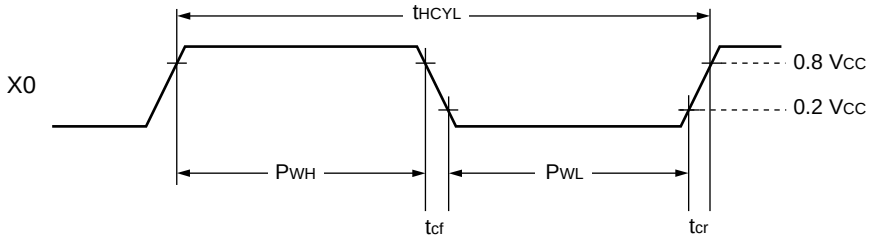
4. AC Characteristics

(1) Clock Timings

(Ta = −40 °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0, X1	—	3	—	16	MHz	
				3		16		× 1/2 (When PLL stops)
				3		16		PLL × 1
				3		8		PLL × 2
				3		5.33		PLL × 3
				3		4		PLL × 4
Clock cycle time	t_{HCYL}	X0, X1		62.5	—	333	ns	
Input clock pulse width	P_{WH} P_{WL}	X0		10	—	—	ns	Recommended duty ratio = 30% to 70%
Input clock rise/fall time	tcr tcf	X0		—	—	5	ns	When using an external clock
Internal operating clock frequency	f_{CP}	—		1.5	—	16	MHz	
Internal operating clock cycle time	t_{CP}	—		62.5	—	666	ns	

- **X0 and X1 clock timing**



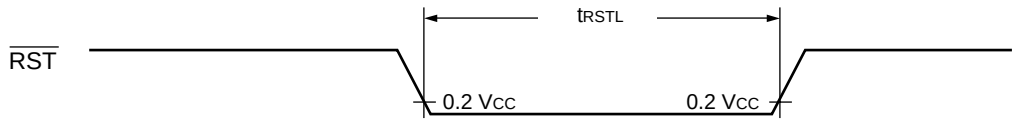
(2) Reset

(Ta = –40 °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

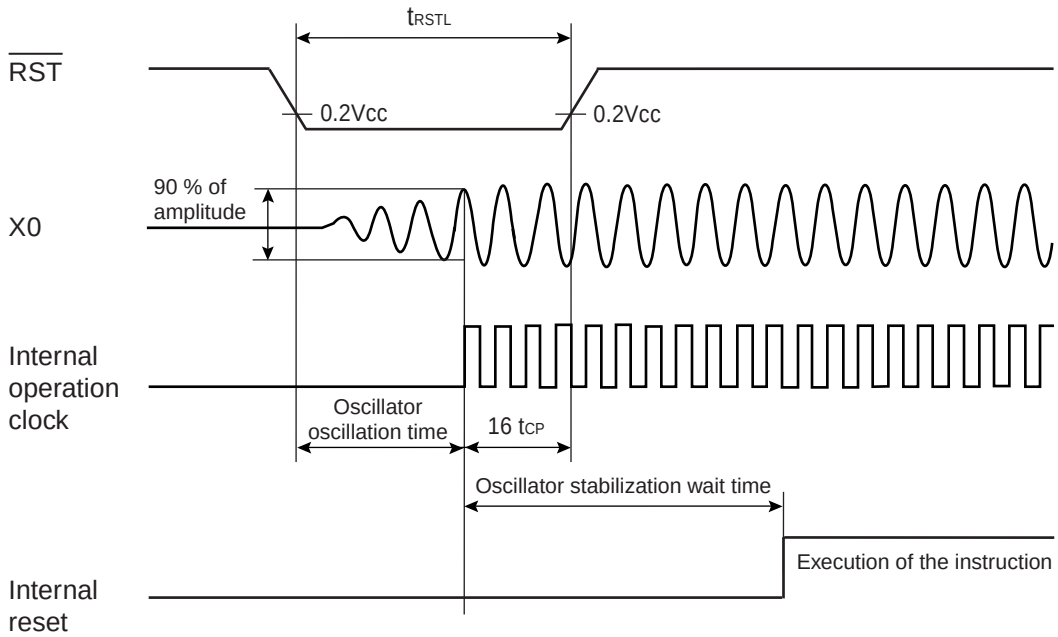
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}	—	ns	In normal operation
				Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode

*: Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several dozen ms; for a FAR/ceramic oscillator, this is several hundred μs to a few ms, and for an external clock this is 0 ms.

• In normal operation



• In stop mode



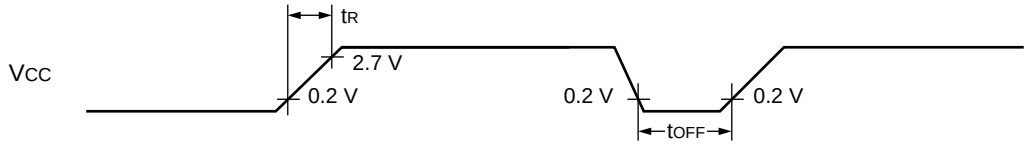
(3) Power-On Reset

(Ta = –40 °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

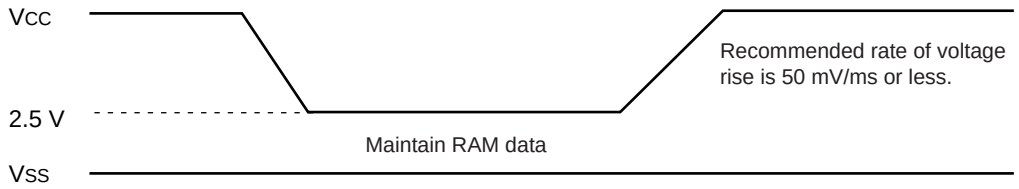
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}*	—	0.05	30	ms	
Power supply cutoff time	t_{OFF}	V_{CC}		4	—	ms	For repeated operation

* : V_{CC} must be less than 0.2 V before power-on.

Notes : • The above rating values are for generating a power-on reset.
• Some internal registers are only initialized by a power-on reset. Always apply the power supply in accordance with the above ratings if you wish to initialize these registers.



Sudden changes in the power supply voltage may cause a power-on reset.
The recommended practice if you wish to change the power supply voltage while the device is operating is to raise the voltage smoothly as shown below. Also, changes to the supply voltage should be performed when the PLL clock is not in use. The PLL clock may be used, however, if the rate of voltage change is 1 V/s or less.



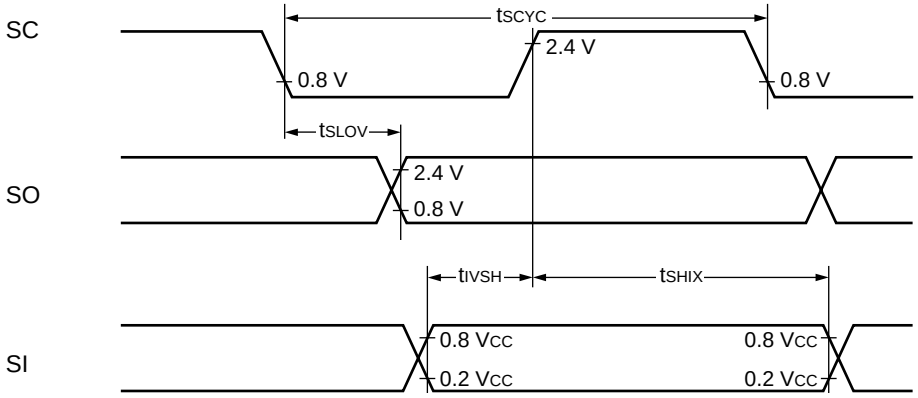
(4) Serial I/O

(Ta = –40 °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

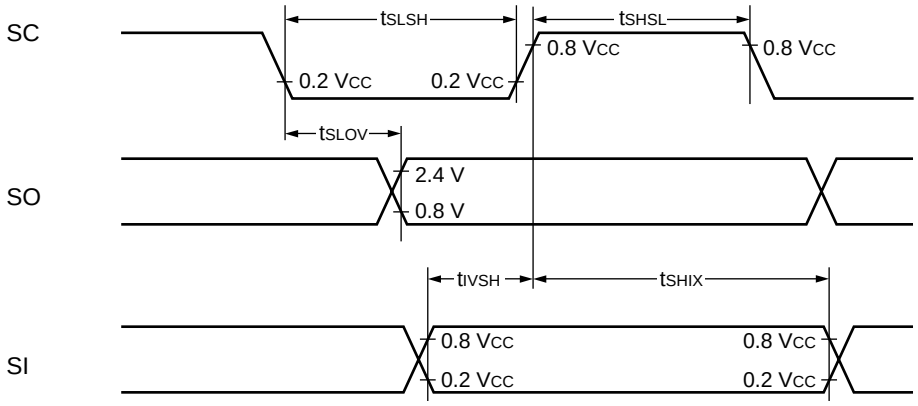
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SC0 to SC3	Internal shift clock mode, output pin load is C_L = 80 pF + 1 TTL	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SC0 to SC3 SO0 to SO3		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SC0 to SC3 SI0 to SI2		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SC0 to SC3 SI0 to SI2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SC0 to SC3	External shift clock mode, output pin load is C_L = 80 pF + 1 TTL	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SC0 to SC3		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SC0 to SC3 SO0 to SO3		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SC0 to SC3 SI0 to SI3		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SC0 to SC3 SI0 to SI2		60	—	ns	

Notes :
- Above rating is the case of CLK synchronous mode.
- C_L is the load capacitor connected to the pin for testing.
- t_{CP} is the machine cycle period (unit = ns)

- **Internal shift clock mode**



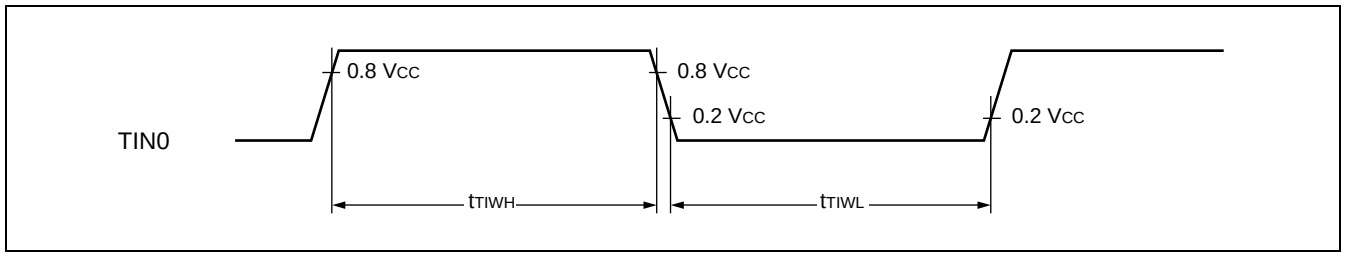
- **External shift clock mode**



(5) Timer Input Timings

(Ta = –40 °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

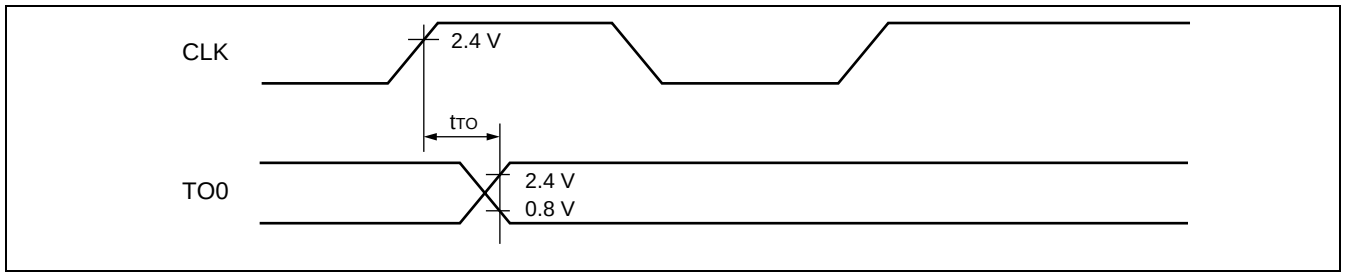
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0	—	4 t_{CP}	—	ns	



(6) Timer Output Timings

(Ta = –40 °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

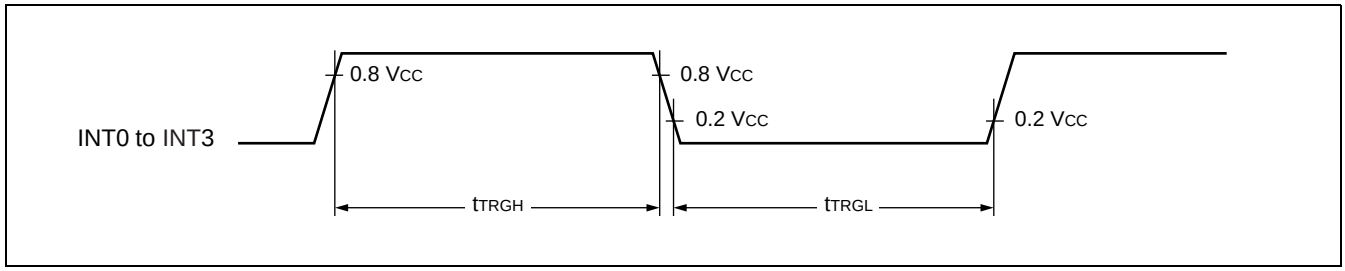
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
CLK ↑ → T_{OUT} change time	t_{TO}	TO0	—	30	—	ns	



(7) Trigger Input Timings

(Ta = –40 °C to +85 °C, V_{DD}-FIP = V_{CC}-CPU = AV_{CC} = 3.0 V to 3.6 V, V_{SS}-IO = V_{SS}-CPU = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGL}	INT0 to INT3	—	5 t_{CP}	—	ns	In normal operation
				1	—	µs	In stop mode



5. Electrical Characteristics of A/D Converter

(Ta = –40 °C to +85 °C, V_{CC}-CPU ≤ AV_{CC} = 3.0 V to 3.6 V, V_{SS}-CPU = V_{SS}-IO = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total Error	—	—	—	—	±3.0	LSB	
Non-linear Error	—	—	—	—	±2.5	LSB	
Differential Linear Error	—	—	—	—	±1.9	LSB	
Zero Transition Voltage	V_{OT}	AN0 to AN15	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	1 LSB = AV_{CC}/1024
Full-scale Transition Voltage	V_{FST}	AN0 to AN15	AV_{CC} – 3.5 LSB	AV_{CC} – 1.5 LSB	AV_{CC} + 0.5 LSB	mV	
Conversion Time (sampling + comparison)	—	—	98 t_{CP}*2	—	—	ns	16 MHz Operation
Sampling Time	—	—	32 t_{CP}*2	—	—	ns	16 MHz Operation
Comparison Time	—	—	66 t_{CP}*2	—	—	ns	16 MHz Operation
Analog Port Input Voltage	I_{AIN}	AN0 to AN15	—	—	10	µA	
Analog Input Voltage	V_{AIN}	AN0 to AN15	0	—	AV_{CC}	V	
Reference Voltage	—	AV_{CC}	3.0	—	AV_{CC}	V	
Power Current	I_A	AV_{CC}	—	1	5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*1
Reference Voltage Supply Current	I_R	AV_{CC}	—	100	200	µA	
	I_{RH}	AV_{CC}	—	—	5	µA	*1
Inter-channel Variance	—	AN0 to AN15	—	—	4	LSB	

*1 : When the A/D converter is not operating, voltage when CPU stopped (at $V_{CC\text{-}CPU}$ = AV_{CC} = 3.3 V)

*2 : t_{CP} signifies 1/internal operating frequency. With t_{CP} at internal 16 MHz, 1/16 MHz = 62.5 ns.

Notes:
- Reference “L” side set permanently to AV_{SS}, and reference “H” side set permanently to AV_{CC}. As AV_{CC} decreases, relative error increases.
- Please use the output impedance of the external analog input circuit under the following conditions : External circuit output impedance ≤ 10 kΩ
- An overly high external circuit output impedance could cause a lack of analog voltage sampling time.

- Analog Input Circuit Equivalent Circuit Diagram

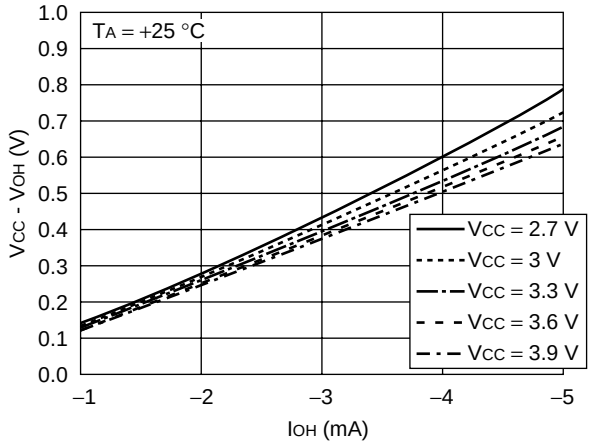
MB90M407/A,MB90M408/A
R_{ON} = approx. 1.5 kΩ
C = approx. 30 pF
MB90MF408/A, MB90MV405
R_{ON} = approx. 3.0 kΩ
C = approx. 65 pF

Note : Please use the figures given here as a rough guide.

■ SAMPLE CHARACTERISTICS

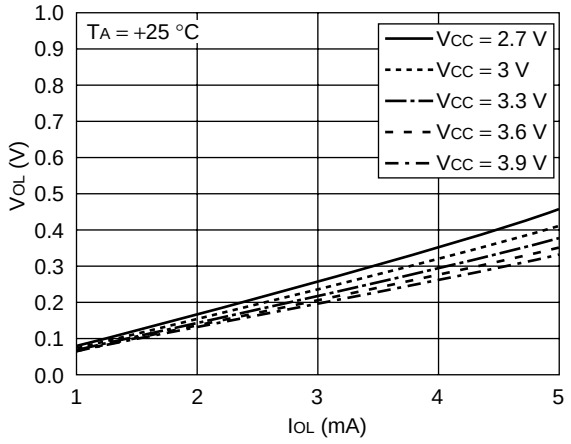
(1) “H” level output voltage

$(V_{CC} - V_{OH})$ – I_{OH}



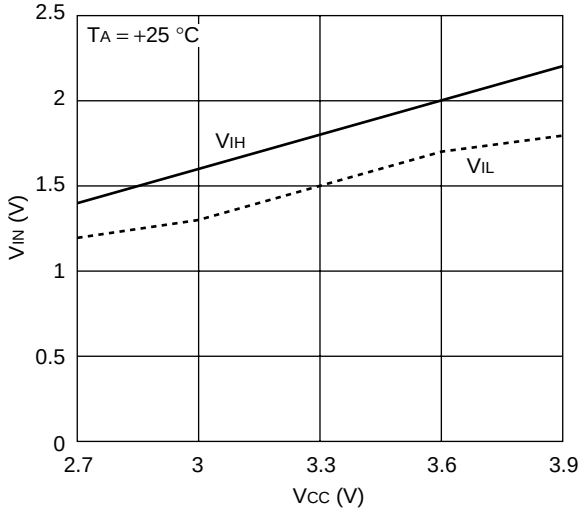
(2) “L” level output voltage

V_{OL} – I_{OL}



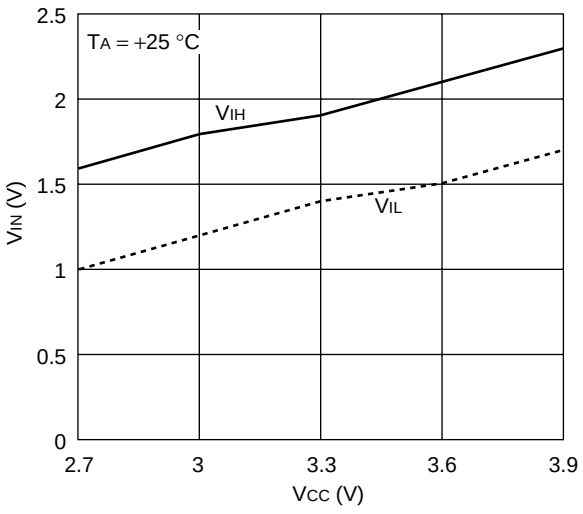
(3) “H” level input voltage/ “L” level input voltage (CMOS input)

V_{IN} – V_{CC}



(4) “H” level input voltage/ “L” level input voltage (hysteresis input)

V_{IN} – V_{CC}



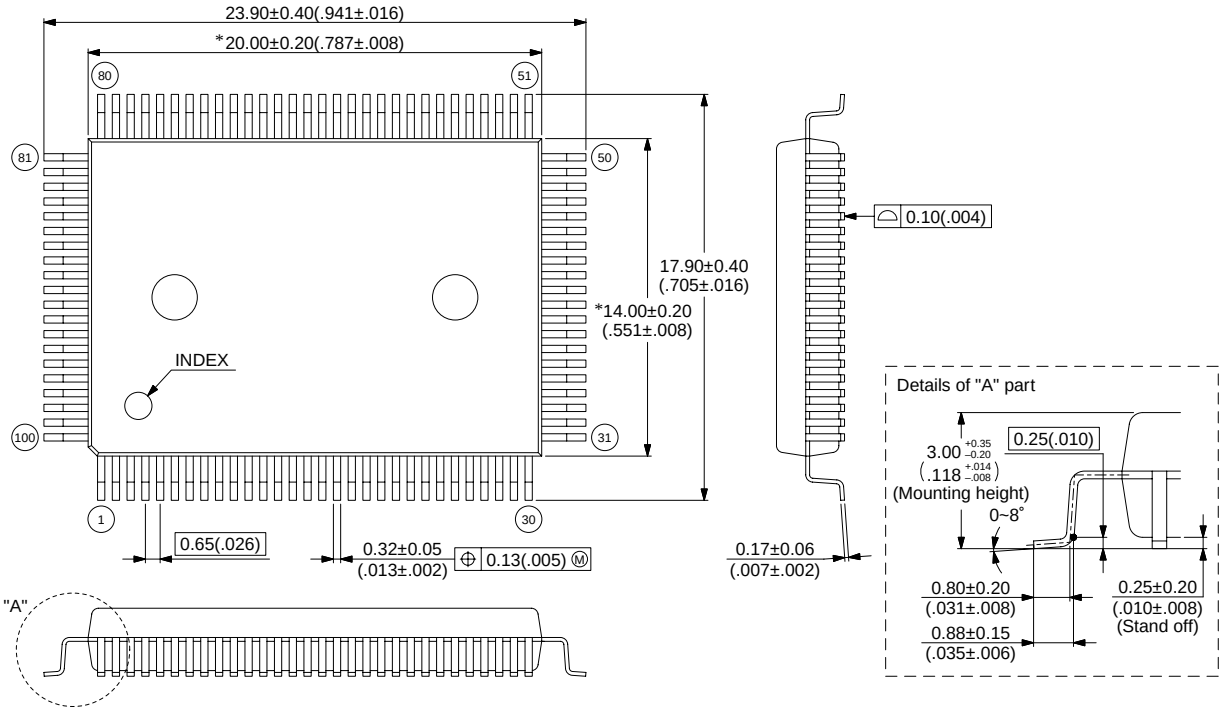
■ ORDERING INFORMATION

Part NO.	Package	Remarks
MB90MF408PF MB90M408PF MB90M407PF	100-pin plastic QFP (FPT-100P-M06)	All FL output pins (FIP0 to FIP59) have pull downs
MB90MF408APF MB90M408APF MB90M407APF		Some FL output pins (FIP0 to FIP16) do not have pull downs. The remaining FL output pins (FIP17 to FIP59) have pull downs.

■ PACKAGE DIMENSIONS

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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