16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90520A/520B Series

MB90522A/523A/522B/523B/F523B/V520A

DESCRIPTION

The MB90520A/520B series is a general-purpose 16-bit microcontroller designed for process control applications in consumer products that require high-speed real-time processing.

The microcontroller instruction set is based on the AT architecture of the F²MC^{*} family with additional instructions for high-level languages, extended addressing modes, enhanced multiplication and division instructions, and a complete range of bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word (32-bit) data.

The MB90520A/520B series peripheral resources include an 8/10-bit A/D converter, 8-bit D/A converter, UART (SCI), extended I/O serial interfaces 0 and 1, 8/16-bit up/down counter/timers 0 and 1, 8/16-bit PPG timers 0 and 1, a range of I/O timers (16-bit free-run timers 1 and 2, input capture (ICU) 0 and 1, and output compare (OCU) 0 and 1), an LCD controller/driver, 8 external interrupt inputs, and 8 wakeup interrupts.

* : F²MC stands for FUJITSU Flexible MicroController.

■ FEATURES

- Clock
- Internal PLL clock multiplication circuit
- Selectable machine clock (PLL clock) : Base oscillation divided by two or multiplied by one to four (For a 4 MHz base oscillation, the machine clock range is 4 MHz to 16 MHz).

PACKAGES





(Continued)
Sub-clock (32.768 KHz) operation available
Minimum instruction execution time : 62.5 ns (for oscillation = 4 MHz. PLL clock setting = \times 4. Vcc = 5.0 V)
• 16MB CPU memory space
Internal 24-bit addressing
Instruction set optimized for controller applications
Rich data types (bit, byte, word, long-word)
Extended addressing modes (23 types)
Enhanced signed multiplication and division instructions and RETI instruction
Enhanced calculation precision using a 32-bit accumulator
Instruction set designed for high-level language (C) and multi-tasking
System stack pointer
Enhanced pointer-indirect instructions and barrel shift instructions
Faster execution speed
4-byte instruction queue
ROM mirror function (48 Kbytes of bank FF is mirrored in bank 00)
• Program patch function : An address match detection function (2 \times addresses)
Interrupt function
32 programmable interrupts with 8 levels
Automatic data transmission function independent of CPU operation
Extended intelligent I/O service function (EI2OS) : Up to 16 channels
Low-power consumption (stand-by) modes
Sleep mode (CPU operating clock stops, peripherals continue to operate.)
Pseudo-clock mode (Only oscillation clock and timebase timer continue to operate.)
Clock mode (Main oscillation clock stops, sub-clock and clock timer continue to operate.)
Stop mode (Main oscillation and sub-clock both stop.)
CPU intermittent operation mode
Hardware stand-by mode (Change to stop mpde by operating hardware stand-by pins.)
Process
CMOS technology
• I/O ports
General-purpose I/O ports (CMOS input/output) : 53 ports
General-purpose I/O ports (inputs with pull-up resistors) : 24 ports
General-purpose I/O ports (Nch open-drain outputs) : 8 ports
• Timers
Timebase timer, clock timer, watchdog timer : 1 channel each
8/16-bit PPG timers 0 and 1 : 8-bit $ imes$ 2 channels or 16-bit $ imes$ 1 channel
16-bit reload timers 0 and 1 : 2 channels
16-bit I/O timers :
16-bit free-run timers 0 and 1 : 2 channels
16-bit input capture 0 : 2 channels (2 channels per unit)
16-bit output compare 0 and 1 : 8 channels (4 channels per unit)
8/16-bit up/down counter/timers 0 and 1 : 8-bit $ imes$ 2 channels or 16-bit $ imes$ 1 channel
Clock output function : 1 channel
 Communications macro (communication interface)
Extended I/O serial interfaces 0 and 1 : 2 channels
UART (full-duplex, double-buffered, SCI : Can also be used for synchronous serial transfer) : 1 channel

• External event interrupt control function

DTP/external interrupts : 8 channels (Can be set to detect rising edges, falling edges, "H" levels, or "L" levels) Wake-up interrupts : 8 channels (Detects "L" levels only)

Delayed interrupt generation module : 1 channel (for task switching)

Analog/digital conversion
 8/10-bit A/D converter : 8 channels (Can be initiated by an external trigger. Minimum conversion time = 10.2 μs for a 16 MHz machine clock)

 8-bit D/A converter : 2 channels (R-2R type. Settling time = 12.5 μs for a 16 MHz machine clock)

Display function

LCD controller/driver : 32 \times segment drivers + 4 \times common drivers

www.DataSheet4U.eo**Other**

Supports serial writing to flash memory. (Only on versions with on-board flash memory.)

Note : The MB90520A and 520B series cannot be used in external bus mode. Always set these devices to singlechip mode.

■ PRODUCT LINEUP

Parameter	Part Number	MB90522A	MB90523A	MB90522B	MB90523B	MB90F523B	MB90V520A		
Classificatio	on		Mask	Flash ROM	Evaluation product				
ROM size		64 Kbytes	128 Kbytes	128 Kbytes					
RAM size				•	6 Kbytes				
Separate er power supp	mulator ly⁺¹	_	_	_	_	_	No		
Process				CN	IOS				
Operating p supply volta	oower age ^{*2}	3.0 V t	o 5.5 V	2.7 V t	o 5.5 V	3.0 V to 5.5 V			
Internal reg	ulator circuit		not mo	ounted		mou	nted		
CPU functio	ons	Number of ins Instruction siz Instruction ler Data sizes : 1	Number of instructions : 340 Instruction sizes : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data sizes : 1-bit, 8-bit, 16-bit						
		Minimum instruction execution time : 62.5 ns (for a 16 MHz machine clock)							
		Interrupt processing time : 1.5 μ s min. (for a 16 MHz machine clock)							
Low power (standby m	operation lodes)	Sleep mode, clock mode, pseudo-clock mode, stop mode, hardware standby mode, and CPU intermittent operation mode							
I/O ports		General-purpose I/O ports (CMOS outputs) : 53 General-purpose I/O ports (inputs with pull-up resistors) : 24 General-purpose I/O ports (Nch open drain outputs) : 8 Total : 85							
Timebase ti	mer	18-bit counter Interrupt interval : 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (for a 4 MHz base oscillation)							
Watchdog t	imer	Reset trigger period • For a 4 MHz base oscillation : 3.58, 14.33, 57.23, 458.75 ms • For 32.768 sub-clock operation : 0.438, 3.500, 7.000, 14.000 s							
	16-bit freerun timer	Number of ch Generates an	annels : 2 interrupt on ov	verflow					
16-bit I/O timers	16-bit output compare	Number of ch Pin change tir	annels : 8 ning : Free run	timer register	value equals o	utput compare	register value.		
16-bit input capture		Number of channels : 2 Saves the value of the freerun timer register when a pin input occurs (rising edge, falling edge, either edge) .							
16-bit reloa	d timer	Number of channels : 2 Count clock frequency : 0.125, 0.5, or 2.0 μ s for a 16 MHz machine clock Can be used to count an external event clock.							

(Continued)

Part Number Parameter	MB90522A	MB90523A	MB90522B	MB90523B	MB90F523B	MB90V520A
Clock timer	15-bit timer Interrupt interv	/al : 0.438, 0.5	, or 2.0 μs for s	ub-clock frequ	ency = 32.768	kHz
8/16-bit PPG timer	Number of cha Can generate	annels : 1 (Car a pulse wavef	t be used in 2 × porm output with	8-bit channel specified perio	mode) od and 0 to 100	0% duty ratio.
8/16 -bit up/down counter/timers	Number of cha External even Reload/compa	annels : 1 (Car t inputs : 6 cha are function : 8	i be used in 2 × nnels ·bit × 2 channe	8-bit channel	mode)	
Clock monitor	Clock output f	requency : Ma	chine clock/21 t	o machine cloo	:k/2 ⁸	
Delayed interrupt generation module	Interrupt gene	ration module	for task switchi	ng. (Used by I	REALOS.)	
DTP/External interrupts	Input channels : 8 Generates interrupts to the CPU on rising edges, falling edges with input "H" level, or "L" level. Can be used for external event interrupts and to activate El ² OS.					
Wakeup interrupts	Input channels Triggered by "	s : 8 L" level.				
8/10-bit A/D converter (successive approximation type)	Number of channels : 8 Resolution : 8-bit or 10-bit selectable Conversion can be performed sequentially for multiple consecutive channels. • Single-shot conversion mode : Converts specified channel once only. • Continuous conversion mode : Repeatedly converts specified channel. • Intermittent conversion mode : Converts specified channel then balts temporarily.					
8-bit D/A converter (R-2R type)	Number of cha Resolution : 8	annels : 2 -bit				
UART (SCI)	Number of channels : 1 Clock synchronous transfer : 62.5 Kbps to 1 Mbps Clock asynchronous transfer : 1202 bps to 31250 bps Supports bi-directional and master-slave communications.					
Extended I/O serial interface	Number of channels : 2 Clock synchronous transfer : 31.25 Kbps to 1 Mbps (Using internal shift clock) Transmission format : Selectable LSB-first or MSB-first					
LCD controller/driver	Number of common outputs : 4 Number of segment outputs : 32 Number of power supply pins for LCD drive : 4 LCD display memory : 16 bytes Divider resistor for LCD drive : Internal					

*1 : As for the necessity of a DIP switch setting (S2) when using the emulation pod (MB2145-507) . Refer to the hardware manual for the emulation pod (MB2145-507) fomr details.

*2 : Take note of the maximum operating frequency and A/D converter precision restrictions when operating at 3.0 V to 3.6 V. See the "Electrical Characteristics" section for details.

■ PACKAGES AND CORRESPONDING PRODUCTS

Package	MB90522A	MB90523A	MB90522B	MB90523B	MB90F523B	MB90V520A
FPT-120P-M05 (LQFP)	0	0	0	0	0	×
FPT-120P-M13 (QFP)	0	0	0	0	0	×
PGA-256C-A01 (PGA)	×	×	×	×	×	0

www.DataSheet4U.cQn : Available, × : Not available

Note : See the "■ PACKAGE DIMENSIONS" section for more details.

■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

	Pin No.		Circuit			
	LQFP-120 ^{*1} QFP-120 ^{*2}	Pin Name	Туре	Function		
	92, 93	X0, X1	А	Oscillator pin		
	74, 73	X0A, X1A	В	Sub-oscillator pin		
	89 to 87	MD0 to MD2	С	Input pins for setting the operation mode. Connect directly to V_{CC} or V_{SS} .		
iee	4U.com 90	RST	С	External reset input pin		
	86	HST	С	Hardware standby input pin		
95 to 101	P00 to P06	D	General-purpose I/O ports The settings in the pull-up resistor setup register (RDR0) are enabled when ports are set as inputs. The RDR0 settings are ignored when ports are set as outputs.			
	INT0 to INT6		Event input pins for ch.0 to ch.6 of the DTP/external interrupt circuit			
	102 P07		D	General-purpose I/O port The settings in the pull-up resistor setup register (RDR0) are enabled when ports are set as inputs. The RDR0 settings are ignored when ports are set as outputs.		
103 to ⁻	103 to 110	P10 to P17	P10 to P17	P10 to P17	D	General-purpose I/O ports The settings in the pull-up resistor setup register (RDR1) are enabled when ports are set as inputs. The RDR1 settings are ignored when ports are set as outputs.
		WI0 to WI7		Event input pins for the wakeup interrupts.		
		P20, P21, P22, P23		General-purpose I/O ports		
	111, 112, 113, 114	IC00, IC01, IC10, IC11	Е	Trigger input pins for input capture units (ICU) 0 and 1. Input operates continuously when channels 0 and 1 of input capture units (ICU) 0 and 1 are operating. Accordingly, output to the pins from other func- tions that share this pin must be suspended unless performed intentionally.		
		P24		General-purpose I/O port		
	115	AINO	E	Also can be used as the count clock A input to 8/16-bit up/down counter/ timer 0.		
		P25		General-purpose I/O port		
	116	BIN0	E	Also can be used as the count clock B input to 8/16-bit up/down counter/ timer 0.		
		P26		General-purpose I/O port		
	117	ZINO	Е	Also can be used as the control clock Z input to 8/16-bit up/down counter/ timer 0.		
		INT7		Event input pin for ch.7 of the DTP/external interrupt circuit		

*1 : FPT-120P-M05

*2 : FPT-120P-M13

	Pin No.		0:			
	LQFP-120 ^{*1} QFP-120 ^{*2}	Pin Name	Туре	Function		
		P27		General-purpose I/O port		
	118	ADTG	E	External trigger input to the 8/10-bit A/D converter Input operates continuously when the 8/10-bit A/D converter is performing input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally.		
DataShee	4U.com 120	P30	E	General-purpose I/O port		
		P31		General-purpose I/O port		
	1	СКОТ	E	Output pin for clock monitor function The clock monitor is output when clock monitor output is enabled.		
	2	P32	F	General-purpose I/O port Only available when waveform output from output compare 0 is disabled.		
-	2	OUT0	L	Event output pin for ch.0 of output compare unit 0 (OCU) Only available when event output is enabled for output compare unit 0.		
	3	P33	Г	General-purpose I/O port Only available when waveform output from output compare 1 is disabled.		
		OUT1	E	Event output pin for ch.1 of output compare unit 0 (OCU) Only available when event output is enabled for output compare unit 0.		
	4	P34	F	General-purpose I/O port Only available when waveform output from output compare 2 is disabled.		
	+	OUT2	L	Event output pin for ch.2 of output compare unit 0 (OCU) Only available when event output is enabled for output compare unit 0.		
	5	P35	E	General-purpose I/O port Only available when waveform output from output compare 3 is disabled.		
	5	OUT3	L	Event output pin for ch.3 of output compare unit 0 (OCU) Only available when event output is enabled for output compare unit 0.		
	6	P36	F	General-purpose I/O port Only available when waveform output from PG00 is disabled.		
	0	PG00	L	Output pin for 8/16-bit PPG timer 0 Only available when waveform output is enabled for PG00.		
	7	P37	F	General-purpose I/O port Only available when waveform output from PG01 is disabled.		
	/	PG01	E	Output pin for 8/16-bit PPG timer 0 Only available when waveform output is enabled for PG01.		

*1 : FPT-120P-M05

*2 : FPT-120P-M13

	Pin No.		Oirrowit	Function		
	LQFP-120 ^{*1} QFP-120 ^{*2}	Pin Name	Туре			
	9, 10	P40, P41	D	General-purpose I/O ports Only available when waveform outputs from PG10 and PG11 are disabled. The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs.		
w.DataShee	4U.com	PG10, PG11		Output pins for 8/16-bit PPG timer 1 Only available when waveform output is enabled for PG10 and PG11.		
	11	P42	D	General-purpose I/O port The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs.		
		SINO		UART (SCI) serial data input pin Input operates continuously when the UART is performing input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally.		
	12	P43	3 D	General-purpose I/O port The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs.		
		SOT0		UART (SCI) serial data output pin Only available when serial data output is enabled for the UART (SCI) .		
	13	P44	D	General-purpose I/O port The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs.		
		SCK0		UART (SCI) serial clock input/output pin Only available when serial clock output is enabled for the UART (SCI) .		
	14	P45	D	General-purpose I/O port The settings in the pull-up resistor setup register (RDR4) are enabled when ports set as inputs. The RDR4 settings are ignored when ports set are as outputs.		
-	14	SIN1	U	Data input pin for extended I/O serial interface 1 Input operates continuously when the performing serial input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally.		
	15	P46	D	General-purpose I/O port The settings in the pull-up resistor setup register (RDR4) are enabled when ports set as inputs. The RDR4 settings are ignored when ports are set as outputs.		
		SOT1		Data output pin for extended I/O serial interface 1 Only available when serial data output is enabled for SOT1.		

*1 : FPT-120P-M05

*2 : FPT-120P-M13

	Pin No.		Oires it	
	LQFP-120 ^{*1} QFP-120 ^{*2}	Pin Name	Туре	Function
	16	P47	D	General-purpose I/O port The settings in the pull-up resistor setup register (RDR4) are enabled when ports are set as inputs. The RDR4 settings are ignored when ports are set as outputs.
ataShee	4U.com	SCK1		Serial clock input/output pin for extended I/O serial interface 1 Only available when serial clock output is enabled for SCK1.
		P50		General-purpose I/O port
	35	SIN2	E	Data input pin for extended I/O serial interface 2 Input operates continuously when the performing serial input. Accordingly, output to the pin from other functions that share this pin must be suspended unless performed intentionally.
		AIN1		Also can be used as the count clock A input to 8/16-bit up/down counter/ timer 1.
		P51		General-purpose I/O port
	36	SOT2	E	Data output pin for extended I/O serial interface 2 Only available when serial data output is enabled for SOT2.
		BIN1		Also can be used as the count clock B input to 8/16-bit up/down counter/ timer 1.
		P52		General-purpose I/O port
	37	SCK2	Е	Serial clock input/output pin for extended I/O serial interface 2 Only available when serial clock output is enabled for SCK2.
		ZIN1		Also can be used as the control clock Z input to 8/16-bit up/down counter/ timer 1.
	40.41	P53, P54	I	General-purpose I/O ports
	+0, 41	DA0, DA1	1	Analog output pins for ch.0 and ch.1 of the 8-bit D/A converter
	46 to 53	P60 to P67	ĸ	General-purpose I/O ports Port input is enabled when the analog input enable register (ADER) is set to the ports.
	40 10 55	AN0 to AN7	ĸ	Analog inputs for the 8/10-bit A/D converter Analog input is enabled when the analog input enable register (ADER) is set.
		P70, P72		General-purpose I/O ports
	55, 57	TI0, TI1	E	Event input pins for 16-bit reload timers 0 and 1 Input operates continuously when 16-bit reload timers 0 and 1 input an external clock. Accordingly, output to these pins from other functions that share the pins must be suspended unless performed intentionally.
		OUT4, OUT6	-	Event output pins for ch. 4 and ch. 6 of output compare unit 1 (OCU) Only available when event output from output compare 1 is enabled.

*1 : FPT-120P-M05

*2 : FPT-120P-M13

Pin No.			0			
	LQFP-120 ^{*1} QFP-120 ^{*2}	Pin Name	Type	Function		
		P71, P73		General-purpose I/O ports Only available when event outputs from 16-bit reload timers 0 and 1 are disabled.		
	56, 58	TO0, TO1	E	Output pins for 16-bit reload timers 0 and 1. Only available when output is enabled for 16-bit reload timers 0 and 1.		
DataShee	4U.com	OUT5, OUT7		Event output pins for ch. 5 and ch. 7 of output compare unit 1 (OCU) Only available when event output from output compare 1 is enabled.		
	50 to 62	P74 to P77		General-purpose I/O ports Only available when the LCD controller/driver control register is set to the ports.		
	39 10 02	COM0 to COM3	L	Common pins for the LCD controller/driver Only available when the LCD controller/driver control register is set to the common outputs.		
	64 to 71	P80 to P87	L	General-purpose I/O ports Only available when the LCD controller/driver control register is set to the ports.		
		SEG16 to SEG23		LCD segment output pins for the LCD controller/driver Only available when the LCD controller/driver control register is set to the segment outputs.		
	72,	P90, P91 to P97	- M -	General-purpose I/O ports (Support up to $I_{OL} = 10 \text{ mA}$) Only available when the LCD controller/driver control register is set to the ports.		
	75 to 81	SEG24, SEG25 to SEG31		LCD segment output pins for the LCD controller/driver Only available when the LCD controller/driver control register is set to the segment outputs.		
	17 to 24	SEG0 to SEG7	F	LCD segment 00 to 07 pins for the LCD controller/driver		
	25 to 32	PA0 to PA7	I	General-purpose I/O ports Only available when the LCD controller/driver control register is set up to the ports.		
	25 to 32	SEG8 to SEG15	EG8 to EG15	LCD segment 08 to 15 pins for the LCD controller/driver Only available when the LCD controller/driver control register is set to the segment outputs.		

*1 : FPT-120P-M05

*2 : FPT-120P-M13

(Continued)

Pin No.		Circovit			
LQFP-120 ^{*1} QFP-120 ^{*2}	Pin Name	Туре	Function		
34	С	G	Capacitor connection pin for stabilizing power supply Connect an external ceramic capacitor of approximately 0.1 μ F. If operating at 3.3 V or lower, connect to V _{CC} .		
82 to 85	V0 to V3	N	Power supply input pins for the LCD controller/driver		
ei4U∴8,∩54, 94	Vcc	Power supply	Power supply input pins for the digital circuit		
33, 63, 91, 119	9 Vss	Power supply	GND level power supply input pins for the digital circuit		
42	AVcc	н	Power supply input for the analog circuit Ensure that a voltage greater than AV $_{\rm CC}$ is applied to V $_{\rm CC}$ before turning the analog power supply on or off.		
43	AVRH	J	"H" reference voltage for the A/D converter Ensure that a voltage greater than AVRH is applied to AV $_{\rm CC}$ before turning the power supply to this pin on or off.		
44	AVRL	Н	"L" reference voltage for the A/D converter		
45	AVss	Н	GND level power supply input pin for the analog circuit		
38	DVcc	н	"H" reference voltage for the D/A converter Ensure that this voltage does not exceed Vcc.		
39	DVss	н	"L" reference voltage for the D/A converter Apply the same voltage level as Vss.		

*1 : FPT-120P-M05

*2 : FPT-120P-M13

■ I/O CIRCUIT TYPE









■ HANDLING DEVICES

Take note of the following points when handling devices :

- Do not exceed maximum rated voltage (to prevent latch-up)
- Supply voltage stability
- · Power-on precautions
- Power supply pins
- Crystal oscillator circuit
- Notes on using an external clock
- · Precautions when not using sub-clock mode
- Treatment of unused pins
- ww.DataSheet4U.eoTreatment of N.C. pins
 - Treatment of pins when A/D converter is not used
 - Sequence for connecting and disconnecting the A/D converter power supply and analog input pins
 - · Shared use of general-purpose I/O ports and LCD controller/driver SEG/COM pins
 - · Conditions when output from ports 0 and 1 is undefined
 - Initialization
 - Notes on using the DIV A, Ri and DIVW A, RWi instructions
 - Notes on using REALOS

Device Handling Precautions

• Do not exceed maximum rated voltage (to prevent latch-up)

Latch-up occurs in CMOS ICs if a voltage greater than Vcc or less than Vss is applied to an input or output pin (other than a high or medium withstand voltage pin) or if the voltage applied between Vcc and Vss exceeds the rating. If latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.

Similarly, when turning the analog power supply on or off, ensure the analog power supply voltages (AVcc, AVRH, DVcc) and analog input voltages do not exceed the digital voltage (Vcc).

Also ensure that the voltages applied to the LCD power supply pins (V3 to V0) do not exceed the power supply voltage (V_{CC}).

Supply voltage stability

Rapid changes in supply voltage may cause the device to misoperate, even if the voltage remains within the allowed operating range. Accordingly, ensure that the Vcc supply is stable.

The standard for power supply voltage stability is a peak-to-peak V_{CC} ripple voltage at the mains supply frequency (50 to 60 Hz) of 10% or less of V_{CC} and a transient voltage change rate of 0.1 V/ms or less when turning the power supply on or off.

Power-on precautions

To prevent misoperation of the internal regulator circuit at power-on, ensure that the power supply rising time (0.2 V to 2.7 V) is at least 50 μ s.

• Power supply pins

When multiple V_{cc} and V_{ss} pins are provided, connect all V_{cc} and V_{ss} pins to power supply or ground externally. Although pins at the same potential are connected together in the internal device design so as to prevent misoperation such as latch-up, connecting all V_{cc} and V_{ss} pins appropriately minimizes unwanted radiation, prevents misoperation of strobe signals due to increases in the ground level, and keeps the overall output current rating.

Also, ensure that the impedance of the Vcc and Vss connections to the power supply are as low as possible.

Connection of a bypass capacitor of approximately 0.1 μ F between V_{cc} and V_{ss} is recommended to prevent power supply noise. Connect the capacitor close to the V_{cc} and V_{ss} pins.

Crystal oscillator circuit

Noise on the X0 and X1 pins can be a cause of device misoperation. Place the X0 and X1 pins, crystal oscillator (or ceramic oscillator), and bypass capacitor to ground as close together as possible. Also, design the circuit board so that the X0 and X1 pin wiring does not cross other wiring.

Surrounding the X0/X1 and X0A/X1A pins with ground in the printed circuit board design is recommended to ensure stable operation.

www.DataSheet4U. CoNotes on using an external clock

When using an external clock, drive the X0 pin only and leave the X1 pin open. The figure below shows an example of how to use an external clock.



· Precautions when not using sub-clock mode

Connect an oscillator to X0A and X1A, even if not using sub-clock mode.

• Treatment of unused pins

Leaving unused input pins unconnected can cause misoperation or permanent damage to the device due to latchup. Always pull-up or pull-down unused pins using a 2 k Ω or larger resistor.

If some I/O pins are unused, either set as outputs and leave open circuit or set as inputs and treat in the same way as input pins.

• Treatment of N.C. pins

Always leave N.C. (non connect) pins open circuit.

• Treatment of pins when A/D converter not used

When not using the A/D converter and D/A converter, always connect $AV_{CC} = DV_{CC} = AVRH = V_{CC}$ and $AV_{SS} = AVRL = V_{SS}$.

• Sequence for connecting and disconnecting the A/D converter power supply and analog input pins

Do not apply voltage to the A/D and D/A converter power supply (AVcc, AVRH, AVRL, DVcc, DVss) or analog inputs (AN0 to AN7) until the digital power supply (Vcc) is turned on.

When turning the device off, turn off the digital power supply after disconnecting the A/D converter power supply and analog inputs. When turning the power on or off, ensure that AVRH and DVcc do not exceed AVcc (turning the analog and digital power supplies on and off simultaneously is OK).

Shared use of general-purpose I/O ports and LCD controller/driver SEG/COM pins

The SEG08 to SEG31 and COM0 to COM3 pins are shared with general-purpose I/O ports. The electrical ratings for SEG08 to SEG23 and COM0 to COM3 are the same as for CMOS outputs and the electrical ratings for SEG24 to SEG31 are the same as for N-ch open-drain ports.

• Conditions when output from ports 0 and 1 is undefined

After turning on the power supply, the outputs from ports 0 and 1 are undefined during the oscillation stabilization delay time controlled by the regulator circuit (during the power-on reset). The figure below shows the timing.

Note that this undefined output period does not occur on products without an internal regulator circuit as these products do not have an oscillation stabilization delay time.



Note : See the "■ PRODUCT LINEUP" section for details of which MB90520A/520B series products have an internal regulator circuit.

Initialization

The device contains internal registers that are only initialized by a power-on reset. To initialize these registers, restart the power supply.

• Notes on using the DIV A, Ri and DIVW A, RWi instructions

Set the corresponding bank registers (DTB, ADB, USB, SSB) to "00H" when using the signed division instructions "DIV A, Ri" and "DIVW A, RWi".

If the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than "00_H", the remainder value produced by the instruction is not stored in the instruction operand register.

Notes on using REALOS

The extended intelligent I/O service (El²OS) cannot be used when using REALOS.

Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

• BLOCK DIAGRAM



- *2 : Incorporates a pull-up register setting register. CMOS level input and output.
- *3 : As this port shares pins with the LCD output, the port uses N-ch open-drain circuits.



Note : The upper part of 00 bank contains a mirror of the ROM data in FF bank. This is called the mirror ROM function and enables use of the C compiler's small memory model. As the lower 16 bits of the FF bank and 00 bank addresses are the same, tables located in ROM can be referenced without needing to declare far pointers.

For example, accessing $00C000_{H}$ actually accesses the contents of ROM at FFC000_H. Note that, as the FF bank ROM area exceeds 48 KBytes, the entire ROM image cannot be mirrored in 00 bank. Accordingly, as ROM data from FF4000_H to FFFFFF_H is mirrored in 004000_{H} to $00FFFF_{H}$, always locate ROM data tables in the range FF4000_H to FFFFFF_H.

■ I/O MAP

Address	Abbreviated Register Name	Register Name	Peripheral Name	Initial Value				
00000н	PDR0	Port 0 data register	Port 0	XXXXXXXXB				
000001н	PDR1	Port 1 data register	Port 1	XXXXXXXXB				
000002н	PDR2	Port 2 data register	Port 2	XXXXXXXXB				
000003н	PDR3	Port 3 data register	Port 3	XXXXXXXXB				
4 000004н	PDR4	Port 4 data register	Port 4	XXXXXXXXB				
000005н	PDR5	Port 5 data register	Port 5	XXXXXXXXB				
000006н	PDR6	Port 6 data register	Port 6	XXXXXXXXB				
000007н	PDR7	Port 7 data register	Port 7	XXXXXXXXB				
000008н	PDR8	Port 8 data register	Port 8	XXXXXXXXB				
000009н	PDR9	Port 9 data register	Port 9	XXXXXXXXB				
00000Ан	PDRA	Port A data register	Port A	XXXXXXXXB				
00000Bн	LCDCMR	Port 7/COM pin selection register	Port 7, LCD controller/driver	XXXX 0 0 0 0 _B				
00000Сн	0084	OCLL compare register ch 4	16 bit 1/O timor	XXXXXXXXB				
00000Dн	0064	CCC compare register cn.4		XXXXXXXXB				
00000EH		(Access prohibited)						
00000Fн	EIFR	Wakeup interrupt flag register	Wakeup interrupts	XXXXXXX0 _B				
000010н	DDR0	Port 0 direction register	Port 0	00000000 _B				
000011н	DDR1	Port 1 direction register	Port 1	00000000 _B				
000012н	DDR2	Port 2 direction register	Port 2	00000000 _B				
000013н	DDR3	Port 3 direction register	Port 3	00000000 _B				
000014н	DDR4	Port 4 direction register	Port 4	00000000 _B				
000015н	DDR5	Port 5 direction register	Port 5	XXX 0 0 0 0 0 _B				
000016н	DDR6	Port 6 direction register	Port 6	00000000 _B				
000017н	DDR7	Port 7 direction register	Port 7	00000000 _B				
000018H	DDR8	Port 8 direction register	Port 8	00000000 _B				
000019н	DDR9	Port 9 direction register	Port 9	00000000 _B				
00001Ан	DDRA	Port A direction register	Port A	00000000 _B				
00001Вн	ADER	Analog input enable register	Port 6, A/D converter	11111111 _B				
00001CH	OCP5	OCU compare register ch 5	16-bit I/O timer	XXXXXXXXB				
00001DH				XXXXXXXXB				
00001EH		(Access prohibi	ted)					
00001Fн	EICR	Wakeup interrupt enable register	Wakeup interrupts	00000000B				

Address	Abbreviated Register Name	Register Name	Peripheral Name	Initial Value
000020н	SMR	Serial mode register		00000000
000021н	SCR	Serial control register		00000100в
000022н	SIDR/ SODR	Serial input data register/ Serial output data register	(SCI)	XXXXXXXX
000023н	SSR	Serial status register		00001X00 _B
⁴ 000024н	SMC S1	Sorial mode control status register 1		XXXX0000 _B
000025н	310031	Senal mode control status register 1	Extended I/O serial interface 1	0000010в
000026н	SDR1	Serial data register 1		XXXXXXXXB
000027н	CDCR	Communication prescaler control register	Communication prescaler register	0 XXX 1 1 1 1 _B
000028н	SMCSO	Sorial mode control status register 2	-	XXXX0000 _B
000029н	3101032	Senar mode control status register 2	Extended I/O serial interface 2	0000010в
00002Ан	SDR2	Serial data register 2		XXXXXXXXB
00002Вн		(Access prohib	ited)	
00002Сн	00945	OCLI control status register ch 45		0000XX00 _B
00002Dн	00040		16-bit I/O timor	XXX 0 0 0 0 0 _B
00002Ен	00967	OCS67 OCU control status register ch 67		0000XX00 _B
00002Fн	00307			XXX 0 0 0 0 0 _B
000030н	ENIR	DTP/interrupt enable register		00000000 _B
000031н	EIRR	DTP/interrupt request register	DTP /external interrupt	XXXXXXXXB
000032н	EI VB	Request level setting register	circuit	00000000
000033н				00000000
000034н	OCP6	OCI I compare register ch 6	16-bit I/O timer	XXXXXXXXB
000035н		COO compare register cit.o		XXXXXXXXB
000036н	ADCS	A/D control status register		00000000 _B
000037н	Aboo		8/10-bit A/D converter	00000000
000038н	ADCB	A/D data register	of to bit A/D converter	XXXXXXXXB
000039н	Abon			$00001XXX_B$
00003Ан	DADR0	D/A converter data register ch.0		XXXXXXXXB
00003Вн	DADR1	D/A converter data register ch.1	8-hit D/A converter	XXXXXXXXB
00003Сн	DACR0	D/A control register 0		XXXXXXX 0B
00003Dн	DACR1	D/A control register 1		XXXXXXX 0B
00003Ен	CLKR	Clock output enable register	Clock monitor function	ХХХХ 0 0 0 0в
				(Continued)

Address	Abbreviated Register Name	Register Name	Peripheral Name	Initial Value		
00003Fн	(Access prohibited)					
000040н	PRLL0	PPG0 reload register L		XXXXXXXXB		
000041н	PRLH0	PPG0 reload register H	PG0 reload register H			
000042н	PRLL1	PPG1 reload register L		XXXXXXXXB		
000043н	PRLH1	PPG1 reload register H	8/16-bit PPG timer 0, 1	XXXXXXXXB		
000044н	PPGC0	PPG0 operation mode control register		0X000XX1 _B		
000045н	PPGC1	PPG1 operation mode control register		0X00001B		
000046н	PPGOE	PPG0, 1 output control register		00000000		
000047н		(Access prohibi	ited)			
000048н	TMCSRO	Timor control status register ch 0		00000000 _B		
000049н	TMCONU		16 bit relead timer 0	XXXX0000 _B		
00004Ан	TMR0/	16-bit timer register ch.0/		XXXXXXXXB		
00004Вн	TMRLR0	16-bit reload register ch.0		XXXXXXXXB		
00004Сн	TMCSD1	Timer central statue register of 1	16 bit relead timer 1	00000000		
00004Dн	INCONT	Timer control status register ch. I		XXXX0000 _B		
00004Ен	TMR1/	16-bit timer register ch.1/		XXXXXXXXB		
00004F н	TMRLR1	16-bit reload register ch.1		XXXXXXXXB		
000050н		ICI I data registar ab 0		XXXXXXXXB		
000051н				XXXXXXXXB		
000052н		ICI I data registor ch 1	16-bit I/O timer	XXXXXXXXB		
000053н				XXXXXXXXB		
000054н	ICS01	ICU control status register		00000000 _B		
000055н		(Access prohibi	ited)			
000056н	ΤΟΠΤΟ	Freerup timer data register 0		00000000 _B		
000057н			16-bit I/O timer	00000000 _B		
000058н	TCCS0	Freerun timer control status register 0		00000000 _B		
000059н	(Access prohibited)					
00005Ан		OCLL compare register ch 0		XXXXXXXXB		
00005Вн			16 bit I/O timor	XXXXXXXXB		
00005Cн		OCLI compare registor ch 1		XXXXXXXXB		
00005Dн				XXXXXXXXB		
00005Eн	0002	OCI I compare register ch 2	1	XXXXXXXXB		
00005Fн				XXXXXXXXB		

Address	Abbreviated Register Name	Register Name	Peripheral Name	Initial Value		
000060н	OCP3	OCI I compare register ch 3		XXXXXXXXB		
000061н	0013			XXXXXXXXB		
000062н	00501	OCLL control status register ch 0, ch 1	16-bit I/O timor	0000XX00 _B		
000063н	00301			XXX00000 _B		
000064н	00523	OCLL control status register ch 2, ch 3		0000XX00 _B		
000065н	00323			XXX00000 _B		
000066н		Freerup timer data register 1		00000000B		
000067н	ICDII		16-bit I/O timer	00000000B		
000068н	TCCS1	Freerun timer control status register 1		00000000B		
000069н		(Access prohibi	ted)	•		
00006Ан	LCR0	LCDC control register 0	LCD controller/driver	0001000B		
00006Вн	LCR1	LCDC control register 1		00000000B		
00006Сн	0007	OCU compare register ch 7	16 hit 1/0 timor	XXXXXXXXB		
00006Dн	UCF7	OCO compare register cn.7		XXXXXXXXB		
00006Ен	(Access prohibited)					
00006Fн	ROMM	ROM mirror function selection register	ROM mirror function selection module	XXXXXXX1B		
000070н to 00007Fн	VRAM	Data memory for LCD display	LCD controller/driver	XXXXXXXXB		
000080н	UDCR0	Up/down count register 0		0000000B		
000081н	UDCR1	Up/down count register 1		0000000B		
000082н	RCR0 Reload compare register 0		8/16-bit up/down	00000000B		
000083н	RCR1	Reload compare register 1		00000000B		
000084н	CSR0	Counter status register 0		00000000B		
000085н		(Reserved) *	3			
000086н	CCBO	Counter control register 0		Х000000в		
000087н	CCHU	Counter control register o	8/16-bit up/down	00000000B		
000088н	CSR1 Counter status register 1			0000000B		
000089н	(Reserved) *3					
00008Ан	CCB1	Counter control register 1	8/16-bit up/down	Х000000в		
00008Вн	CONT		counter/timer 0, 1	Х000000в		
00008Cн	RDR0	Port 0 input pull-up resistor setup register	Port 0	00000000 _B		
00008Dн	RDR1	Port 1 input pull-up resistor setup register	Port 1	0 0 0 0 0 0 0 0 0 _B		

(Continued)

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Address	Abbreviated Register Name	Register Name	Peripheral Name	Initial Value	
00008Eн	RDR4	Port 4 input pull-up resistor setup register	Port 4	00000000	
00008Fн to 00009Dн		(Access prohibi (Area reserved for sys	ited) tem use) ⁺⁴		
4 00009Ен	PACSR	Address detection control register	Address match detection function	0 0 0 0 0 0 0 0 _B	
00009Fн	DIRR	Delayed interrupt request output/clear register	Delayed interrupt generation module	XXXXXXX 0B	
0000A0 н	LPMCR	Low power consumption mode control register	Low power consumption	00011000 _B	
0000A1н	CKSCR	Clock selection register	(standby) mode	11111100 _в	
0000А2н to 0000А7н	(Access prohibited)				
0000А8 н	WDTC	Watchdog timer control register	Watchdog timer	XXXXXXXXB	
0000А9 н	TBTC	Timebase timer control register	Timebase timer	1 XX 0 0 0 0 _B	
0000ААн	WTC Clock timer control register		Clock timer	1 X 0 0 1 0 0 0в	
0000ABн to 0000ADн	(Access prohibited)				
0000АЕн	FMCS	Flash memory control status register	1 Mbit flash memory	000X000 _B	
0000AFн	(Access prohibited)				
0000В0н	ICR00	Interrupt control register 00		00000111в	
0000B1н	ICR01	Interrupt control register 01		00000111в	
0000В2н	ICR02	Interrupt control register 02		00000111в	
0000ВЗн	ICR03	Interrupt control register 03		00000111в	
0000B4н	ICR04	Interrupt control register 04		00000111в	
0000В5н	ICR05	Interrupt control register 05		00000111в	
0000В6н	ICR06	Interrupt control register 06	Interrupt controller	00000111в	
0000В7 н	ICR07	07 Interrupt control register 07		00000111 _в	
0000B8н	ICR08	Interrupt control register 08		00000111в	
0000В9н	ICR09	Interrupt control register 09		00000111в	
0000ВАн	ICR10	Interrupt control register 10		00000111в	
0000ВВн	ICR11	Interrupt control register 11		00000111в	
0000ВСн	ICR12	Interrupt control register 12		00000111в	
0000BDH	ICR13	Interrupt control register 13		00000111в	

(Continued)							
Address	Abbreviated Register Register Name Name		Peripheral Name	Initial Value			
0000BEH	ICR14	Interrupt control register 14	Interrupt controller	00000111 _B			
0000BFн	ICR15	Interrupt control register 15	00000111 _B				
0000C0н to 0000FFн		(Access prohibited) ^{*1}					
4 000100н to 00####н		(RAM area)	*2				
00####н to 001FEFн		(Reserved area	a) *3				
001FF0н		Detection address setting register 0 (low byte)		XXXXXXXX			
001FF1н	PADR0	Detection address setting register 0 (middle byte)		XXXXXXXX			
001FF2н		Detection address setting register 0 (high byte)	Address match	XXXXXXXX			
001FF3⊦		Detection address setting register 1 (low byte)	detection function	XXXXXXXX			
001FF4н	PADR1	Detection address setting register 1 (middle byte)		XXXXXXXXB			
001FF5⊦		Detection address setting register 1 (high byte)		XXXXXXXXB			
001FF6н to 001FFF⊦		(Reserved area	a) *3				

Initial value notation

0 : Initial value of bit is "0".

- 1 : Initial value of bit is "1".
- X : Initial value of bit is undefined.

*1 : Access is prohibited to the address range 0000C0_H to 0000FF_H. See the "■ MEMORY MAP" section.

*2 : See the "
MEMORY MAP" section for details of the " (RAM area) ".

*3 : " (Reserved areas) " are addresses used internally by the system and may not be used.

*4 : The " (Area reserved for system use) " contains setting registers used by the evaluation tools.

- Notes : LPMCR, CKSCR, and WDTC are initialized by some types of reset and not by others. The initial values listed are for the case when the registers are initialized.
 - The boundary address "#####" between the " (RAM area) " and " (Reserved area) " differs depending on the product. See the "■ MEMORY MAP" section for details.
 - OCU compare registers ch.0 to ch.3 use 16-bit freerun timer 0 and OCU compare registers ch.4 to ch.7 use 16-bit freerun timer 1. Note that 16-bit freerun timer 0 is also used by input capture 0 and 1 (ICU).

■ INTERRUPTS, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Intervent	El ² OS	Interr	rupt Vector Interrupt Control Registe		Control Register	Duiouitur
interrupt	Support	No.	Address	ICR	Address	Priority
Reset	×	#08	FFFFDC _H			High
INT 9 instruction	×	#09	FFFFD8H			
Exception	×	#10	FFFFD4 _H			
8/10-bit A/D converter	0	#11	FFFFD0H		000080	
Timebase timer	×	#12	FFFFCC H		0000000	
DTP0/DTP1 (external interrupt 0/external interrupt 1)	0	#13	FFFFC8⊦	ICR01	0000B1н	
16-bit freerun timer 0 overflow	×	#14	FFFFC4 _H			
Extended I/O serial interface 1	0	#15	FFFFC0H		0000820	
Wakeup interrupt	×	#16	FFFFBC _H	101102	0000D2H	
Extended I/O serial interface 2	0	#17	FFFFB8 _H			
DTP2/DTP3 (external interrupt 2/external interrupt 3)	0	#18	FFFFB4 _H	ICR03	0000B3н	
8/16-bit PPG timer 0 counter borrow	×	#19	FFFFB0н			
DTP4/DTP5 (external interrupt 4/external interrupt 5)	0	#20	FFFFACH	ICR04	0000B4н	
8/16-bit up/down counter/timer 0 compare match	0	#21	FFFFA8 _H		0000R5	
8/16-bit up/down counter/timer 0 overflow, up/down direction change	0	#22	FFFFA4 _H			
8/16-bit PPG timer 1 counter borrow	×	#23	FFFFA0 _H			
DTP6/DTP7 (external interrupt 6/external interrupt 7)	0	#24	FFFF9CH	ICR06	0000B6н	
Output compare 1 (OCU) ch.4, ch.5 match	0	#25	FFFF98н		0000B7	
Clock timer	×	#26	FFFF94н		0000878	
Output compare 1 (OCU) ch.6, ch.7 match	0	#27	FFFF90 _H		000088	
16-bit freerun timer 1 overflow	×	#28	FFFF8CH	101100	ООООВОН	
8/16-bit up/down counter/timer 1 compare match	0	#29	FFFF88⊦		000080	
8/16-bit up/down counter/timer 1 overflow, up/down direction change	0	#30	FFFF84 _H			
Input capture 0 (ICU) capture	0	#31	FFFF80H		0000BA	
Input capture 1 (ICU) capture	0	#32	FFFF7CH			
Output compare 0 (OCU) ch.0 match	0	#33	FFFF78н	ICB11	0000RR.	
Output compare 0 (OCU) ch.1 match	0	#34	FFFF74 _H			

(Continued)

Interrupt	El ² OS	Interr	upt Vector	Interrupt (Control Register	Priority
interrupt	Support	No.	Address	ICR	Address	FIIOIIty
Output compare 0 (OCU) ch.2 match	0	#35	FFFF70 _H		000086	
Output compare 0 (OCU) ch.3 match	0	#36	FFFF6CH	101112	0000BCH	
UART (SCI) receive complete	Ô	#37	FFFF68 _H	ICB13		
16-bit reload timer 0	0	#38	FFFF64 _H	101113	0000BDH	
UART (SCI) send complete	0	#39	FFFF60 _H		0000BEu	
16-bit reload timer 1	0	#40	FFFF5CH	10114	OOOBEH	
Flash memory	×	#41	FFFF58н		0000RE.	*
Delayed interrupt generation module	×	#42	FFFF54H		UUUUBFH	Low

○ : Supported

 \times : Not supported

 \odot : Supported, includes El²OS stop function

PERIPHERAL RESOURCES

1. I/O Ports

- The I/O ports can be used as general-purpose I/O ports (parallel I/O ports) . The MB90520A and 520B series have 11 ports (85 pins) . The ports share pins with the inputs and outputs of the peripheral functions.
- The port data registers (PDR) are used to output data to the I/O pins and capture the input signals from the I/O ports.
- Similarly, the port direction registers (DDR) set the I/O direction (input or output) for each individual port bit. • The following tables list the I/O ports and peripheral functions with which they share pins.

411.com	Pin Name (Port)	Pin Name (Peripheral)	Peripheral Function that Shares Pin
Port 0	P00 – P06	INT0 – INT6	External interrupts
TOILO	P07		Not shared
Port 1	P10 – P17	WI0 – WI7	Wakeup interrupts
	P20 – P23	IN00 – IN11	Input capture (unit 0)
Port 2	P24, P25	AIN0, BIN0	8/16-bit up/down counter/timer 0
	P26	ZIN0/INT7	8/16-bit up/down counter/timer 0, external interrupt
	P30	—	Not shared
Port 3	P31	СКОТ	Clock monitor function
FUILS	P32 – P35	OUT0 – OUT3	Output compare (unit 0)
	P36, P37	PPG00, PPG01	8/16-bit PPG timer 0
	P40, P41	PPG10, PPG11	8/16-bit PPG timer 1
Port 4	P42 – P44	SIN0, SOT0, SCK0	UART (SCI)
	P45 – P47	SIN1, SOT1, SCK1	Extended I/O serial interface 0
Port 5	P50 – P52	SIN2/AIN1, SOT1/BIN1, SCK1/ZIN1	8/16-bit up/down counter/timer 0 Extended I/O serial interface 1
	P53, P54	DA0, DA1	8-bit D/A converter
Port 6	P60 – P67	AN0 – AN7	8/16-bit A/D converter
Port 7	P70 – P73	TIN0/OUT4, TOT0/OUT5, TIN1/OUT6, TOT1/OUT7	16-bit reload timers 0, 1 Output compare (unit 1)
	P74 – P77	COM0 – COM3	LCD control driver common output
Port 8	P80 – P87	SEG16 – SEG23	LCD control driver segment output
Port 9	P90 – P97	SEG24 – SEG31	LCD control driver segment output
Port A	PA0 – PA7	SEG8 – SEG15	LCD control driver segment output

Notes

- Port 9 contains general-purpose I/O ports with N-ch open-drain output circuits.
- Connect an external pull-up resistor when using port 9 pins as outputs.
- Port 6 shares pins with the analog inputs. When using port 6 as a general-purpose port, ensure that the corresponding analog input enable register (ADER) bits are set to "0". ADER is initialized to "FFH" after a reset.



















2. Timebase Timer

- The timebase timer is an 18-bit freerun timer (timebase timer/counter) that counts up synchronized with the main clock (oscillation clock : HCLK divided by 2).
- The timer can generate interrupt requests at a specified interval, with four different interval time settings available.
- The timer supplies the operating clock for peripheral functions including the oscillation stabilization delay timer and watchdog timer.

Timebase timer interval settings

40 Internal Count Clock Period	Interval Time
	2 ¹² /HCLK (approx. 1.024 ms)
	2 ¹⁴ /HCLK (approx. 4.096 ms)
2/ΠΟΕΚ (0.5 μ5)	2 ¹⁶ /HCLK (approx. 16.384 ms)
	2 ¹⁹ /HCLK (approx. 131.072 ms)

HCLK : Oscillation clock frequency

• The values enclosed in () indicate the times for a clock frequency of 4 MHz.

• Period of clocks supplied from timebase timer

Peripheral Function	Clock Period
	2 ¹⁰ /HCLK (approx. 0.256 ms)
Oscillation stabilization delay	2 ¹³ /HCLK (approx. 2.048 ms)
for the main clock	2 ¹⁵ /HCLK (approx. 8.192 ms)
	2 ¹⁷ /HCLK (approx. 32.768 ms)
	2 ¹² /HCLK (approx. 1.024 ms)
Watchdog timor	2 ¹⁴ /HCLK (approx. 4.096 ms)
Walchuby limer	2 ¹⁶ /HCLK (approx. 16.384 ms)
	2 ¹⁹ /HCLK (approx. 131.072 ms)
PPG timer	2 ⁹ /HCLK (approx. 0.128 ms)

HCLK : Oscillation clock frequency

• The values enclosed in () indicate the times for a clock frequency of 4 MHz.


The actual interrupt request number for the timebase timer is :

Interrupt request number : #12 (0CH)

3. Watchdog Timer

- The watchdog timer is a timer/counter used to detect faults such as program runaway.
- The watchdog timer is a 2-bit counter that counts the clock signal from the timebase timer or clock timer.
- Once started, the watchdog timer must be cleared before the 2-bit counter overflows. If an overflow occurs, the CPU is reset.

• Interval time for the watchdog timer

HCLK : (Oscillation Clock (4	MHz)	SCLK : Sub-Clock (8.192 kHz)		
Min	Мах	Clock Period	Min	Max	Clock Period
Approx. 3.58 ms	Approx. 4.61 ms	$2^{14}\pm2^{11}$ / HCLK	Approx. 0.438 s	Approx. 0.563 s	$2^{12}\pm2^9/SCLK$
Approx. 14.33 ms	Approx. 18.30 ms	$2^{16}\pm2^{13}$ / HCLK	Approx. 3.500 s	Approx. 4.500 s	$2^{15} \pm 2^{12}$ / SCLK
Approx. 57.23 ms	Approx. 73.73 ms	$2^{18} \pm 2^{15}$ / HCLK	Approx. 7.000 s	Approx. 9.000 s	$2^{16} \pm 2^{13}$ / SCLK
Approx. 458.75 ms	Approx. 589.82 ms	$2^{21}\pm2^{18}$ / HCLK	Approx. 14.00 s	Approx. 18.00 s	$2^{17}\pm2^{14}/SCLK$

* : The difference between the maximum and minimum watchdog timer interval times is due to the timing when the counter is cleared.

* : As the watchdog timer is a 2-bit counter that counts the carry-up signal from the timebase timer or clock timer, clearing the timebase timer (when operating on HCLK) or the clock timer (when operating on SCLK) lengthens the time until the watchdog timer reset is generated.

Watchdog timer count clock

WTC : WDCS	HCLK : Oscillation clock PCLK : PLL clock	SCLK : Sub-clock
"0"	Count the clock timer output.	Count the clock timer output
"1"	Count the timebase timer output.	

• Events that stop the watchdog timer

- 1 : Stop due to a power-on reset
- 2 : Reset due to recovery from hardware standby mode
- 3 : Watchdog reset

• Events that clear the watchdog timer

- 1 : External reset input from the RST pin.
- 2 : Writing "0" to the software reset bit.
- 3 : Writing "0" to the watchdog control bit (second and subsequent times) .
- 4 : Changing to sleep mode (clears the watchdog timer and temporarily halts the count) .
- 5 : Changing to pseudo-clock mode (clears the watchdog timer and temporarily halts the count) .
- 6 : Changing to clock mode (clears the watchdog timer and temporarily halts the count) .
- 7 : Changing to stop mode (clears the watchdog timer and temporarily halts the count) .



4. 8/16-bit PPG (Programmable Pulse Generator) Timers 0 and 1

The 8/16-bit PPG timer is a two-channel reload timer module (PPG0 and PPG1) that can generate pulse outputs with the periods specified in the table below and with duty ratios between 0 and 100%. Note that the pulse periods are different depending on the operation mode.

Operation		PPG00, PPG0	01 (PPG ch0)	PPG10, PPG11 (PPG ch1)		
Mode	Mode Count Clock*2		Output Pulse Width	Interval Time	Output Pulse Width	
	¢/1 (62.5 ns)	1/φ to 2 ⁸ /φ	1/ǫ to 2º/ǫ	1/φ to 2 ⁸ /φ	1/φ to 2 ⁹ /φ	
er4U.com 8-bit	φ/2 (125 ns)	2/\$ to 2%	2²/\$ to 210/\$	2/φ to 2%	2²/\$ to 210/\$	
PPG output	¢/4 (250 ns)	2²/φ to 2¹º/φ	2 ³ /\$\$ to 2 ¹¹ /\$	2²/φ to 2¹º/φ	2³/φ to 2¹¹/φ	
Independent	φ/8 (500 ns)	2³/φ to 2¹¹/φ	24/\$ to 212/\$	2³/φ to 211/φ	24/\$ to 212/\$	
mode	∳/16 (1000 ns)	24/\$ to 212/\$	2 ⁵ /φ to 2 ¹³ /φ	24/\$ to 212/\$	2⁵/φ to 2¹³/φ	
	HCLK/512 (128 μs)	2 ⁹ /HCLK to 2 ¹⁷ /HCLK	2 ¹⁰ /HCLK to 2 ¹⁸ /HCLK	2 ⁹ /HCLK to 2 ¹⁷ /HCLK	2 ¹⁰ /HCLK to 2 ¹⁸ /HCLK	
	¢/1 (62.5 ns)	1/φ to 2¹6/φ	1/φ to 2 ¹⁷ /φ	1/φ to 2¹6/φ	1/φ to 2 ¹⁷ /φ	
	φ/2 (125 ns)	2/\$ to 217/\$	2²/\$ to 218/\$	2/\$ to 217/\$	2²/\$ to 218/\$	
16-bit PPG output	¢/4 (250 ns)	2²/φ to 2¹8/φ	2³/φ to 219/φ	2²/φ to 2¹8/φ	2³/φ to 2¹9/φ	
operation	∳/8 (500 ns)	2³/φ to 2¹9/φ	24/\$ to 220/\$	2³/φ to 2¹9/φ	24/\$ to 220/\$	
mode	∳/16 (1000 ns)	2⁴/ϕ to 2²⁰/ϕ	2 ⁵ /\$ to 2 ²¹ /\$	2⁴/ϕ to 2²⁰/ϕ	2⁵/∳ to 2²¹/∳	
	HCLK/512 (128 μs)	2 ⁹ /HCLK to 2 ²⁵ /HCLK	2 ^{10/} HCLK to 2 ^{26/} HCLK	2 ⁹ /HCLK to 2 ²⁵ /HCLK	2 ^{10/} HCLK to 2 ²⁶ /HCLK	
	¢/1 (62.5 ns)	1/φ to 2 ⁶ /φ	1/ǫ to 2º/ǫ	1/φ to 2¹6/φ	1/φ to 2 ¹⁷ /φ	
	φ/2 (125 ns)	2/\$ to 29/\$	2²/\$ to 210/\$	2/φ to 217/φ	2²/\$ to 218/\$	
8 + 8-bit	¢/4 (250 ns)	2²/\ to 210/\	2 ³ /\$ to 2 ¹¹ /\$	2²/\phi to 2 ¹⁸ /\phi	2 ³ /\$ to 2 ¹⁹ /\$	
operation	φ/8 (500 ns)	2³/ϕ to 211/ϕ	24/\$ to 212/\$	2³/φ to 2¹9/φ	24/\$ to 220/\$	
mode ^{*1}	φ/16 (1000 ns)	24/\$ to 212/\$	25/\$ to 213/\$	24/\$ to 220/\$	2⁵/φ to 2²¹/φ	
	HCLK/512 (128 μs)	2 ⁹ /HCLK to 2 ¹⁷ /HCLK	2 ^{10/} HCLK to 2 ^{18/} HCLK	2 ⁹ /HCLK to 2 ²⁵ /HCLK	2 ^{10/} HCLK to 2 ²⁶ /HCLK	

*1 : 8 + 8-bit PPG output operation mode consists of using the lower 8 bits as a prescaler for the PPG timer.

*2 : The values enclosed in () indicate the times for a machine clock frequency of 16 MHz.

• PPG timer channels and PPG pins

The figure below shows the relationship between the 8/16-bit PPG channels and PPG pins on the MB90520A/ 520B series.







5. 16-bit Reload Timers 0 and 1 (With Event Count Function)

The 16-bit reload timers have the following functions.

- The count clock can be selected from three internal clock and the external event clock.
- Either software trigger or external trigger can be selected as the start signals for 16-bit reload timers 0 and 1.
- An interrupt to the CPU can be generated when an underflow occurs on 16-bit reload timer 0 and 1. This interrupt allows the timers to be used as interval timers.
- Two different operation modes can be selected when an underflow occurs on 16-bit reload timer 0 and 1 : oneshot mode in which timer operation halts when an underflow occurs or reload mode in which the reload register value is loaded into the timer and counting continues.
- www.DataSheet4U.e.Extended intelligent I/O service (EI2OS) is supported.
 - The MB90520A/520B series contains two 16-bit reload timer channels.

• 16-bit reload timer operation modes

Count Clock	Start Trigger	Operation when an Underflow Occurs
	Software trigger	One-shot mode
Internal clock	Software ingger	Reload mode
(3 clocks available)	External trigger	One-shot mode
	External ingger	Reload mode
	Software trigger	One-shot mode
Event clock	Software ingger	Reload mode
EVEN CIOCK	External trigger	One-shot mode
	External ingger	Reload mode

• Interval times for the 16-bit reload timers

Count Clock	Count Clock Period	Example Interval Times
	2¹T (0.125 μs)	0.125 μs to 8.192 ms
Internal clock	2³T (0.5 μs)	0.5 μs to 32.768 ms
	2⁵T (2.0 μs)	2.0 μs to 131.1 ms
Event clock	2 ³ T or longer	0.5 μs or longer

Note : The values enclosed in () and the example interval times are for a machine clock frequency of 16 MHz. "T" is the machine cycle and is 1/ (machine clock frequency).



6. 16-bit I/O Timers

The 16-bit I/O timers consist of a two-channel 16-bit freerun timer, two-channel input capture, and eight-channel output compare. The output compare channels can be used to generate eight independent waveform outputs based on the 16-bit freerun timer. The input capture channels can be used to measure input pulse widths and external clock periods.

• Structure of I/O timers in the MB90520A/520B series

	16-bit Freerun Timer	Output Compare	Input Capture
16-bit I/O timer ^{4U.com} (unit 0)	16-bit freerun timer 0	Output compare 0 to 3 (unit 0)	Input capture 0 and 1 (unit 0)
16-bit I/O timer (unit 1)	16-bit freerun timer 1	Output compare 4 to 8 (unit 1)	

• 16-bit freerun timer functions

- The count value for the 16-bit freerun timer sets the base time for the input capture and output compare functions.
- An interrupt can be generated when the 16-bit freerun timer overflows.
- Extended intelligent I/O service (El²OS) can be generated.
- 16-bit freerun timers 0 and 1 can be cleared to "0000+" when an external reset is input, on setting the timer clear bit (TCCS : CLR = 1), and when a compare match occurs on output compare 0 to 4.
- The count clock frequency can be selected from the following four clocks : $4/\phi$ (250 ns), $16/\phi$ (1.0 µs), $64/\phi$ (4.0 µs), $256/\phi$ (16.0 µs)

Note : ϕ is the machine clock frequency. The values in () are for 16 MHz machine clock.

Input capture functions

- The input capture saves the value of the 16-bit freerun timer and generates an interrupt request when the specified edge is detected on the trigger input from the external trigger input pin (IC00 or IC01/IC10 or IC11).
- Input capture channels 0 and 1 can perform input capture and generate interrupt request independently.
- Extended intelligent I/O service (El²OS) can be generated.
- Detection of rising edges, falling edges, or either edge can be selected as the trigger edge.
- When using input capture 0, either the IC00 or IC01 pin can be used. Note, however, that masking one pin only is not possible.
- When using input capture 1, either the IC10 or IC11 pin can be used. Note, however, that masking one pin only is not possible.

Output compare functions

- The output compare channels compare the values set in output compare registers 0 to 7 with the 16-bit freerun timers 0 and 1 count values and invert the level of the corresponding output compare pin and clear the 16-bit freerun timer to "0000H" when a match is detected.
- Extended intelligent I/O service (El²OS) can be generated.
- The initial output levels at the output compare pins can be set after the microcontroller boots.
- The output levels from the eight output compare channels are controlled independently. Similarly, interrupt requests are also generated independently by each channel.







7. 8/16-bit Up/Down Counter/Timers 0 and 1

- The 8/16-bit up/down counter/timers can operate in timer mode, up/down count mode, and phase difference count mode.
- The unit can be used as either a 2-channel × 8-bit or 1-channel × 16-bit up/down counter/timer.

	Operation Mode	Count Mode	Count Clock (Count Edge)	Function of ZIN Pin	Other Functions
Sheel	4U.com	Timer mode	2/φ, 4/φ (φ : Machine clock frequency)	_	
		Up/down count	Counts up on detecting speci- fied edge on the AIN pin.	Counter clear function	
		mode	Counts down on detecting spec- ified edge on the BIN pin.	Gate function	
	8-bit	Phase difference count	Reads the AIN pin input level on detecting a rising or falling edge	Counter clear function	
	×2-channel mode	(multiply by 2)	counts down.	Gate function	
		Phase	Reads the AIN pin input level on detecting a rising or falling edge	Counter clear function	Compare function Beload function
		difference count mode (multiply by 4)	ference count mode multiply by 4) (AIN pin and counts up of counts down. Similarly, reads the BIN pin input level on detec ing a rising or falling edge on the AIN pin and counts up or counts down.	Gate function	 Compare/reload function Compare/reload prohibit The direction of the previous count can be determined from the up/ down flag
	-	Timer mode	2/φ, 4/φ (φ : Machine clock frequency)	_	 Interrupt requests can be generated on the following
		Up/down count	Counts up on detecting speci- fied edge on the AIN pin.	Counter clear function	conditions : 1 : Compare match
		mode	ified edge on the BIN pin.	Gate function	3 : Count direction
	16-bit	Phase difference count	Reads the AIN pin input level on detecting a rising or falling edge	Counter clear function	change
	× 1-channel mode	mode (multiply by 2)	counts down.	Gate function	
		Phase	Reads the AIN pin input level on detecting a rising or falling edge	Counter clear function	
		difference count mode (multiply by 4)	counts down. Similarly, reads the BIN pin input level on detect- ing a rising or falling edge on the AIN pin and counts up or counts down.	Gate function	

• 8/16-bit up/down counter/timer functions





• Pins and interrupt numbers

8/16-bit up/down counter/timer 0 AIN0 pin : P24/AIN0 BIN0 pin : P25/BIN0 ZIN0 pin : P26/ZIN0 Compare match interrupt number : #21 (15_H) Interrupt number for underflow/overflow interrupt, count direction change interrupt : #2 (16_H)

8/16-bit up/down counter/timer 1 AIN1 pin : P50/AIN1 BIN1 pin : P51/BIN1 ZIN1 pin : P52/ZIN1 Compare match interrupt number : #29 (1DH) Interrupt number for underflow/overflow interrupt, count direction change interrupt : #3 (1EH)

8. Extended I/O Serial Interfaces 0 and 1

- The extended I/O serial interfaces are serial I/O interfaces that perform clock-synchronized data transfer.
- The MB90520A/520B series contain two internal extended I/O serial interface channels.
- Either LSB-first or MSB-first data transmission format can be selected.

• Extended I/O serial interface functions

		Function
	Transmission direction	• Transmit and receive can be handled simultaneously. (A setting is required to select transmit or receive.)
www.DataShee	⁴⁰ Transmission mode	Clock synchronous (data transfer only)
	Transmission clock	 Internal shift clock mode (Uses the communications prescaler output clock.) External shift clock mode (Inputs the clock signal from SCK1 and SCK2.)
	Transmission speed	 When using internal shift clock : Up to 1 MHz operation can be achieved (for a 16 MHz machine clock with the divisor setting for the communication prescaler set to 8) . Speeds faster than 1 MHz are not possible. When using an external shift clock : As a minimum of 5 machine cycles are required, when the machine clock is 16 MHz the maximum input frequency for the external shift clock is 16 MHz / 5 = 3.2 MHz.
	Data transmission format	 LSB-first or MSB-first, selectable Data transfer only Number of data bits = 8 (fixed)
	Interrupt request generation	Interrupt generated when transfer completes
	EI ² OS support	Supports use of the extended intelligent I/O service.



9. UART (SCI : Serial Communication Interface)

- The UART (SCI) is a general-purpose serial communications interface for performing synchronous or asynchronous communications with external devices.
- The interface provides bi-directional communications in both clock synchronous and clock asynchronous modes.
- Includes a master-slave communication function (multi-processor mode) .
- Can generate interrupt requests at receive complete, receive error detected, and transmit complete timings. Also supports El²OS.

	Function
Data buffer	Full-duplex double-buffered
Transmission modes	 Clock synchronous (with no start/stop bit, no parity bit) Clock asynchronous (start-stop sync)
Baud rate	 Can use dedicated baud rate generator. Can use external clock input. Can use clock supplied by 16-bit reload timer 0. For machine clock speeds of 6 MHz, 8 MHz, 10 MHz, 12 MHz, and 16 MHz : Available speeds for asynchronous communications : 31250 bps, 9615 bps, 4808 bps, 2404 bps, and 1202 bps Available speeds for synchronous communications : 1 Mbps, 500 Kbps, 250 Kbps, 125 Kbps, and 62.5 Kbps
Number of data bits	 7 bits (when parity is used for asynchronous normal mode) 8 bits (when parity is not used)
Signal format	 Non return to zero (NRZ) format
Receive error detection	 Framing errors (not available in clock synchronous mode) Overrun errors Parity errors (not available in clock synchronous mode and multi-processor mode)
Interrupt requests	 Receive interrupt (Receive complete or receive error detected) Transmit interrupt (Transmission complete) Both transmit and receive support the extended intelligent I/O service (EI²OS) .
Master/slave communication function (multi-processor mode)	• Used for 1 (master) to n (slave) communications. (Can only be used as master)
El ² OS support	Supports the extended intelligent I/O service (El ² OS)

• UART (SCI) functions

	Operation Mode			ata Bits	Parit	y Bit	No. of S	top Bits
				8 bits	None	Use	1 bit	2 bits
Mode 0	Asynchronous	Normal mode (1-to-1)	0	0	0	0	0	0
Mode 1	Asynchronous	Multi-processor mode (1-to-n)	×	O (+1)	0	×	0	0
Mode 2	Clock synchronous	Clock synchronous mode (one-to-one)	×	0	0	×	×	×

• UART (SCI) operation modes

○ : Available

- \times : Not available
- +1 : Address/data bit used for communication control

Notes :

- The number of data bits must be set to eight for multi-processor and clock synchronous modes.
- A parity bit cannot be used in multi-processor and clock synchronous modes.
- Only data can be transferred in clock synchronous mode. Start and stop bits cannot be added to the transmission data.



10. DTP (Data Transfer Peripheral) /External Interrupt Circuit

The DTP/external interrupt function detects interrupt requests and data transfer requests input from external devices and passes these to the CPU as external interrupt requests. This block can also activate the extended intelligent I/O service (El²OS).

• DTP/external interrupt functions

		External Interrupt	DTP Function		
Ĩ	Input pins	8 channels (INT0 to INT7)			
neet	4U.com Interrupt	• Can be set independently for each channel (each pin) in the detection level setup (ELVR) .			
	conditions	 "H" level, "L" level, rising edge, or falling edge input 	"H" level or "L" level input		
Interrupt control • Interrupts can be enabled or disabled in the DTP/external intervention		DTP/external interrupt enable register (ENIR) .			
Ī	Interrupt flag	• The DTP/external interrupt request register (EIRR) stores interrupt requests.		
	Processing selection	 Set El²OS to be disabled (ICR : ISE = 0) 	• Set EI^2OS to be enabled (ICR : ISE = 1)		
Ĩ	Interrupt execution	Jumps to interrupt handler routine Jumps to interrupt handler routine automatic data transfer by El ² OS c			
Ī	El ² OS support	 Supports the extended intelligent I/O service 	e (El²OS)		



11. Wakeup Interrupts

- The wakeup interrupt function detects wakeup interrupt requests from external devices by detecting "L" levels input to the wakeup interrupt input pins (WI0 to WI7) and passes these to the CPU for interrupt processing.
- Wakeup interrupts can be used to wakeup the microcontroller from standby mode. (However, wakeup interrupts cannot be used to recover from hardware standby mode.)
- Not supported by the extended intelligent I/O service (EI2OS) .

Wakeup interrupt functions

		Function and Control
nee	^{4U.com} Input pins	 8 channels (8 pins : WI0 to WI7)
	Interrupt trigger	 "L" level inputs. One interrupt flag is shared by all eight channels.
	Interrupt control	 Interrupt requests can be enabled or disabled in the wakeup interrupt control register (EICR).
	Interrupt flag	 Interrupt requests are stored in the wakeup interrupt flag register (EIFR).
	EI ² OS support	 Not supported by the extended intelligent I/O service (EI²OS).



12. Delayed Interrupt Generation Module

The delayed interrupt generation module is used to generate the task switching interrupt. Generation of this hardware interrupt can be specified by software.

• Delayed interrupt generation module functions

		Function and Control
aSheei	Interrupt trigger 4U.com	 Writing "1" to bit R0 of the delayed interrupt request generation/clear register (DIRR : R0 = 1) generates an interrupt request. Writing "0" to bit R0 of the delayed interrupt request generation/clear register (DIRR : R0 = 0) clears the interrupt request.
	Interrupt control	 No enable/disable register is provided for this interrupt.
	Interrupt flag	• Set in bit R0 of the delayed interrupt request generation/clear register (DIRR : R0) .
	EI ² OS support	 Not supported by the extended intelligent I/O service (EI²OS).



13. 8/10-bit A/D Converter

- The 8/10-bit A/D converter uses RC successive approximation to convert analog input voltages to an 8-bit or 10-bit digital value.
- The input signals can be selected from the eight analog input pin channels.
- Either a software trigger, internal timer output, or external pin trigger can be selected to trigger the start of A/ D conversion.

• 8/10-bit A/D converter functions

	Function
A/D conversion time	 Sampling time : Can be selected from 64, 128, or 4096 machine cycles. The minimum is 4 μs. Compare time : Can be selected from 44, 99, or 176 machine cycles. The minimum is 4.4 μs. A/D conversion time = sampling time + conversion time. The minimum A/D conversion time is 10.2 μs.
Conversion method	RC successive approximation with sample & hold circuit
Resolution	8-bit or 10-bit, selectable
Analog input pins	 Up to eight channels can be used. However, two or more channels cannot be used simultaneously.
Interrupts	 An interrupt request can be generated when A/D conversion completes.
A/D conversion start trigger	Selectable : software, internal timer output, or falling edge on input from external pin
El ² OS support	 Supported by the extended intelligent I/O service (EI²OS).

• 8/10-bit A/D converter conversion modes

	Description
Single-shot conversion mode	Performs A/D conversion sequentially from the start channel to the end channel. A/D conversion halts after conversion completes for the end channel.
Continuous conversion mode	Performs A/D conversion sequentially from the start channel to the end channel. A/D conversion starts again from the start channel after conversion completes for the end channel.
Incremental conversion mode	A/D conversion is performed for one channel then halts until the next trigger. After conversion is performed for the end channel, the next conversion is performed for the start channel, and repeated this operation.



14. 8-bit D/A Converter

- The 8-bit D/A converter performs R-2R D/A conversion with 8-bit resolution.
- Two D/A converter channels with independent analog outputs are provided.

• D/A converter functions

	Function
D/A conversion time	•The settling time is 12.5 μ s. This is independent of the machine clock.
Conversion method	R-2R conversion
el4U.com Resolution	• 8-bit
Analog output pins	 Two output pins are provided. Both pins can be used simultaneously.
Interrupts	• None
D/A conversion trigger	• Set the digital value in the D/A data register (DADR) , then enable D/A output in the D/A control register (DACR) to start analog output from the D/A output pin.
EI ² OS support	 Not supported by the extended intelligent I/O service (EI²OS).

• D/A converter theoretical output voltage

D/A Data Register Setting	Theoretical Output Voltage Value
00н	$0 / 256 \times DV_{CC}$ voltage (= 0 V)
00н	$1 / 256 \times DV_{CC}$ voltage
•••	•••
FE	254 / 256 $ imes$ DVcc voltage
FF	255 / 256 $ imes$ DVcc voltage

Note : DVcc voltage : D/A converter reference voltage. This must not exceed Vcc. Also, always ensure that DVss is equipotential to Vss.



15. Clock Timer

- The clock timer is a 15-bit freerun timer that counts up synchronized with the sub-clock.
- Seven different interval time settings are available.
- This timer provides the clock for the sub-clock's oscillation stabilization delay timer and the watchdog timer.
- This timer always counts the sub-clock, regardless of the settings in the clock selection register (CKSC) .

Clock timer functions

	Function
Interval time	Selectable from the seven settings shown in the table below.
Clock timer size	• 15-bit
Clock supply	Oscillation stabilization delay timer for sub-clock and watchdog timer
Source clock	Sub-oscillation clock divided by four. (SCLK : Sub-clock)
Interrupts	Interval time overflow
EI ² OS support	Not supported by the extended intelligent I/O service (El ² OS).

Clock timer interval times

Sub-Clock Period	Interval Time
	2 ⁹ /SCLK (approx. 62.5 ms)
	2 ¹⁰ /SCLK (approx. 125.0 ms)
	2 ¹¹ /SCLK (approx. 250.0 ms)
SCLK (122 μs)	2 ¹² /SCLK (approx. 500.0 ms)
	2 ¹³ /SCLK (approx. 1.0 s)
	2 ¹⁴ /SCLK (approx. 2.0 s)
	2 ¹⁶ /SCLK (approx. 4.0 s)

SCLK : Sub-clock frequency

The values enclosed in () are the times for a sub-clock frequency of 8.192 kHz.

Note that the sub-oscillation clock is divided by four to generate the sub-clock frequency. The sub-oscillation clock operates at 32.768 kHz.

· Clock periods generated by clock timer

Clock Supply	Clock Period
Oscillation stabilization delay timer for sub-clock	2 ¹⁴ /SCLK (approx. 2.0 s)
	2 ¹⁰ /SCLK (approx. 125.0 ms)
Watebdag timor	2 ¹³ /SCLK (approx. 1.0 s)
Watchdog timer	2 ¹⁴ /SCLK (approx. 2.0 s)
	2 ¹⁶ /SCLK (approx. 4.0 s)

SCLK : Sub-clock frequency

The values enclosed in () are the times for a sub-clock frequency of 8.192 kHz.

Note that the sub-oscillation clock is divided by four to generate the sub-clock frequency. The sub-oscillation clock operates at 32.768 kHz.



16. LCD Controller/Driver

- The LCD controller/driver can drive an LCD (Liquid Crystal Display) directly.
- The LCD is driven by 4 common outputs and 32 segment outputs.
- The output mode can be set to 1/2, 1/3, or 1/4 duty.

• LCD controller/driver functions

		Function
	Divider resistor for LCD drive power	• Either the internal resistor (approx. 100 k Ω) or an externally connected resistor can be selected.
www.DataSheel	4U.com Common outputs	 Max 4 outputs (The corresponding pins cannot be used as I/O ports when using an LCD.)
	Segment outputs	Max 32 outputs (of these, 24 pins can be used as I/O ports in blocks of 8 pins.)
	Display data memory	 16 bytes of RAM for internal display are provided
	Duty	• 1/2, 1/3, or 1/4 can be selected.
	Bias	 1/3 only supported
	Drive clock	• Either the oscillation clock (HCLK) or sub-clock (SCLK) can be used.
	Interrupts	• None
	EI ² OS support	 Not supported by the extended intelligent I/O service (EI²OS).

• Bias, duty, and common output combinations

Bias	1/2 Duty Output Mode	1/3 Duty Output Mode	1/4 Duty Output Mode
1/3 bias	COM0 and COM1 outputs	COM0 to COM2 outputs	COM0 to COM3 outputs
	used	used	used



17. Communications Prescaler

- Supplies the clock to the dedicated baud rate generator used by the UART (SCI) and extended I/O serial interfaces.
- By dividing the machine clock to produce the clock supply to the dedicated baud rate generator, the baud rate can be specified independently of the machine clock speed.
- The communications prescaler can divide the machine clock frequency φ by the following seven ratios to generate the clock supply to the dedicated baud rate generator and extended I/O serial interface : φ/2, φ/3, φ/4, φ/5, φ/6, φ/7, φ/8

• Communications prescaler functions

	Function
Clock supply	• Dedicated baud rate generator for the UART (SCI) and the extended I/O serial interface. However, the same clock is supplied to both peripherals.
Divided clock frequency	 φ/2, φ/3, φ/4, φ/5, φ/6, φ/7, φ/8 (φ : Machine clock frequency)
Interrupts	• None
EI ² OS support	 Not supported by the extended intelligent I/O service (EI²OS).

Note: As the same output from the communications prescaler is supplied to both the UART (SCI) and the extended I/O serial interface, the transfer clock speed settings must be revised if the communications prescaler settings are changed.



18. Address Match Detection Function

- If the program address during program execution matches the value set in one of the detection address setting registers (PADR), the address match detection function replaces the instruction being executed with the INT9 instruction and executes the interrupt handler program.
- The address match detection function provides a simple method of correcting programming errors (patching) using RAM or similar.

Address match detection functions

		Function
ee	⁴ UNo? of address settings	 Two channels (two addresses can be set)
	Interrupts	 An interrupt is generated when the program address matches the detection address setting register.
	EI ² OS support	 Not supported by the extended intelligent I/O service (El²OS).



19. ROM Mirror Function Selection Module

The ROM mirror function selection module enables ROM data in FF bank to be read by accessing 00 bank.

• ROM mirror function selection module functions

		Function
et	Mirror setting address	• Data in FFFFFF _H to FF4000 _H in FF bank can be read from 00FFFF _H to 004000 _H in 00 bank.
	Interrupts	• None
	4U.com El ² OS support	 Not supported by the extended intelligent I/O service (El²OS).

• Relationship between addresses in the ROM mirror function





20. Low Power Consumption (Standby) Modes

The power consumption of F²MC-16LX devices can be reduced by various settings relating to the operating clock selection.

CP	U Operation Clock	Operation Mode	Explanation
	PLL clock	Normal run	The CPU and peripheral functions operate using the oscillation clock (HCLK) mul- tiplied by the PLL circuit.
heel4U.c		Sleep	The peripheral functions only operate using the oscillation clock (HCLK) multiplied by the PLL circuit.
		Pseudo- clock	The timebase timer only operates using the oscillation clock (HCLK) multiplied by the PLL circuit.
		Stop	The oscillation clock is stopped and the CPU and peripherals halt operation.
	Main clock	Normal run	The CPU and peripheral functions operate using the oscillation clock (HCLK) divided by 2.
Ν		Sleep	The peripheral functions only operate using the oscillation clock (HCLK) divided by 2.
		Stop	The oscillation clock is stopped and the CPU and peripherals halt operation.
	Sub-clock	Normal run	The CPU and peripheral functions operate using the sub-clock (SCLK) . The os- cillation clock stops.
		Sleep	The peripheral functions only operate using the sub-clock (SCLK) . The oscillation clock stops.
		Clock	The clock timer only operates using the sub-clock (SCLK) . The oscillation clock stops.
		Stop	The oscillation clock and sub-clock are stopped and the CPU and peripherals halt operation.
ir	CPU ntermittent operation	Normal run	The oscillation clock (HCLK) divided by 2 operates intermittently for fixed time in- tervals.
	Hardware standby	Stop	The oscillation clock and sub-clock are stopped and the CPU and peripherals halt operation.

• Functions of each CPU operation mode
21. Clock Monitor Function

The clock monitor function outputs the machine clock divided by a specified amount to the clock monitor pin (CKOT) .

Clock monitor functions

	Function
Output frequency	 Machine clock divided by 2 to 32 (8 settings available)
Interrupts	• None
el4U.com El ² OS support	 Not supported by the extended intelligent I/O service (EI²OS).

• Output frequency of the clock monitor function

FRQ2 - 0 Machine Clock		When $\varphi=$ 16 MHz		When ϕ	= 8 MHz	When $\phi = 4 \text{ MHz}$		
Bits	Divide Ratio	Period	Frequency	Period	Frequency	Period	Frequency	
000в	φ/2 ¹	125 ns	8 MHz	250 ns	4 MHz	500 ns	2 MHz	
001 B	φ/ 2 ²	250 ns	4 MHz	500 ns	2 MHz	1.0 μs	1 MHz	
010в	φ/ 2 ³	500 ns	2 MHz	1.0 μs	1 MHz	2.0 μs	500 kHz	
011в	φ/2 ⁴	1.0 μs	1 MHz	2.0 μs	500 kHz	4.0 μs	250 kHz	
100в	φ/ 2 ⁵	2.0 μs	500 kHz	4.0 μs	250 kHz	8.0 μs	125 kHz	
101в	φ/2 ⁶	4.0 μs	250 kHz	8.0 μs	125 kHz	16.0 μs	62.5 kHz	
110в	φ/ 2 ⁷	8.0 μs	125 kHz	16.0 μs	16.0 μs 62.5 kHz		31.25 kHz	
111в	φ/ 2 ⁸	16.0 μs	62.5 kHz	32.0 μs	32.0 μs 31.25 kHz		15.625 kHz	

Block diagram



22. 1 Mbit Flash Memory

- This section describes the flash memory on the MB90F523B and does not apply to evaluation products and MASK ROM versions.
- The flash memory is located in banks FE to FF in the CPU memory map.

• Flash memory functions

	Function
Memory size	• 1 Mbit (128 KBytes)
Memory configuration	• 128 KWords \times 8 bits or 64 KWords \times 16 bits
Sector configuration	 16 KBytes + 8 KBytes + 8 KBytes + 32 KBytes + 64 KBytes
Sector protect function	Selectable for each sector
Programming algorithm	 Automatic programming algorithm (Embedded Algorithm[*] : Equivalent to MBM29F400TA)
Operation commands	 Compatible with JEDEC standard commands Includes an erase pause and restart function Data polling and toggle bit write/erase completion Erasing by sector available (sectors can be combined in any combination)
No. of write/erase cycles	Min 10,000 guaranteed
Memory write/erase method	 Can be written and erased using a parallel writer (Minato Electronics model 1890A, Ando Denki AF9704, AF9705, AF9706, AF9708, and AF9709) Can be written and erased using a dedicated serial writer (YDC AF200, AF210, AF120, and AF110) Can be written and erased by the program
Interrupts	Write and erase completion interrupts
El ² OS support	 Not supported by the extended intelligent I/O service (EI²OS).

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

Sector configuration of flash memory

Flash memory	CPU address	Writer address*
	FE0000H	60000н
SAU (64 KDyte)	FEFFFH	6FFFH
	FF0000н	70000н
SAT (32 RDyle)	FF7FFFH	77FFFн
CAO(O Xh) to	FF8000н	78000н
SA2 (8 KDyle)	FF9FFFH	79FFFн
	FFA 000н	7А000н
SA3 (8 Kbyte)	FFBFFFH	7BFFFн
	FFC000H	7С000н
SA4 (16 Kbyte)	FEFFFFH	7FFFFH

* : The writer address is the address to use instead of the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing using a general-purpose parallel writer.

 Pins used for Fujitsu Microelectronics standard serial on-board progr 	amming
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Pin	Function	Explanation				
MD2, MD1, MD0	Mode pins	Setting MD2 = MD1 = 1, MD0 = 0 selects flash memory serial program- ming mode.				
X0, X1	Oscillation input pin	Flash memory serial programming mode uses the PLL clock with the multiplier set to 1 as the machine clock. Set the oscillation frequency used for serial programming to between 3 MHz and 16 MHz.				
P00, P01	Write program activation pins	Input P00 = 0 ("L" level) and P01 = 1 ("H" level)				
RST	Reset pin	—				
HST	Hardware standby pin	Input an "H" level during flash memory serial programming mode.				
SIN0	Serial data input pin					
SOT0	Serial data output pin	Uses the UART (SCI) in clock synchronous mode.				
SCK0	Serial clock input pin					
С	C pin	Capacitor pin for power supply stabilization. Connect an external capacitor of approx. 0.1 $\mu\text{F}.$				
Vcc	Power supply voltage pins	If the user system can provide the programming voltage (5 V \pm 10%) , do not need to connect to the flash microcontroller writer.				
Vss	GND pin	Connect to common GND with the flash microcontroller writer.				

• Overall configuration of connection between serial writer and MB90F523A

Fujitsu Microelectronics standard serial on-board programming uses a flash microcontroller writer made by YDC.



Note : Contact YDC for details of the functions and operation of the flash microcontroller writer (AF220, AF210, AF120, or AF110) , standard connection cable (AZ210) , and connectors.

Electrical Characteristics\

1. Absolute Maximum Ratings

(Vss = AVss = 0.0 V)

Beremeter	Symbol	Rat	ting	Unit	Bomorko
Falameter	Symbol	Min	Max	Unit	nemarks
	Vcc	Vss - 0.3	Vss + 6.0	V	
	AVcc	Vss - 0.3	Vss + 6.0	V	*1
Power supply voltage	AVRH, AVRL	Vss - 0.3	Vss + 6.0	V	*1
	DVcc	Vss - 0.3	Vss + 6.0	V	*2
Input voltage	Vı	Vss - 0.3	Vss + 6.0	V	*3
Output voltage	Vo	Vss - 0.3	Vss + 6.0	V	*3
"L" level maximum output current	lo∟	—	15	mA	*4
"L" level average output current	Iolav	—	4	mA	*5
"L" level total maximum output current	ΣΙοι	—	100	mA	
"L" level total average output current	ΣΙοιαν	—	50	mA	*6
"H" level maximum output current	Іон	—	–15	mA	*4
"H" level average output current	Іонач	—	-4	mA	*5
"H" level total maximum output current	ΣІон	—	-100	mA	
"H" level total average output current	ΣΙοήαν		-50	mA	*6
Power consumption	Pd		400	mW	MB90522A/523A/ F523B
			300	mW	MB90522B/523B
Operating temperature	Та	-40	+85	°C	
Storage temperature	Tstg	-55	+150	°C	

*1 : AVcc, AVRH, AVRL, and DVcc shall never exceed Vcc . AVRH and AVRL shall never exceed AVcc. Also, AVRL shall never exceed AVRH.

*2 : Vcc \geq AVcc \geq DVcc \geq 3.0 V.

*3 : V1 and Vo shall never exceed Vcc + 0.3 V.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output current is the average current value for a single pin during a 100 ms period.

*6 : The total average current is the average current for all pins during a 100 ms period.

Note : Average output current = operating current \times operating ratio

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(Vss = AVss = 0.0 V)

Paramotor	Symbol	Value		Unit	Pomarka
Falanetei	Symbol	Min	Max	Onic	nemarks
Power supply voltage	Vcc	3.0	5.5	V	
Smoothing capacitor	Cs	0.1	1.0	μF	
Operating temperature	Та	-40	+85	°C	

Note : Use a ceramic capacitor or other capacitor with equivalent frequency characteristics. The capacitance of the smoothing capacitor connected to the Vcc pin must be greater than Cs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



3. DC Characteristics

(AVcc = Vcc = 5.0 V \pm 10%, AVss = Vss = DVss = 0.0 V, Ta = -40 °C to +85 °C)

Parameter	Sym-	ⁿ⁻ Pin Name Condition			Value	Unit	Remarks	
rarameter	bol	r in Name	Condition	Min	Тур	Max	Onit	Hemarks
"H" level input voltage el40.com	Viнs	P20 to P27, P30 to P37, P53, P54, P70 to P77, P80 to P87, PA0 to PA7		0.8 Vcc		Vcc + 0.3	v	
	VIHM	MD0 to MD2	$V_{00} = 3.0 \text{ V}$ to 5.5 V	Vcc - 0.3	_	Vcc + 0.3	v	
"L" level input voltage	Vi∟s	P20 to P27, P30 to P37, P53, P54, P70 to P77, P80 to P87, PA0 to PA7	Vcc = 3.0 V to 5.5 V -	V _{ss} – 0.3		0.2 Vcc	v	
	VILM	MD0 to MD2		V _{ss} – 0.3		V _{ss} + 0.3	V	
"H" level output voltage	Vон	All output pins other than P90 to P97	V _{CC} = 4.5 V Іон = -2.0 mA	Vcc – 0.5			v	
"L" level output voltage	Vol	All output pins	$V_{CC} = 4.5 V$ IoL = 2.0 mA			0.4	V	
Input leak current	Iı.	All output pins other than P90 to P97	$\label{eq:Vcc} \begin{split} V_{\text{CC}} &= 5.5 \ V \\ V_{\text{SS}} &< V_{\text{I}} < V_{\text{CC}} \end{split}$	- 5		5	μA	
Open-drain output leak current	lleak	P90 to P97 output pins	_	_	0.1	5	μA	
Pull-up resistor	Rup	P00 to P07, P10 to P17 P40 to P47, MD0, MD1	_	50	100	200	kΩ	
Pull-down resistor	RDOWN	MD2		50	100	200	kΩ	
Demerson			For $V_{cc} = 5 V$,		40	65	mA	MB90522A/ 523A
Current*	Icc	Vcc	= 16 MHz,		30	60	mA	MB90F523B
			normal operation		30	40	mA	MB90522B/ 523B

(Continued)

	Paramotor	Sym-	Din Nama	Condition	Condition			Unit	Pomarka
	Faranneler	bol		Condition	Min	Тур	Max	Unit	nelliaiks
				For Vcc = 5 V,		20	25	mA	MB90522A/ 523A
				internal frequency	—	15	20	mA	MB90F523B
				normal operation		15	20	mA	MB90522B/ 523B
aShee	4U.com			For Vcc = 5 V, internal frequency		50	70	mA	MB90522A/ 523A
				= 16 MHz,	—	45	65	mA	MB90F523B
				A/D operation in progress		35	45	mA	MB90522B/ 523B
				For Vcc = 5 V,		25	30	mA	MB90522A/ 523A
				= 8 MHz,		20	25	mA	MB90F523B
		Icc		A/D operation in progress		20	25	mA	MB90522B/ 523B
				For Vcc = 5 V, internal frequency = 16 MHz, D/A operation in progress		55	70	mA	MB90522A/ 523A
						50	70	mA	MB90F523B
	Power supply		Vcc			40	50	mA	MB90522B/ 523B
	current			For $V_{cc} = 5 V$, internal frequency = 8 MHz,		30	35	mA	MB90522A/ 523A
						25	30	mA	MB90F523B
				D/A operation in progress		20	25	mA	MB90522B/ 523B
				Writing or erasing flash memory		50	75	mA	MB90F523B
				For $V_{CC} = 5 V$, internal frequency		8	15	mA	MB90522A/ 523A
		lees		= 16 MHz, sleep mode		15	20	mA	MB90F523B /522B/523B
		1003		For $V_{CC} = 5 V$, internal frequency		7	10	mA	MB90522A/ 523A
				= 8 MHz, sleep mode		12	18	mA	MB90F523B /522B/523B
		Iccl		For $Vcc = 5 V$, internal frequency = 8 kHz,		0.1	1.0	mA	MB90522A/ 523A/522B/ 523B
				sub-clock mode, Ta = 25 °C		4	7	mA	MB90F523B

(AVcc = Vcc = 5.0 V \pm 10%, AVss = Vss = DVss = 0.0 V, Ta = -40 °C to +85 °C)

(Continued)

(Continued)

(AVcc = Vcc = 5.0 V \pm 10%, AVss = Vss = DVss = 0.0 V, Ta = -40 °C to +85 °C)

Daramatar	Parameter Sym- Pin Name Condition			Value	Unit	Pomarka		
Falameter	bol	FIII Name	Condition	Min	Тур	Max	Onit	nema ka
	Iccls		For $V_{CC} = 5 V$, internal frequency = 8 kHz, sub-sleep mode, Ta = 25 °C		30	50	μΑ	
Power supply current [*]	Ісст	Vcc	For $V_{CC} = 5 V$, internal frequency = 8 kHz, clock mode, Ta = 25 °C	_	15	30	μΑ	
	Іссн		Sleep mode, Ta = 25 °C		5	20	μA	
Input capacitance	Cin	Other than AVcc, AVss, C, Vcc, and Vss	_	_	10	80	pF	
LCD divider resistor	RLCD	V0 – V1, V1 – V2, V2 – V3	_	50	100	200	kΩ	
Output impedance for COM0 to COM3	Rvсом	COM0 to COM3	V1 to V3 – 5.0 V	_		2.5	kΩ	
Output impedance for SEG00 to SEG31	Rvseg	SEG00 to SEG31	V 1 10 V0 - 0.0 V	_		15	kΩ	
LCDC leak current	ILCDC	V0 to V3, COM0 to COM3, SEG00 to SEG31	_	_		±5	μΑ	

* : Current values are provisional and are subject to change without notice to allow for improvements to the characteristics. The power supply current is measured with an external clock.

4. AC Characteristics

(1) Reset and Hardware Standby Input Timings

 $(AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ AV}_{SS} = V_{SS} = DV_{SS} = 0.0 \text{ V}, \text{ Ta} = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C})$

Parameter	Symbol	Pin Condition		Va	lue	Unit	Pomarke
rarameter	Symbol	Name	Condition	Min	Тур	onic	nema ks
Reset input time	t RSTL	RST		4 t _{CP} *	_	ns	
Hardware standby input time	t HSTL	HST		4 t CP [*]	_	ns	

*: See " (3) Clock Timings" for more information about tcp (internal operating clock cycle time) .





(2) Power-On Reset

 $(AVcc = Vcc = 5.0 V \pm 10\%, AVss = Vss = DVss = 0.0 V, Ta = -40 °C to +85 °C)$ Value Pin Condi-Symbol Unit Parameter Remarks Name tion Min Тур Power supply rise time Vcc 30 tR 0.05 ms Power supply cutoff time toff Vcc4 For repeated operation ____ ms

* : Vcc must be less than 0.2 V before power-on.

Notes : • The above rating values are for generating a power-on reset.

- When HST = "L", always apply the power supply in accordance with the above ratings regardless of whether a power-on reset is required.
- Some internal registers are only initialized by a power-on reset. Always apply the power supply in cordance with the above ratings if you wish to initialize these registers.



(3) Clock Timings

1											
	Parameter	Sym-	Pin	Condi-		Value		Unit	Pomarke		
	Falameter	bol	Name	tion	Min	Тур	Max	Unit	nemarks		
	Clock froquency	Fc	X0, X1		3		16	MHz			
	Clock frequency	Fc∟	X0A, X1A			32.768		kHz			
	Clock cyclo timo	t HCYL	X0, X1	—	62.5		333	ns			
	Clock cycle line	t LCYL	X0A, X1A	—	—	30.5	—	μs			
ieei	hout clock pulse width	Р _{wн} Рw∟	X0		10			ns	Recommended duty		
	input clock pulse width	Pwlh Pwll	X0A	—	_	15.2		μs	ratio = 30% to 70%		
	Input clock rise/fall time	tcr tc⊧	X0	—	—		5	ns	When using an external clock		
	Internal operating	fср	—	—	1.5		16	MHz	When using main clock		
	clock frequency	f LCP	—			8.192		kHz	When using sub-clock		
	Internal operating	tсР	—		62.5		666	ns	When using main clock		
	clock cycle time	t LCP				122.1		μs	When using sub-clock		





 $(AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ AV}_{SS} = V_{SS} = DV_{SS} = 0.0 \text{ V}, \text{ Ta} = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C})$



The AC ratings are measured at the following reference voltages.



(4) Clock Output Timings

(AVcc = Vcc = 5.0 V \pm 10%, AVss = Vss = DVss = 0.0 V, Ta = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Va	lue	Unit	Romarke
rarameter	Symbol	Name	Condition	Min	Тур	Onit	nema ko
Cycle time	tcyc	CLK	$V_{00} = 5.0 V + 10\%$	62.5	_	ns	
$CLK \uparrow \to CLK \downarrow$	t cHc∟	OLK	$v_{CC} = 5.0 \ v \pm 10\%$	20		ns	



(5) UART (SCI) Timings

(0) 00000 (000) 0000030	(AV	$V_{\rm CC} = V_{\rm CC} = 5.0$ V	± 10%, AVss = Vss = D	0Vss = 0.0	V, Ta = -	40 °C	to +85 °C)
Paramotor	Sym- bol Pin Name		Condition	Va	lue	Unit	Re-
Falameter			Condition	Min	lin Typ		marks
Serial clock cycle time	t scyc	SCK0 to SCK2		8 t c₽ [*]		ns	
$SCK \downarrow \to SOT$ delay time	tslov	SCK0 to SCK2 SOT0 to SOT2	Internal shift clock	-80	80	ns	
Valid SIN → SCK ↑ 4U.com	tıvsн	SCK0 to SCK2 SIN0 to SIN2	load is $C_{L} = 80 \text{ pF} + 1 \text{ TTL}$	100		ns	
$SCK \uparrow \to valid SIN hold time$	tsнıx	SCK0 to SCK2 SIN0 to SIN2		60		ns	
Serial clock "H" pulse width	tshsl	SCK0 to SCK2		4 t cp*		ns	
Serial clock "L" pulse width	tslsh	SCK0 to SCK2		4 t c₽ [*]		ns	
$SCK \downarrow \to SOT$ delay time	tslov	SCK0 to SCK2 SOT0 to SOT2	External shift clock mode, output pin		150	ns	
Valid SIN \rightarrow SCK \uparrow	tivsh	SCK0 to SCK2 SIN0 to SIN2	$C_L = 80 \text{ pF} + 1 \text{ TTL}$	60		ns	
$SCK^{\uparrow} \to valid \ SIN \ hold \ time$	tshix	SCK0 to SCK2 SIN0 to SIN2		60		ns	

*: See "(3) Clock Timings" for more information about tcp (internal operating clock cycle time).

Notes : • These are the AC ratings for CLK synchronous mode.

• CL is the load capacitor connected to the pin for testing.



(6) Timer Input Timings

$(AVcc = Vcc = 5.0 V \pm 10\%, AVss = Vss = DVss = 0.0 V, Ta = -40 °C to +85 °C)$									
Paramotor	Symbol	Din Namo	Condition	Value		Unit	Pomarka		
Parameter	Symbol	Fill Name	Condition	Min	Тур	Onit	nemarks		
Input pulse width	tтıwн t⊤ıw∟	IC00/01, IC10/11 TI0, TI1		4 tcp*		ns			

* : See " (3) Clock Timings" for more information about tcp (internal operating clock cycle time) .



(7) Timer Output Timings

 $(AVcc = Vcc = 5.0 V \pm 10\%, AVss = Vss = DVss = 0.0 V, Ta = -40 °C to +85 °C)$

Parameter	Parameter Symbol Pin		Pin Name Condition		lue	Unit	Bomarke
Falalletel					Тур	Onit	neillaiks
CLK $\uparrow \rightarrow T_{OUT}$ change time	tто	OUT0 to OUT7 PG00/01 PG10/11 TO0, TO1		30	_	ns	



5. Electrical Characteristics for the A/D Converter

 $(AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ AV}_{SS} = V_{SS} = DV_{SS} = 0.0 \text{ V}, 3.0 \text{ V} \le AVRH - AVRL, Ta = -40 ^{\circ}C \text{ to } +85 ^{\circ}C)$

Deremeter	Sym-	Din Nomo		Value		Unit	Domorko
Parameter	bol	Pin Name	Min	Тур	Max	Unit	Remarks
Resolution				8/10		bit	
Total error	—			—	±5.0	LSB	
Linearity error	—		—		±2.5	LSB	
Differential linearity error	—			—	±1.9	LSB	
Zero transition voltage	Vот	AN0 to AN7	AVss - 3.5 LSB	AVss + 0.5 LSB	AVss + 4.5 LSB	mV	
Full-scale transition voltage	VFST	AN0 to AN7	AVRH - 6.5 LSB	AVRH - 1.5 LSB	AVRH + 1.5 LSB	mV	
A/D conversion time	_		163 tcp			ns	At machine clock = 16 MHz
Compare time	_		99 tcp			ns	At machine clock = 16 MHz
Analog port input current	Iain	AN0 to AN7	—	—	10	μA	
Analog input voltage	VAIN	AN0 to AN7	AVRL	—	AVRH	V	
Poforonoo voltago		AVRH	AVRL + 3.0	—	AVcc	V	
nelelelice voltage		AVRL	0	—	AVRH – 3.0	V	
Power supply current	la	AVcc		5		mA	
	Іан	AVcc		—	5	μA	*
Reference voltage supply	Ir	AVRH		400		μA	
current	Irh	AVRH		—	5	μA	*
Variation between channels		AN0 to AN7	—	—	4	LSB	

* : Current when 8/10-bit A/D converter not used and CPU in stop mode ($V_{CC} = AV_{CC} = AVRH = 5.0 V$)

Note : See "(3) Clock Timings" in "4. AC Ratings" for more information about tcp (internal operating clock cycle time).

6. A/D Converter Glossary

Resolution	:	The change in analog voltage that can be recognized by the A/D converter.
Linearity error	:	The deviation between the actual conversion characteristics and the line linking the zero transition point ("00 0000 0000 _B " $\leftrightarrow \rightarrow$ "00 0000 0001 _B ") and the full scale transition point ("11 1111 1110 _B " $\leftrightarrow \rightarrow$ "11 1111 1111 _B ").
Differential linearity error	:	The variation from the ideal input voltage required to change the output code by 1 LSB.
Total error	:	The total error is the difference between the actual value and the theoretical value. This includes the zero-transition error, full-scale transition error, and linearity error.





7. Notes for A/D Conversion

The recommended external circuit impedance of analog inputs for MB90V520 is approximately 5 k Ω or less, that for MB90F523B is approximately 15.5 k Ω or less, and that for MB90522A/523A/522B/523B is approximately 10 k Ω or less.

If using an external capacitor, the capacitance should be several thousand times the level of the chip's internal capacitor to allow for the partial potential between the external and internal capacitance.

If the impedance of the external circuit is too high, the analog voltage sampling interval may be too short. (for sampling time = 4 μ s, machine clock frequency = 16 MHz).



• Error

The relative error increases as |AVRH - AVRL| becomes smaller.

3. Electrical Characteristics for the D/A Converter $(AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%, \text{ AV}_{SS} = V_{SS} = DV_{SS} = 0.0 \text{ V}, \text{ Ta} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C})$									
Perometer	Symbol	Pin		Value		lloit	Bomorko		
Farameter	Symbol	Name	Min	Тур	Max	Unit	nemarks		
Resolution				8		bit			
Differential linearity error					±0.9	LSB			
Absolute accuracy					±1.2	%			
Linearity error					±1.5	LSB			
40.com Conversion time				10	20	μs	For load capacitance = 20 pF		
Analog reference voltage	—	DVcc	Vss + 3.0		AVcc	V			
Current consumption for	Idvr			120	300	μA			
reference voltage	DVRS				10	μA	Stop mode		
Analog output impedance				20		kΩ			

9. Flash Memory Program/Erase

Parameter	Condition		Value		Linit	Pomarka	
Farameter	Condition	Min	Тур	Max	Unit	neillaiks	
Sector erase time		_	1	15	S	Excludes 00H programming prior erasure	
Chip erase time	Ta = + 25 °C Vcc = 5.0 V	_	5	—	S	Excludes 00H programming prior erasure	
Word (16-bit width) programming time		_	16	3,600	μs	Excludes system-level overhead	
Program/Erase cycle	—	10,000			cycle		
Data hold time		100 K			h		

■ EXAMPLE CHARACTERISTICS

Power supply current (MB90523A)





■ ORDERING INFORMATION

Part No.	Package	Remarks
MB90522APFF MB90523APFF MB90522BPFF MB90F523BPFF	120-pin, Plastic LQFP (FPT-120P-M05)	
MB90522APFV MB90523APFV MB90522BPFV MB90F523BPFV	120-pin, Plastic QFP (FPT-120P-M13)	



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