FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28826-5E

ASSP For Screen Display Control

CMOS

On-screen Display Controller

MB90096

■ DESCRIPTION

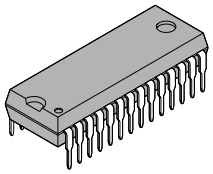
The MB90096 is a multi-scan on-screen display controller that supports horizontal sync signal frequencies of 15 kHz to 120 kHz.The on-screen display configuration is up to 32 characters x 16 lines. The character configuration is up to 24 dots x 32 dots for high resolution, ideal for wide-screen TV, HDTV, and high-resolution personal computer displays.

The character display functions include sprite character, character background display, and graphics functions, contributing to the use of colorful GUI displays.

The MB90096 contains display memory (VRAM), character font ROM, and VCO, allowing characters to be displayed with a minimum of external components. This device also includes command table ROM for storage of display command data, greatly reducing the load on the microcontroller.

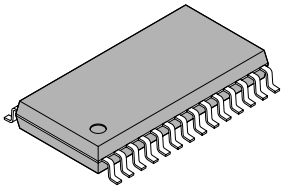
■ PACKAGES

28-pin plastic SH-DIP



(DIP-28P-M03)

28-pin plastic SOP



(FPT-28P-M17)

FUJITSU

■ FEATURES

- Screen display capacity: Up to 32 characters x 16 lines (512 characters)
- Character configuration:

  L size: 24 dots (horizontal) x 2h * dots (vertical)
  M size: 18 dots (horizontal) x 2h * dots (vertical)
  S size: 12 dots (horizontal) x 2h * dots (vertical)
  *: h = 9 to 16

  - L, M, S sizes can be selected by individual character
  - Graphics characters can be displayed in L or S size only
  - Two h values can be set per screen, and either of the two can be selected for each line on the screen.
- Font types: 512 different fonts included (user selectable over entire screen)
- Display modes:

  Normal characters/graphic characters: (set for each character)
  Trimmed display (horizontal trimming/pattern back ground): (set for each screen)
  Character background (fill/shaded background): (set for each character)
  Line background (fill/shaded back ground): (set for each line)
  Enlarged (normal, double width, double height, double width x double height): (set for each line)
  Blinking: Blinking characters: (set for each character)
  Blink period, duty ratio: (set for each screen)
- Sprite character display (graphics display only):

  Capable of displaying one block of characters (maximum 2 x 2 characters) on main screen.
  (Can move horizontally and vertically in 2-dot increments.)
  Setting applies to the first 256 characters only (character codes 000 to 0FFH).
- Background character display (graphics display only):

  Capable of displaying a repeated pattern (2 x 2 characters) on main screen.
  Setting applies to the first 256 characters only (character codes 000 to 0FFH).
- Display colors: Character/background colors: 16 colors each (set for each character)
  Line background/fill colors: 16 characters each (set for each line)
  Screen background colors: 16 colors (set for each screen)
  Graphics character dot colors: 16 colors (set for each dot)
  Shading background frame colors (highlight/shadow):
  16 colors each (set for each screen)
- Display position control:

  Horizontal display start position: Set in 4-dot units (for each screen)
  Vertical display start position: Set in 4-dot units (for each screen)
  Line spacing control: Set in 2-dot units (for each line)
- Character/color signal output:

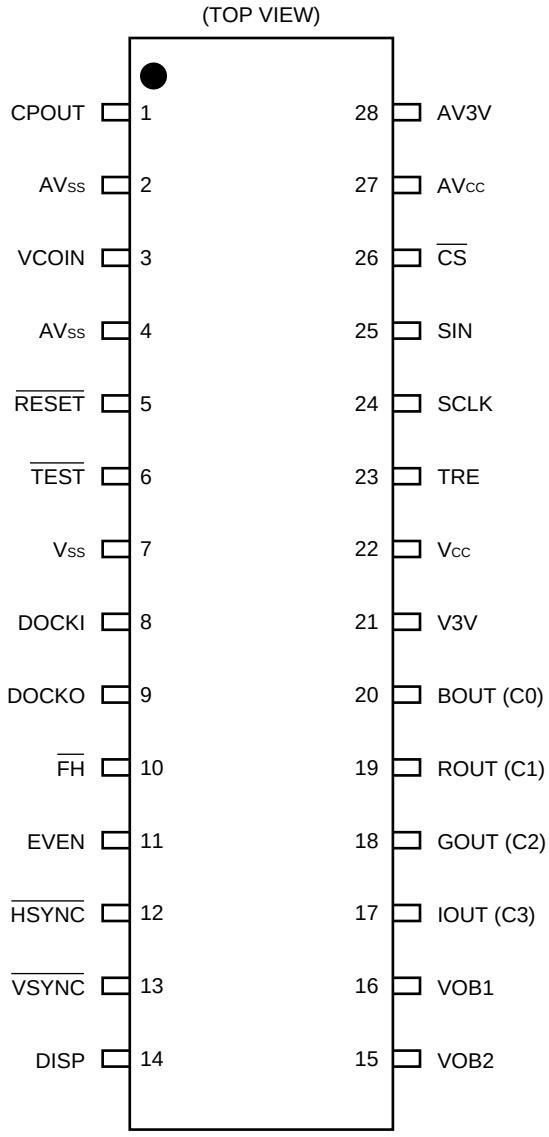
  ROUT, GOUT, BOUT, IOUT (color signals)
  VOB1 (OSD display period output signal)
  VOB2 (semi-transparent color period output signal)
- Command transfer function (macro service):

  Command table ROM, 16Kbyte included
- Compatible horizontal sync signal frequencies:

  15 kHz to 120 kHz (PLL circuit included)
- Microcontroller interface:

  16-bit serial input (3 signal input pins)
- Packages: SH-DIP-28, SOP-28
- Power supply voltage: +5 V

■ PIN ASSIGNMENTS



(DIP-28P-M03)
(FPT-28P-M17)

■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O	Circuit type	Function
1	CPOUT	O	A	Horizontal sync phase comparison result signal output pin. Connects to external low-pass filter.
3	VCOIN	I	B	Internal VCO voltage input pin. Receives voltage signal input from external low-pass filter
8	DOCKI	I	D	Dot clock input pin. Used only when operating on an externally generated dot clock signal. *1 When unused, the horizontal sync signal *2 should be input at this pin. Internal pull-up resistance included.
9	DOCKO	O	C	Output pin for the dot clock signal generated by the internal VCO. This signal can be fixed at “H” level by a command.
10	$\overline{FH}$	O	C	Output pin for the horizontal sync signal generated by the PLL circuit.
11	EVEN	I	D	Field control signal input pin. This pin is disabled when noninterlaced display or internally generated field control signals are selected by command. Internal pull-up resistance included.
12	$\overline{HSYNC}$	I	D	Horizontal sync signal input pin. The period of this signal is used to generate the dot clock signal. The active level is programmable. Internal pull-up resistance included.
13	$\overline{VSYNC}$	I	D	Vertical sync signal input pin. The active level is programmable. Internal pull-up resistance included.
14	DISP	I	D	Display output (ROUT, GOUT, BOUT, IOUT, VOB1, VOB2) control pin. When this pin is set to “L” level, the display control is forcibly set to inactive. Normally, the horizontal and vertical blanking signals are input here. *3 Internal pull-up resistance included.
17 18 19 20	IOUT (C3) GOUT (C2) ROUT (C1) BOUT (C0)	O	C	Color signal output pins. The active level is programmable.
16	VOB1	O	C	Display period output pin. The active level is programmable.
15	VOB2	O	C	Semi-transparent period output signal. The active level is programmable.
24	SCLK	I	D	Serial transfer shift clock input pin. Internal pull-up resistance included.
25	SIN	I	D	Serial data input pin. Internal pull-up resistance included.
26	$\overline{CS}$	I	D	Chip select pin. Set to “L” level for serial transfer. Internal pull-up resistance included.

(Continued)

(Continued)

Pin no.	Pin name	I/O	Circuit type	Function
23	TRE	O	C	Output pin for indicator that command transfer and fill operations are in progress. Active “H” level output.
5	$\overline{\text{RESET}}$	I	D	Reset input pin. Input a “L” level signal *4 at power-on. Internal pull-up resistance included.
6	$\overline{\text{TEST}}$	I	D	Test signal input pin. Input “H” level (fixed) for normal operation. Internal pull-up resistance included.
22	V_{CC}	—	—	+5 V power supply pin.
21	V3V	—	—	Connect 0.1 μF capacitance between this pin and V_{SS}.
7	V_{SS}	—	—	Ground pin.
27	AV_{CC}	—	—	+5 V power supply pin for VCO.
28	AV3V	—	—	Connect 0.1 μF capacitance between this pin and AV_{SS}.
2, 4	AV_{SS}	—	—	Ground pin for VCO.

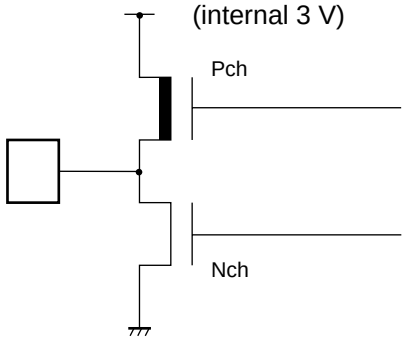
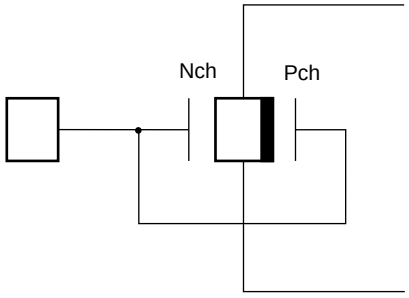
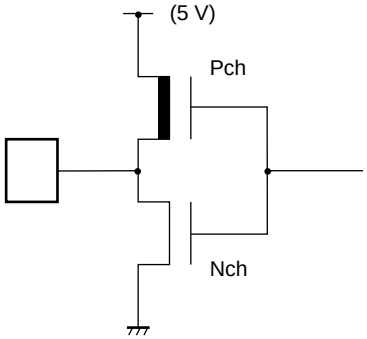
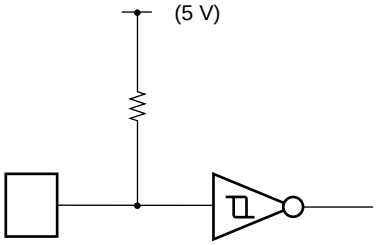
*1: The clock signal should be input even during a reset interval.

*2: The active level of the horizontal sync signal input may be either “H” or “L” level. During reset intervals, including power-on resets, apply a “L” level fixed signal or a horizontal sync signal with one or more “L” level intervals at the DOCKI pin.

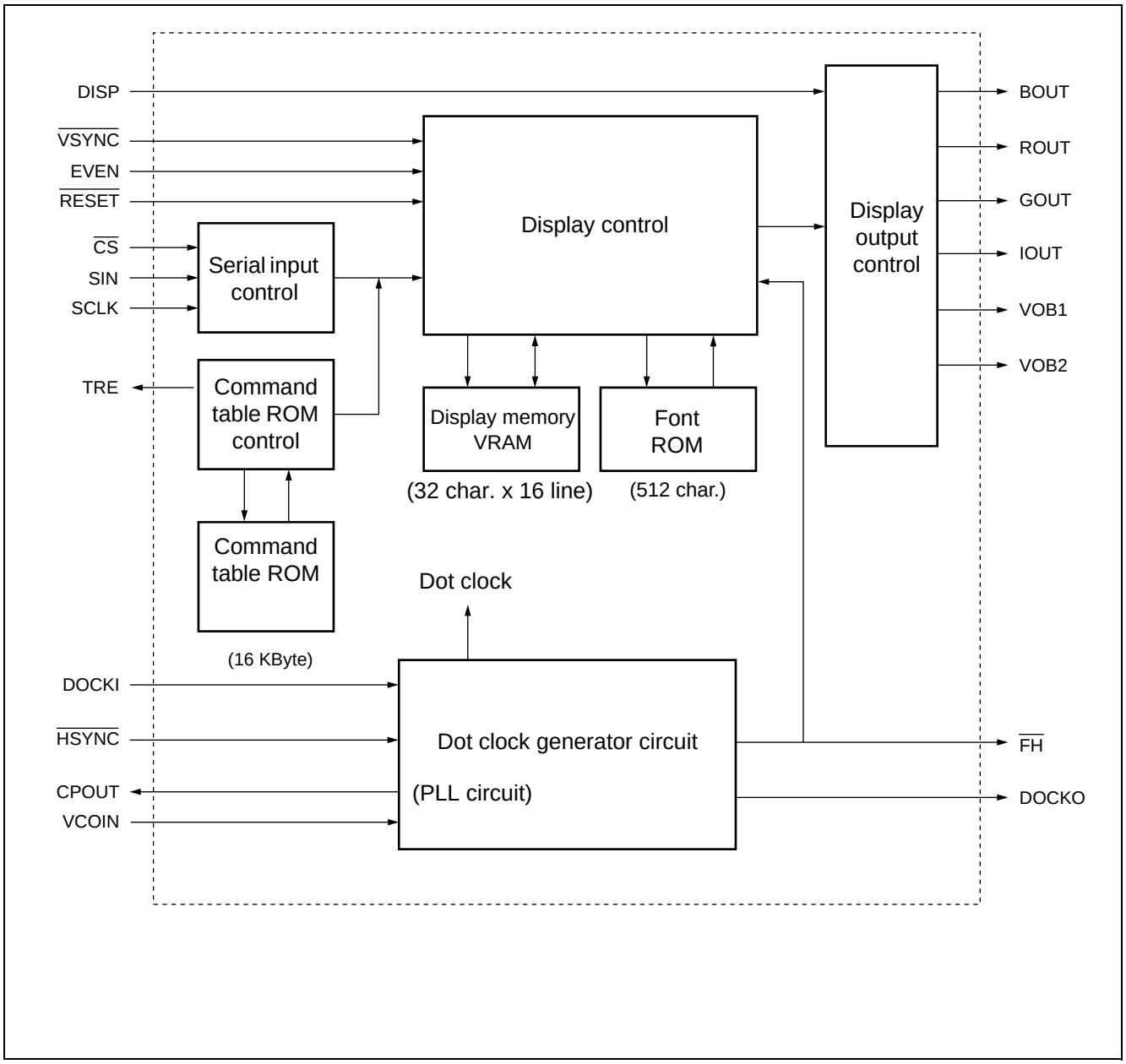
*3: The MB90096 display signals (IOUT, ROUT, GOUT, BOUT, VOB1, VOB2) may be output during horizontal or vertical blanking intervals. Normally devices such as TV or monitors use a reverence color setting during horizontal and vertical blanking intervals, so that during this period the MB90096 display signals must be masked at the DISP pin signal.

*4: When power is switched on, apply a “L” level signal for 1ms or longer after the V_{CC} (AV_{CC}) is stabilized.

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		• CMOS output (internal 3 V) 3-state output
B		• Analog input
C		• CMOS output (5 V)
D		• CMOS hysteresis input Pull-up resistance (approx. 50 kΩ) included

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0 V Typ)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	*
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	*
Capacitance pins	V3V, AV3V	V_{SS} – 0.3	V_{SS} + 3.6	V	
Input voltage	V_{IN}	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_{OUT}	V_{SS} – 0.3	V_{CC} + 0.3	V	
Power consumption	Pd	—	600	mW	
Operating temperature	Ta	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*: AVcc and Vcc must have equal potential.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0 V Typ)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.5	5.5	V	Specification guarantee range
	AV_{CC}	4.5	5.5	V	*1
“H” level input voltage	V_{IHS}	0.8 × V_{CC}	V_{CC} + 0.3	V	
“L” level input voltage	V_{ILS2}	V_{SS} – 0.3	0.2 × V_{CC}	V	
Operating temperature	Ta	–40	+85	°C	
Analog input voltage	V_{IN}	0	3.0	V	VCOIN input *2
Smoothing capacitor (capacitance pin)	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor having equivalent frequency characteristics. The capacitance at the Vcc and AVcc pins must be greater than Cs.

*1: AVcc and Vcc must have equal potential.

*2: This recommended input voltage range does not imply that stable PLL operation is warranted. For stable PLL operation it is recommended that input voltage be between 1.0 V and 2.5 V. Note however that PLL operating status is greatly affected by variations in the input horizontal sync signal period, as well as external filter settings and operating temperature, etc. Thorough testing and evaluation is recommended.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{SS} = AV_{SS} = 0 V, Ta = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
"H" level output voltage 1	V_{OH1}	All output pins except CPOUT pin	V_{CC} = AV_{CC} = 4.5 V, I_{OH} = –4.0 mA	4.0	—	—	V
"H" level output voltage 2	V_{OH2}	CPOUT pin	V_{CC} = AV_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.5	—	—	V
"L" level output voltage	V_{OL}	All output pins	V_{CC} = AV_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V
Pull-up resistance	R_{PULL}	All input pins except VCOIN pin	V_{CC} = AV_{CC} = 5.5 V	20	—	100	kΩ
Input leak current	I_{IL}	VCOIN pin	V_{CC} = AV_{CC} = 5.5 V, V_{SS} < V_{IL} < V_{CC}	–10	—	10	µA
Power supply current	I_{CC}	V_{CC} + AV_{CC}	V_{CC} = AV_{CC} = 5.5 V (no load), Dot clock 60 MHz	—	—	40	mA
			Dot clock 40 MHz	—	—	30	mA
			Dot clock 20 MHz	—	—	20	mA
Input capacitance	C_{IN}	Other than power supply and capacitance pins *	—	—	10	—	pF

*: Power supply pins: V_{CC}, AV_{CC}, V_{SS}, AV_{SS}, Capacitance pins: V3V, AV3V

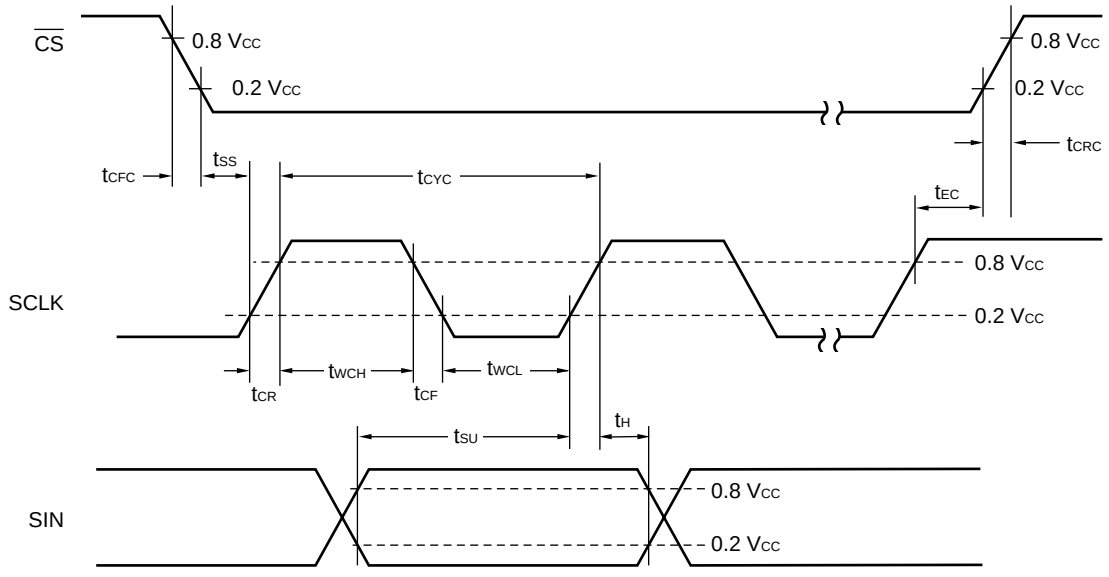
2. AC Characteristics

(1) Serial Input Timing

(V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Shift clock cycle time	t_{CYC}	SCLK	250	—	ns	
Shift clock pulse width	t_{WCH}	SCLK	100	—	ns	
	t_{WCL}		100	—	ns	
Shift clock signal rise/fall time	t_{CR}	SCLK	—	200	ns	
	t_{CF}		—	200	ns	
Shift clock start time	t_{SS}	SCLK	100	—	ns	
Data setup time	t_{SU}	SIN	100	—	ns	
Data hold time	t_H	SIN	50	—	ns	
Chip select end time	t_{EC}	$\overline{CS}$	100	—	ns	
Chip select signal rise/fall time	t_{CRC}	$\overline{CS}$	—	200	ns	
	t_{CFC}		—	200	ns	

• **Serial input timing**



(2) Vertical and horizontal sync signal input timing

(V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to +85 °C)

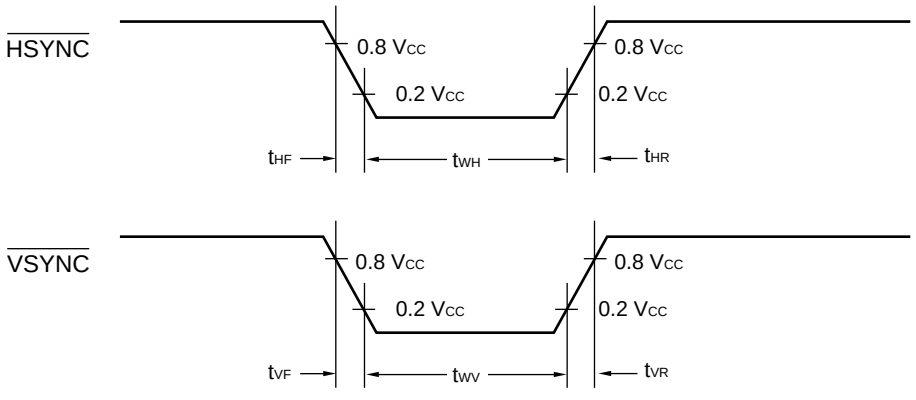
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Horizontal sync signal rise time	t_{HR}	$\overline{HSYNC}$	—	500	ns	
Horizontal sync signal fall time	t_{HF}		—	500	ns	
Vertical sync signal rise time	t_{VR}	$\overline{VSYNC}$	—	500	ns	
Vertical sync signal fall time	t_{VF}		—	500	ns	
Horizontal sync signal pulse width *1	t_{WH}	$\overline{HSYNC}$	18	—	Dot clock	
			—	6	µs	
Vertical sync signal pulse width	t_{WV}	$\overline{VSYNC}$	2	20	H	
Horizontal sync signal setup time	t_{DHST}	$\overline{HSYNC}$	6	—	ns	*2
Horizontal sync signal hold time	t_{DHHD}		3	—	ns	*2
Vertical sync signal setup time	t_{HVST}	$\overline{VSYNC}$	4	1H – 4	Dot clock	
Vertical sync signal hold time	t_{HVHD}		2	20	H	
Vertical sync signal setup time when field signal is generated	t_{EVST}	$\overline{VSYNC}$	18	—	Dot clock	*3
Vertical sync signal hold time when field signal is generated	t_{EVHD}	$\overline{VSYNC}$	18	—	Dot clock	*3

*1: The horizontal sync pulse time is applied after MB90096 internal operations have paused and horizontal operation has been synchronized. For this reason it is necessary to leave an interval between commands so that writing to VRAM (command 2, 4) is not performed more than once.
It is necessary to set the horizontal sync signal pulse width and interval for writing to VRAM so that the horizontal sync signal pulse width is less than the writing interval to VRAM.

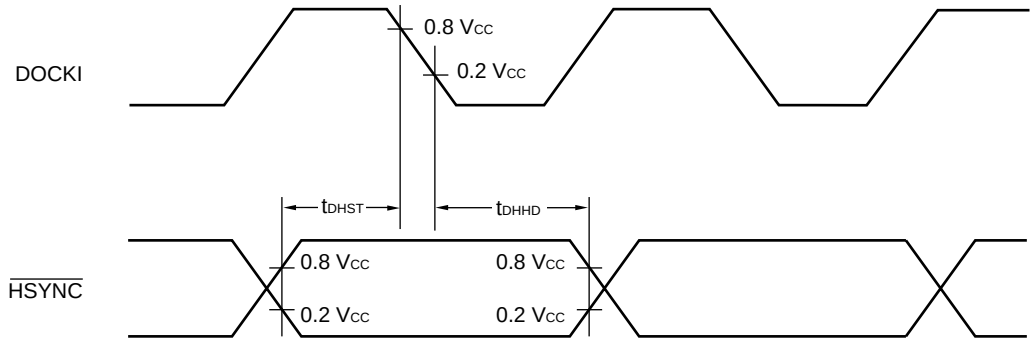
*2: Applied when an external dot clock signal is input.

*3: Applied in interlaced display, when the EVEN signal is applied from an external source.

● **Vertical and horizontal sync signal input timing**

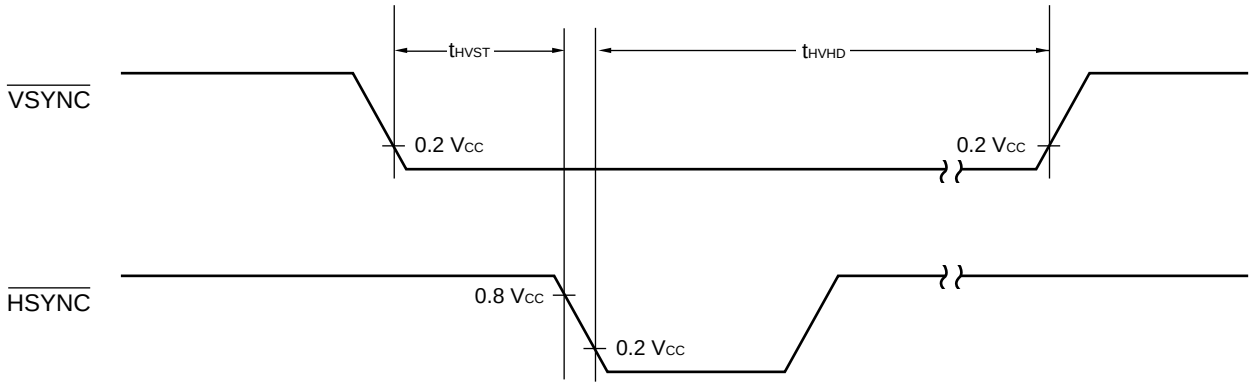


• **Horizontal sync signal setup and hold timing**



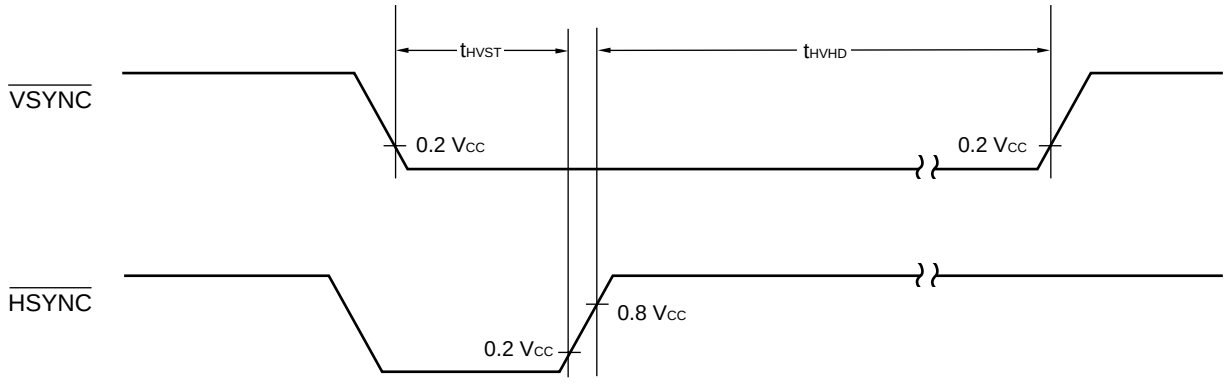
• **Vertical sync signal setup and hold timing**

$\overline{\text{HSYNC}}$: VSYNC detection at front edge (VHE = 0)



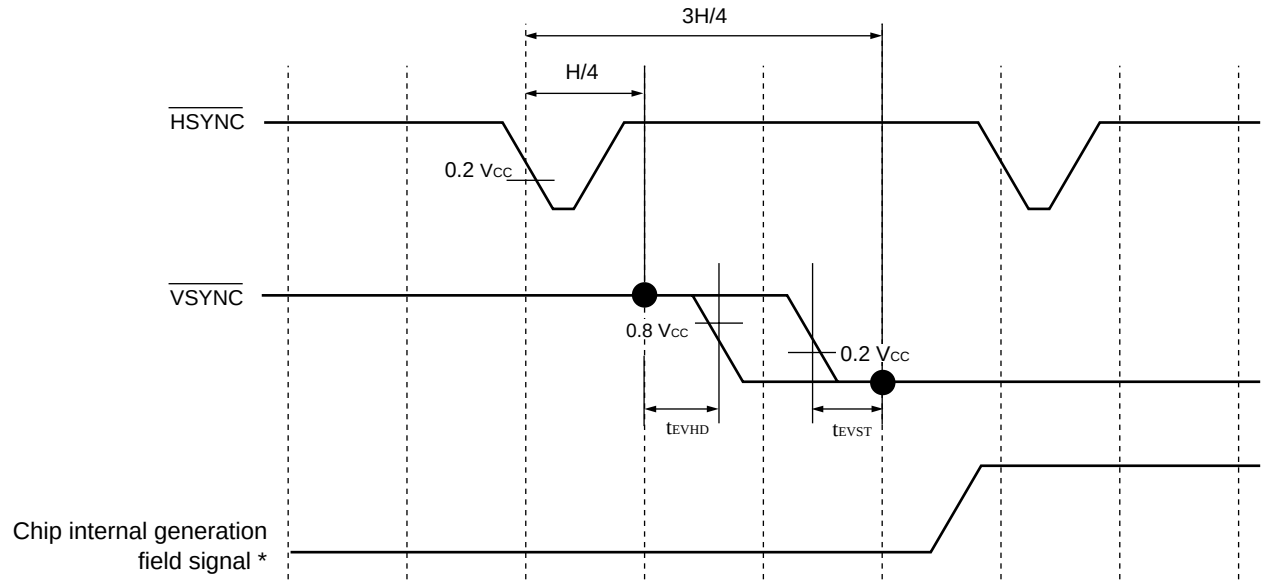
• **Vertical sync signal setup and hold timing**

$\overline{\text{HSYNC}}$: VSYNC detection at back edge (VHE = 1)



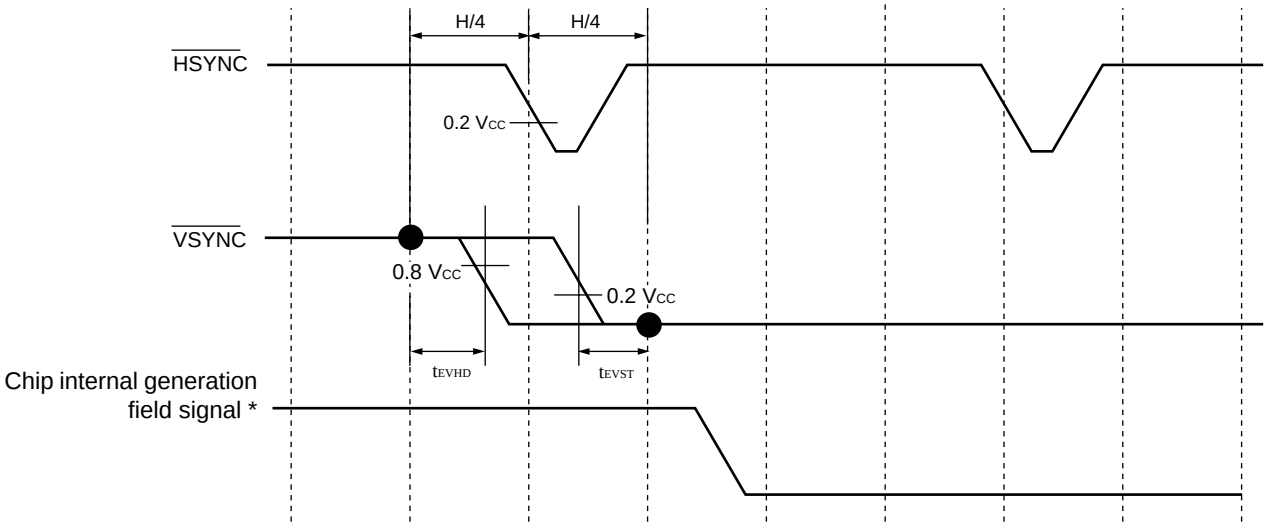
● **EVEN signal generation timing**

Detection of EVEN = 1
(Valid with settings for internal field signal generation [FLD = 0], and dot clock internal generation [DCO = 0].)



● **EVEN signal generation timing**

Detection of EVEN = 0
(Valid with settings for internal field signal generation [FLD = 0], and dot clock internal generation [DCO = 0].)

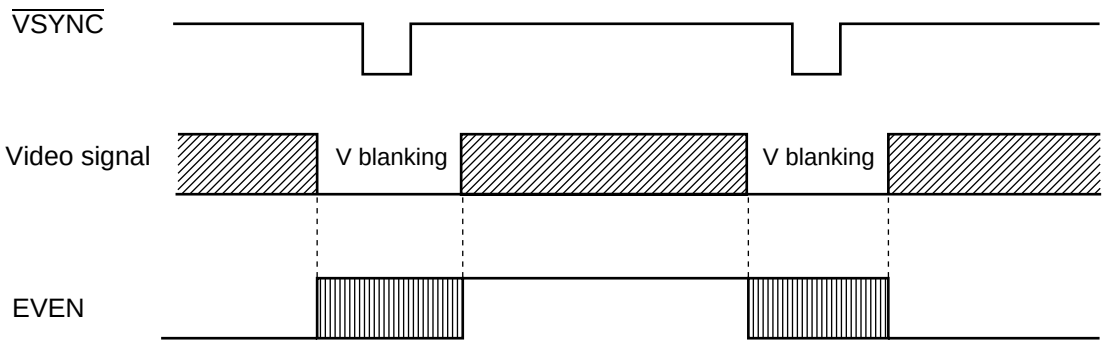


*: Sample of internal generation without field signal correction (command 11-0 FC = 0)

Note: In a normal NTSC signal, H/4 = 63.5 µs / 4 ≒ 15.9 µs, 3H/4 ≒ 47.6 µs.

• **EVEN signal input timing**

(Valid with settings for external field signal input [FLD = 1].)



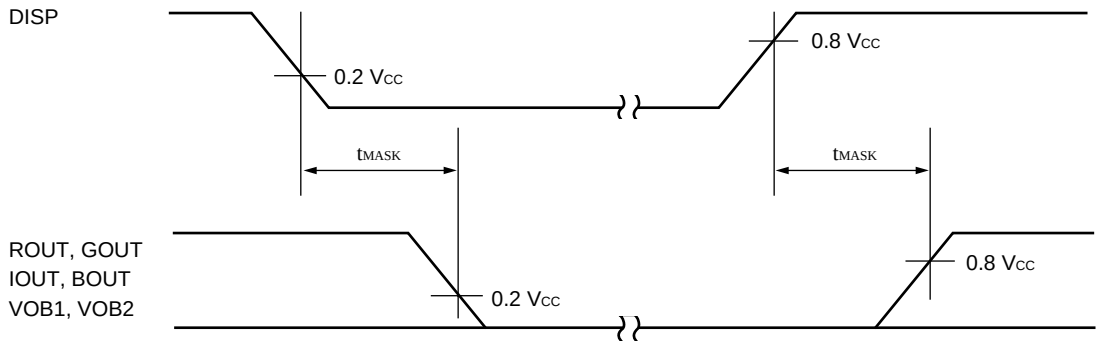
Note: There is no numerical standard for EVEN signal input timing.
Set so that the signal changes during the V blanking interval when no video signal is output.

(3) Display signal timing

(V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Dot clock input frequency	f_{DCK}	DOCKI	7	60	MHz	
Dot clock input cycle time	t_{DCK}	DOCKI	16.7	142.8	ns	
Dot clock input pulse width	t_{DIWH}	DOCKI	7	—	ns	
	t_{DIWL}		7	—	ns	
Display signal output mask timing	t_{MASK}	ROUT, GOUT, BOUT, IOUT, VOB1, VOB2	5	30	ns	
Dot clock output delay	t_{DLIO}	DOCKO	12	24	ns	
Display signal output delay 1	t_{RGB1}	ROUT, GOUT, BOUT, IOUT, VOB1, VOB2	21	33	ns	
Display signal output hold time 1	t_{RGB1HD}		t_{RGB1} – 11		ns	
Display signal output delay 2	t_{RGB2}	ROUT, GOUT, BOUT, IOUT, VOB1, VOB2	—	9	ns	
Display signal output hold time 2	t_{RGB2HD}		– 2	—	ns	
$\overline{FH}$ output delay	t_{DLFH}	$\overline{FH}$	–5	5	ns	

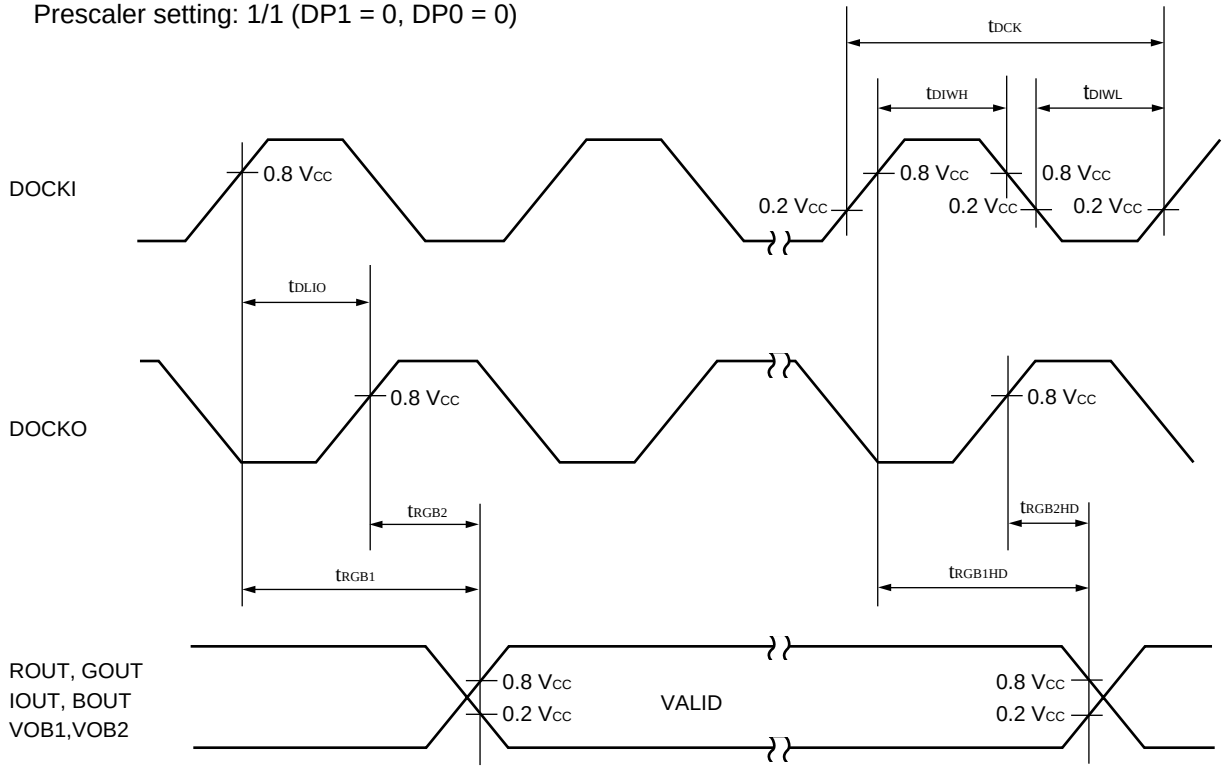
- **Display signal output mask timing**



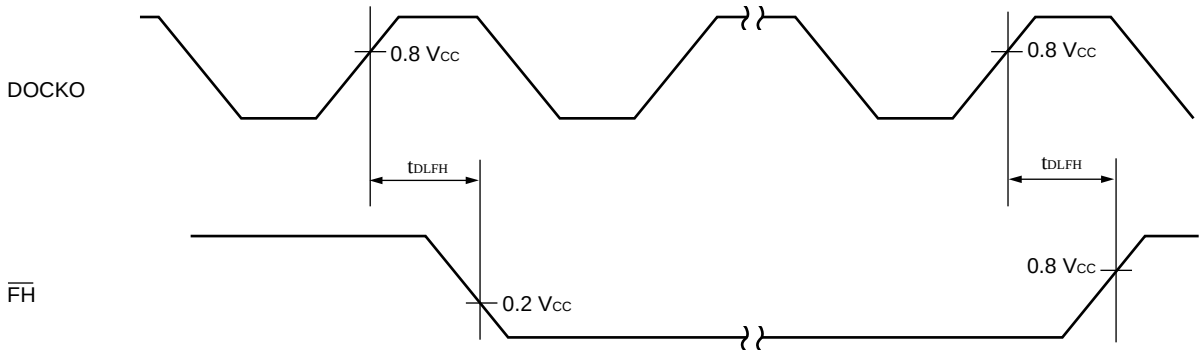
Note: • Display related output logic is written in normal logic settings [command 13-0: DHX = DBX = DCX = 0].
• Sync signal input logic is written in inverse logic settings [command 13-0: SIX = 0].

• **Display signal output delay**

Prescaler setting: 1/1 (DP1 = 0, DP0 = 0)



• **$\overline{\text{FH}}$ output delay**



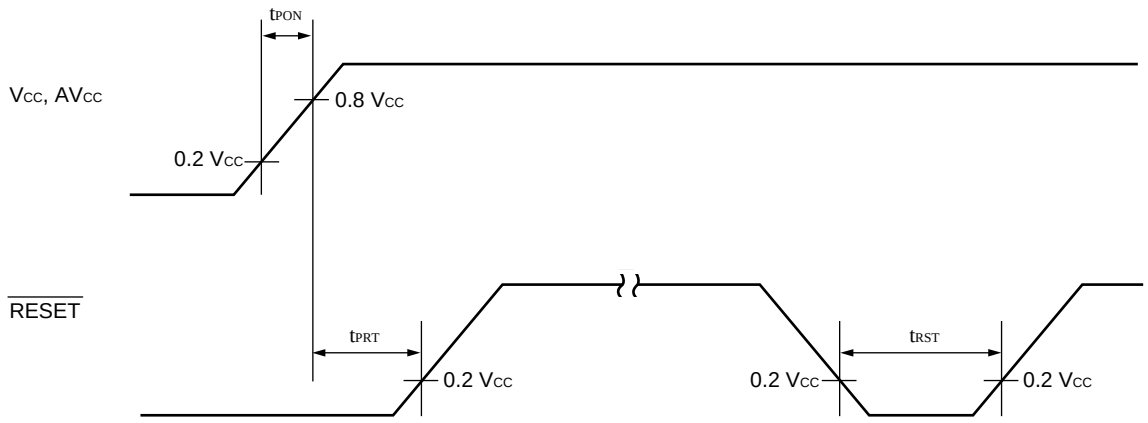
(4) Power supply input, reset input timing

(V_{CC} = AV_{CC} = 5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Vlaue		Unit	Remarks
			Min	Max		
Power supply rise time	t_{PON}	V_{CC}, AV_{CC}	100	—	µs	*
Reset input at power on	t_{PRT}	$\overline{RESET}$	1	—	ms	
Reset input with power stabilized	t_{RST}	$\overline{RESET}$	10	—	µs	

*: Ensure that the slope of the power supply rise (ΔV/Δt) does not exceed 0.05 V/µs.

● **Power-on and reset input timing**



AC rating measurement conditions
C = 28 pF
t_r = 5 ns
t_f = 5 ns
V_{OH} = 0.8 V_{CC}
V_{OL} = 0.2 V_{CC}
V_{IH} = 0.8 V_{CC}
V_{IL} = 0.2 V_{CC}

■ COMMAND LIST

1. Command List

Command no.	Function	Command code/data												
		15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
0	Set VRAM write address	0000	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0
1	Character data 1	0001	MS1	MS0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0
2	Character data 2	0010	MR	MG	MBL	M8	M7	M6	M5	M4	M3	M2	M1	M0
3	Line control data 1	0011	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0
4	Line control data 2	0100	LDS	0	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0
5-0	Screen output control 1	0101	0	0	0	0	SDS	UDS	PDS	DSP	0	0	0	0
5-1	Screen output control 2	0101	0	1	FM1	FM0	BT1	BT0	BD1	BD0	0	0	0	0
5-2	Vertical display position control	0101	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
5-3	Horizontal display position control	0101	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0
6-0	Character vertical size control	0110	0	0	0	0	0	HB2	HB1	HB0	0	HA2	HA1	HA0
6-1	Shading background frame color control	0110	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0
6-2	Transparent / semi-transparent color control	0110	1	0	TC	HC	TC3	TC2	TC1	TC0	HC3	HC2	HC1	HC0
6-3	Graphic color control	0110	1	1	GF	GC	GF3	GF2	GF1	GF0	GC3	GC2	GC1	GC0
7-1	Screen background character control 1	0111	0	1	1	1	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
7-3	Screen background character control 2	0111	1	1	1	0	0	PH2	PH1	PH0	U3	U2	U1	U0
8-1	Sprite character control 1	1000	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0
8-2	Sprite character control 2	1000	1	0	1	SBL	0	SH2	SH1	SH0	0	0	0	0
9-0	Sprite character control 3	1001	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0
9-1	Sprite character control 4	1001	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0
11-0	Sync control	1011	0	0	0	0	EG1	EG0	0	FC0	FLD	0	0	0
11-2	Dot clock control 1	1011	1	0	DO	0	0	0	DP1	DP0	0	0	0	DC0
11-3	Dot clock control 2	1011	1	1	DK9	DK8	DK7	DK6	DK5	DK4	DK3	DK2	DK1	DK0
13-0	I/O pin control	1101	0	0	0	VHE	0	0	SIX	0	0	DHX	DBX	DCX
14-0	CROM transfer start address 1	1110	0	0	0	0	0	0	TSD	TSC	TSB	TSA	TS9	TS8
14-1	CROM transfer start address 2	1110	0	0	1	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	0
14-2	CROM transfer end address 1	1110	0	1	0	0	0	0	TED	TEC	TEB	TEA	TE9	TE8
14-3	CROM transfer end address 2	1110	0	1	1	TSV	TE7	TE6	TE5	TE4	TE3	TE2	TE1	1

(Continued)

(Continued)

Notes: • Initial values are undefined for the VRAM and line VRAM settings in commands 0, 1, 2, 3, and 4. Therefore all VRAM and line VRAM values must be initialized by issuing commands. (FIL functions are valid for all VRAM initializations.)
• The initial value for command 5-0 and command 13-0 is "0" for all bits. However, to protect against abnormal operation due to causes such as external noise, initial settings should be made to all commands *.

*: Initial settings should be made for all commands other than the command ROM transfer commands (command 14-0 through 14-3). Note that initial settings for command 0 through command 9-1 may be stored in command ROM, and initialized by command ROM transfer.

2. Command content

• Command 0 (Set VRAM write address)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0

AY3-AY0 : Line address (0 to F_H)

AX4-AX0 : Column address (0 to $1F_H$)
FL : VRAM file setting (0 : OFF, 1 : ON)

[Functions]

Command 0 specifies the write address in VRAM memory.

This command is used to specify the line and column address before using commands 1 and 2 to set character data, and to specify the line address before using commands 3 and 4 to set line control data.

[Description]

- Normal writing (writing in units of 1 character data or 1 line control data) is done with the VRAM fill setting OFF (FL = 0).
- After executing command 2, the VRAM address is incremented automatically. (At the end of a column, the address is incremented to the head of the next column, and at the end of the last line the address is incremented to the head of the next page.)
- If the VRAM fill setting (FL=1) is used, the same character data (specified by commands 1, 2) is written to all addresses from the line and column address specified by command 0 to the end of the page. VRAM fill is executed by the set character data 2 command (command 2). When this command is executing, the TRE pin output is at "H" level.

Notes: • When command 3 and 4 settings (line control data) are in effect, the column address values in this command (AX4-AX0) are ignored.
• VRAM addresses are not incremented automatically by executing commands 3 and 4 (line control data).
• VRAM fill settings are valid only for commands 1 and 2 (character data).
• When VRAM fill is executing, commands 1-4 may not be issued.

• **Command 1 (Character data 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	MS1	MS0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0

MC3-MC0: Character color (16 colors)
MB3-MB0: Character background color (16 colors)
MM1, MM0: Character background control
(0, 0 : OFF)
(0, 1 : Fill in)
(1, 0 : Shaded concave)
(1, 1 : Shaded convex)

MS1, MS0: Character horizontal size control
0, 0: 12-dot
0, 1: 18-dot
1, 0: 24-dot
1, 1: (prohibited)

[Function]

Command 1 sets character data. This data is written in VRAM and displayed on the screen by executing the character data 2 command (command 2).

[Description]

- The character color, background color, character background type, and horizontal size can be set in any combination, for each character separately.
- Shading can be oriented towards, top, bottom, right, or left using a combination of the MR bit in command 2 and the LD and LE bits in command 4.
- Shading background frame color settings are made using command 6-1.

Note: These settings are not available for M size graphics characters.

• **Command 2 (Character data 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	MR	MG	MBL	M8	M7	M6	M5	M4	M3	M2	M1	M0

MR: Shaded background right-character fusion control
(0: No fusion with right-character)
(1: Fusion with right-character)
M8-M0: Character code

MG: Character/graphics character control
(0: character, 1: graphics character)
MBL: Blinking control (0: OFF, 1: ON)

[Function]

Command 2 writes the character data set by the character data 1 command (command 1) as well as the data contained in this command to the VRAM address specified by the VRAM write address command (command 0).

After command 2 is executed, the VRAM write address is automatically incremented.

[Description]

- The blinking control setting (MBL=1) causes the display to blink according to the settings of the BT1, BT0, BD1, BD0 bits in command 5-1.
- The shaded background right-character fusion control bit (MR) is used only with characters having the shading setting specified in command 1 (MM1=1).

Notes: • Because all VRAM settings are undefined after a reset, it is necessary to enter all VRAM settings before executing a display.
•These settings are not available for M size graphics characters.

• **Command 3 (Line control data 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0

LHS: Line character vertical size type
(0: Character vertical size A)
(1: Character vertical size B)
LW2-LW0: Line spacing control
(0-14 dots, in 2-dot increments)
LF3-LF0: Trimming color (16 colors)

LFD, LFC: Trimming output control
(0,0: All OFF)
(0,1: Trimming ON for characters without background only)
(1,0: Trimming ON for characters without background and filled characters only)
(1,1: Trimming output ON)
LFB, LFA: Trimming control
(0,0: Trimming OFF)
(0,1: Right trimming)
(1,0: Left trimming)
(1,1: Left and right trimming)

[Function]

Command 3 sets line control data. This data is written in VRAM and reflected on the screen display when the line data 2 command (command 4) is executed.

[Description]

- Command 6-0 (Character vertical size control) determines the specification of the actual size of the characters controlled by the line character vertical size type setting (LHS).
- The trimming format is specified by the FM1, FM0 bits in command 5-1 (Trimming format control).

• **Command 4 (Line control data 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	LDS	0	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0

LDS: Line character output control
(0: OFF, 1: ON)
LG1, LG0: Line expansion control
(0:,0: Normal)
(0,1: Double width)
(1,0: Double height)
(1,1: Double height and width)

LE: Character background expansion control
(0: Normal, 1: Expanded)
LD: Shaded background lower side fusion control
(0: Not fused, 1: Lower side fused)
LM1, LM0: Line background control
(0,0: OFF)
(0,1: Fill display)
(1,0: Shaded concave display)
(1,1: Shaded convex display)
L3-L0: Line background color (16 colors)

[Function]

Command 4 writes the line control data set by the line control data 1 command (command 3) as well as the data contained in this command to the VRAM address specified by the VRAM write address command (command 0).

Notes:
- Because all VRAM settings are undefined after a reset, it is necessary to enter all VRAM settings before executing a display.
- Executing this command does not cause automatic incrementing of the VRAM write address. The address must be set by command 0 for each line for which this command is executed.

• **Command 5-0 (Screen output control 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0	SDS	UDS	PDS	DSP	0	0	0	0

SDS: Sprite character output control
(0: OFF, 1: ON)
UDS: Screen background output control
(0: OFF, 1: ON)

PDS: Screen background character output control
(0: OFF, 1: ON)
DSP: Display output control
(Character + trimming + character background + line background control)
(0: OFF, 1: ON)

[Function]

Command 5-0 controls screen display output.

Note: When the display is turned ON by turning the SDS, PDS, UDS, DSP bits ON, starting from a state in which at least one of those bits is already ON, it may happen that the display screen (characters) appear displaced vertically by the amount of the initial field in the setting.

• **Command 5-1 (Screen output control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	FM1	FM0	BT1	BT0	BD1	BD0	0	0	0	0

BT1, BT0: Blinking period control
(0,0: 16 V)
(0,1: 32 V)
(1,0: 48 V)
(1,1: 64 V)

BD1, BD0: Blinking duty control
(0,0: On:off = 1:0 (always on))
(0,1: On:off = 1:1)
(1,0: On:off = 1:3)
(1,1: On:off = 3:1)

FM1, FM0: Trimming format control
(0,0: Horizontal trimming 1 dot)
(0,1: Horizontal trimming 2 dots)
(1,0: Pattern background 1)
(1,1: Pattern background 2)

[Function]

Command 5-1 controls screen display output.

[Description]

The blinking control bits of this command are applied to characters for which blinking control is specified (MBL=1) in command 2, as well as sprite characters for which blinking control is specified (SBL=1) in command 8-2.

• **Command 5-2 (Vertical display position control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Y8-Y0: Vertical display position control
(0-2044, in 4-dot units)

[Function]

Command 5-2 controls the vertical display position on the screen.

• **Command 5-3 (Horizontal display position control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0

X8-X0: Horizontal display position control
(0-2044, in 4-dot units)

[Function]

Command 5-3 controls the horizontal display position on the screen.

• Command 6-0 (Character vertical size control)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	HB2	HB1	HB0	0	HA2	HA1	HA0

HB2-HB0: Character vertical size control B (18-32 dots, in 2-dot units)
HA2-HA0: Character vertical size control A (18-32 dots, in 2-dot units)

[Function]

Command 6-0 controls the vertical size of character types A and B.

[Description]

This command specifies the actual values of the vertical size settings (LHS=0: Size A, LHS=1: Size B) for individual lines in command 3.

• Command 6-1 (Shading background frame color)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0

BH2-BH0: Shaded background frame highlight color (16 colors)
BS2-BS0: Shaded background frame shadow color (16 colors)

[Function]

Command 6-1 controls the frame color of the shading background.

[Description]

- This command sets the frame color for characters for which shaded character background is specified in command 1 (MM1=1), as well as shading background for lines for which shaded line background is specified in command 4 (LM1=1).
- The highlight color indicates the color of the left and top edges of the character area when convex shaded character background is selected, or the color of the top edge of the line area when convex shaded line background is selected.
- The shadow color indicates the color of the right and bottom sides of the character area when convex shaded character background is selected, or the color of the bottom edge of the line area when convex shaded line background is selected.
- When concave shaded character background or concave shaded line background is selected, the highlight and shadow colors are the reverse of those selected for convex display.

• **Command 6-2 (Transparent / semi-transparent color control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	0	TC	HC	TC3	TC2	TC1	TC0	HC3	HC2	HC1	HC0

TC: Transparent color control (0: OFF, 1: ON) TC3-TC0: Transparent color code (16 colors)
HC: Semi-transparent color control (0: OFF, 1: ON) HC3-HC0: Semi-transparent color code (16 colors)

[Function]

Command 6-2 controls the transparent and semi-transparent color settings.

[Description]

- The setting TC=1 causes areas of the designated transparent color (TC3-TC0) to be excluded (so that the color behind those areas shows through).
- The setting HC=1 causes areas of the designated semi-transparent color (HC3-HC0) to be excluded at the same time a semi-transparent interval signal output from the VOB2 pin, so that the signal can be used by external circuits to reduce brightness, etc.

Notes:
- If both the transparent and semi-transparent settings are selected at the same time, they should be set for different colors.
- The semi-transparent interval signal output from the VOB2 pin is applied to areas other than the main screen character, trimming, and graphics areas.

• **Command 6-3 (Graphic color control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	1	GF	GC	GF3	GF2	GF1	GF0	GC3	GC2	GC1	GC0

GF: Graphic color trimming color replacement control (0: OFF, 1: ON) GF3-GF0: Trimming color replacement color code (16 colors)
GC: Graphic color character color replacement control (0: OFF, 1: ON) GC3-GC0: Character color replacement color code (16 colors)

[Function]

Command 6-3 controls the replacement of a specified color in graphics characters with the character color or trimming color.

[Description]

- Graphics characters are registered in font ROM in fixed colors, but this command allows two of the 16 colors to be designated for replacement as the trimming color and character color.
- The setting GF=1 causes areas of the color specified as the trimming color to be replaced by the color that is designated as the trimming color for that line (by command 3).
- The setting GC=1 causes areas of the color specified as the character color to be replaced by the color that is designated as the character color for that line (by command 1).

Notes:
- This command applies only to colors of graphics characters in a main screen display.
- If both the trimming color replacement and character color replacement settings are selected at the same time, they should be set for different colors.
- Transparent and semi-transparent colors are applied to colors after replacement.

• **Command 7-1 (Screen background character control 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	1	1	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

PM7-PM0: Screen background character code
(000_H to $0FF_H$, 256 types)

[Function]

Command 7-1 controls screen background characters.

[Description]

- The display can be started by using command 5-0 to turn screen background character output control ON (PDS-1).
- Vertical character size can be set by command 7-3 for screen background character vertical size control (PH2-PH0).

Notes: • Screen background characters can only be selected from the first 256 or the 512 characters, using character codes in multiples of 4 (PM1=0, PM0=0).
• Only graphics character arrays of 2 characters wide x 2 characters high may be designated.
• Screen background character replacement colors (command 6-3) may not be applied.

• **Command 7-3 (Screen background character control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	0	0	PH2	PH1	PH0	U3	U2	U1	U0

PH2-PH0: Screen background character vertical size control (18-32 dots, in 2-dot units)
U3-U0: Screen background color (16 colors)

[Function]

Command 7-3 controls screen background characters and the screen background color.

[Description]

- The screen background color is displayed by using command 5-0 to turn the screen background output control ON (UDS=1).
- The screen background characters are displayed by using command 5-0 to turn the screen background character output control ON (PDS=1).

• **Command 8-1 (Sprite character control 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0

SD1, SD0: Sprite character configuration control
(0,0: 1 character)
(0,1: Horizontal 2 characters)
(1,0: Vertical 2 characters)
(1,1: Vertical 2 x horizontal 2 characters)

SM7-SM0: Sprite character codes
(000_H to $0FF_H$, 256 types)

[Function]

Command 8-1 controls sprite characters.

[Description]

- Sprite character display is started by using command 5-0 to turn sprite character output control ON (SDS=1).
- The sprite character start position is set by command 9-0 and command 9-1.
- Vertical size is controlled by using command 8-2 to set the sprite character vertical size control (SH2-SH0), and blinking is controlled by the sprite character blinking control bit (SBL).
- The sprite character blinking period and duty are controlled by the BT1, BT0, BD1, and BD0 bits in command 5-1.

Notes:
- Sprite characters may only be selected from the first 256 of the 512 characters.
- For configurations of 2 characters or greater, only characters codes in multiples of 4 (SM1=0, SM0=0) may be used.
- Sprite characters are always displayed in graphic character displays
- Replacement color control (command 6-3) cannot be applied to sprite characters.

• **Command 8-2 (Sprite character control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	0	1	SBL	0	SH2	SH1	SH0	0	0	0	0

SBL: Sprite character blinking control
(0: OFF, 1: ON)

SH2-SH0: Sprite character vertical size control
(18-32 dots, in 2-dot units)

[Function]

Command 8-2 controls sprite characters.

• **Command 9-0 (Sprite character control 3)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0

SY9-SY0: Sprite character vertical display position control (0-2046, in 2-dot units)

[Function]

Command 9-0 controls the sprite character vertical display position.

• **Command 9-1 (Sprite character control 4)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0

SX9-SX0: Sprite character horizontal display position control (0-2046, in 2-dot units)

[Function]

Command 9-1 controls the sprite character horizontal display position.

[Description]

For information related to sprite character settings, see the description under command 8-1.

• **Command 11-0 (Sync control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	EG1	EG0	0	FC0	FLD	0	0	0

EG1, EG0: Vertical enlargement control
(0,0: Interlaced)
(0,1: Non-interlaced)
(1,0: Setting prohibited)
(1,1: Vertical 2x)

FC0: Field 0 correction control
Field E-0 conversion
(0: No correction, 1: Correction)

FLD: Field 0 signal input control
(0: Internal separation generation,
1: External input)

[Function]

Command 11-0 controls the synchronization system.

[Description]

- The vertical display area is adjusted by the combination of vertical enlargement control (EG1, EG0) and the scan method. This setting is applied to all vertical count parameters (display position, dot size).
- If interlaced display (EG1=0, EG0=0) is used, the field 0 signal input control (FLD) is used to select either an internally generated field signal or an externally input signal. If an external input is used the field signal must be input from the EVEN pin.

• **Command 11-2 (Dot clock control 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	0	DO	0	0	0	DP1	DP0	0	0	0	DC0

DO: Dot clock pin output control
(0: OFF, 1: ON)

DC0: Dot clock selection control
(0: external input, 1: internal VCO (H-PLL)

DP1, DP0: Dot clock prescaler control
(0,0: 1/1)
(0,1: 1/2)
(1,0: 1/4)
(1,1: 1/8)

[Function]

Command 11-2 controls the dot clock signal.

[Description]

The internal dot clock signal can be output from the DOCKO pin by setting the dot clock pin output control to ON (DO=1).

Note: If no external dot clock signal is needed, it is recommended that the dot clock pin output control be set to OFF (DO=0) to keep noise to a minimum.

• **Command 11-3 (Dot clock control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	1	DK9	DK8	DK7	DK6	DK5	DK4	DK3	DK2	DK1	DK0

DK9-DK0: Dot clock multiplier value (4-dot units)

[Function]

Command 11-3 adjusts the dot clock frequency.

[Description]

This command sets the number by which the prescaler multiplies the input dot clock signal to produce the horizontal sync signal period (in 4-dot units).

Notes:
- Settings lower than 040_H may not be used.
- This setting is necessary only when an internal VCO signal is used.

• **Command 13-0 (I/O pin control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	0	0	VHE	0	0	SIX	0	0	DHX	DBX	DCX

VHE: Vertical sync detection HSYNC edge selection (0: Front edge, 1: back edge)

SIX: Sync signal input logic control (0: inverse logic, 1: normal logic)
DCX: Display color signal output logic control (0: normal logic, 1: inverse logic)
DBX: Display output period signal logic control (0: normal logic, 1: inverse logic)
DHX: Semi-transparent period signal output logic control (0: normal logic, 1: inverse logic)

[Function]

Command 13-0 controls the input-output pin functions.

[Description]

This command can eliminate vertical movement (dancing) by using the vertical sync detection HSYNC edge selection (VHE) to adjust the vertical sync signal and horizontal sync signal input timing.

Note: The sync signal input logic control bit (SIX) is applied to both the vertical sync signal and horizontal sync signal.

• **Command 14-0 (Command ROM transfer start address 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	TSD	TSC	TSB	TSA	TS9	TS8

TSD-TS8: Command ROM transfer start address 1 (high address)

[Function]

Command 14-0 is used for the command ROM transfer start address 1 setting.

[Description]

This command sets the upper half of the starting address for a command ROM transfer.

• **Command 14-1 (Command ROM transfer start address 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	1	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	0

TS7-TS1: Command ROM transfer start address 2 (low address)

[Function]

Command 14-1 is used for the command ROM transfer start address 2 setting.

[Description]

This command sets the lower half of the starting address for a command ROM transfer.

• **Command 14-2 (Command ROM transfer end address 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	0	0	0	TED	TEC	TEB	TEA	TE9	TE8

TED-TE8: Command ROM transfer end address 1 (high address)

[Function]

Command 14-2 is used for the command ROM transfer end address 1 setting.

[Description]

This command sets the upper half of the ending address for a command ROM transfer.

• **Command 14-3 (Command ROM transfer end address 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	1	TSV	TE7	TE6	TE5	TE4	TE3	TE2	TE1	1

TSV: Command ROM transfer sync control (0: Not synchronized, 1: V synchronized)

TE7-TE1: Command ROM transfer end address 2 (low address)

[Function]

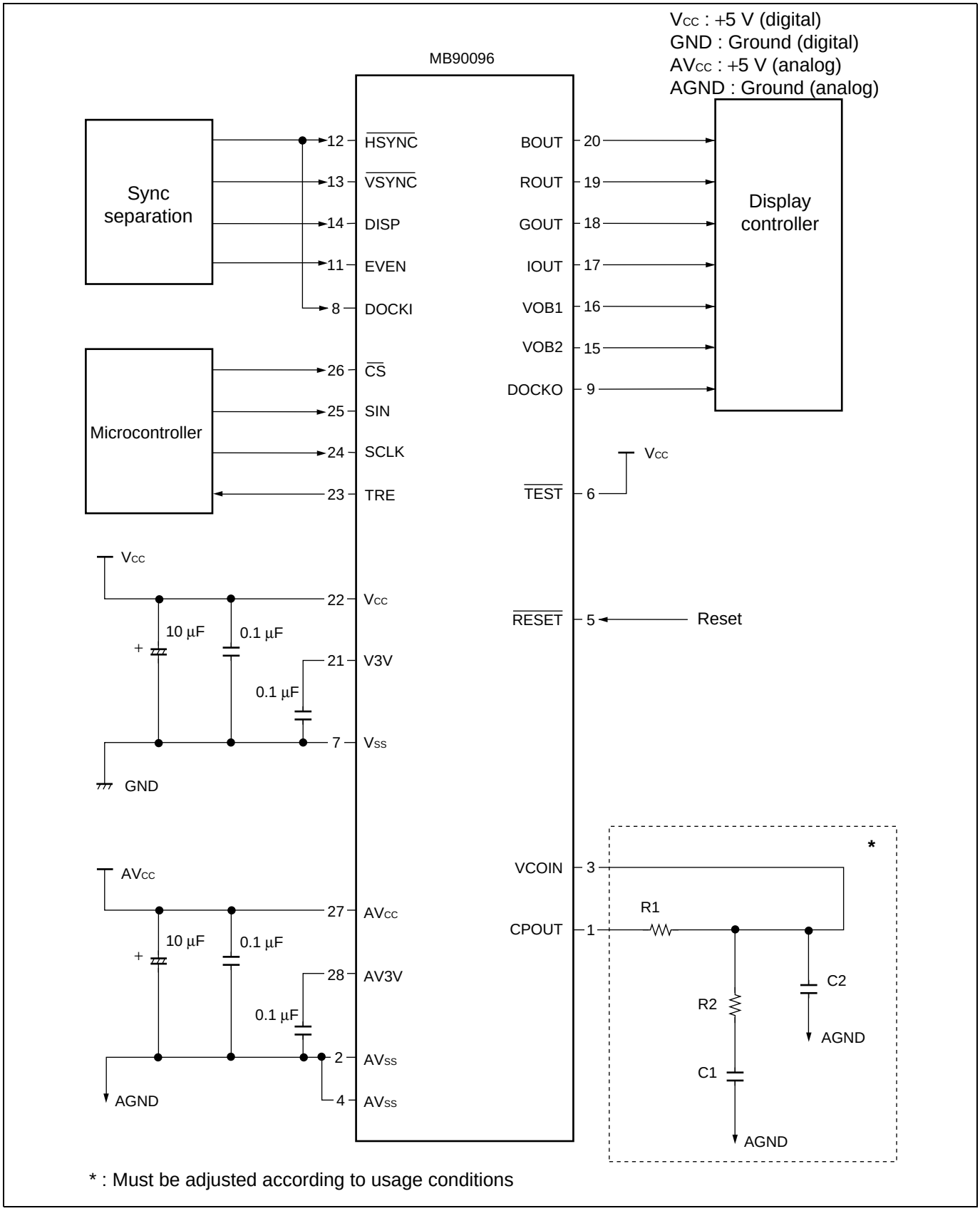
Command 14-3 is used for the command ROM transfer end address 2 setting.

[Description]

- This command sets the lower half of the ending address for a command ROM transfer.
- Turn the command ROM transfer sync control ON (TSV=1) to start a transfer in sync with the front edge of the vertical sync signal.
- When the command ROM transfer sync control is OFF (TSV=0), a transfer is started when this command is issued.

Note: If command ROM transfer sync control is used, it is necessary to use the screen output control command (command 5-0) to turn one of the output control bits (SDS, PDS, UDS, DSP) ON.

■ SAMPLE APPLICATION CIRCUIT

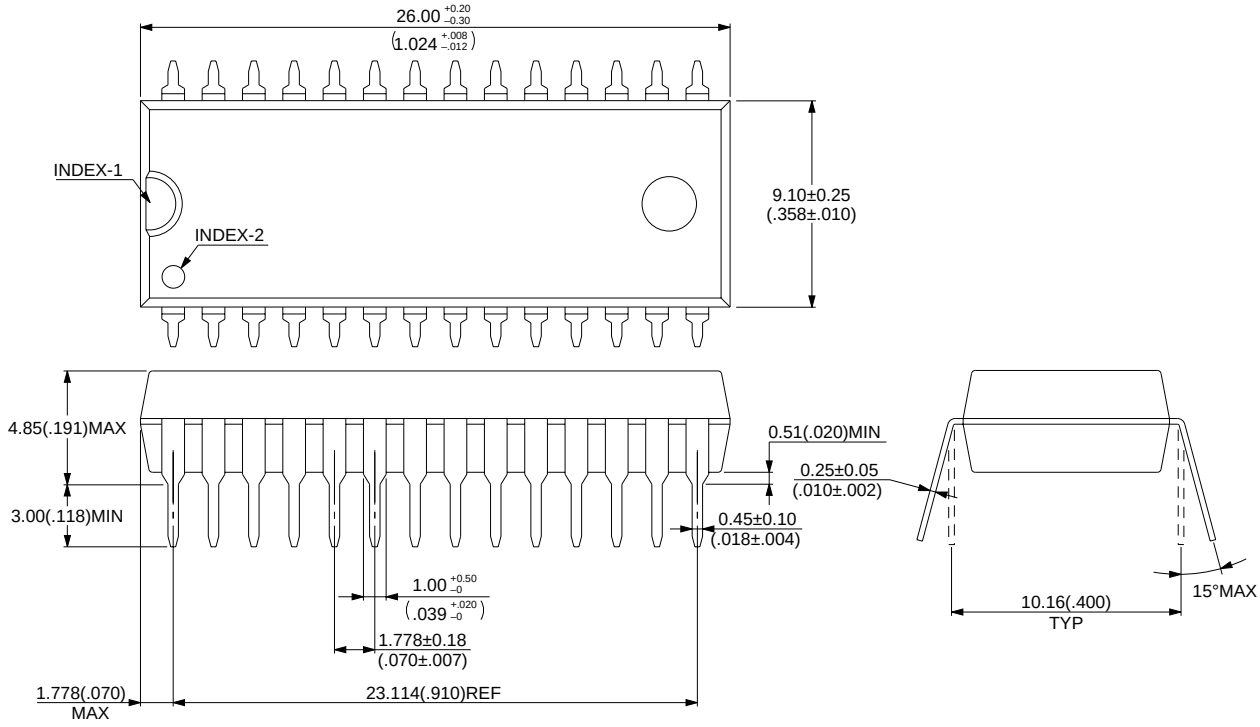


■ ORDERING INFORMATIONS

Part number	Package	Remarks
MB90096P	28-pin plastic SH-DIP (DIP-28P-M03)	
MB90096PF	28-pin plastic SOP (FPT-28P-M17)	

■ PACKAGE DIMENSIONS

28-pin plastic SH-DIP
(DIP-28P-M03)

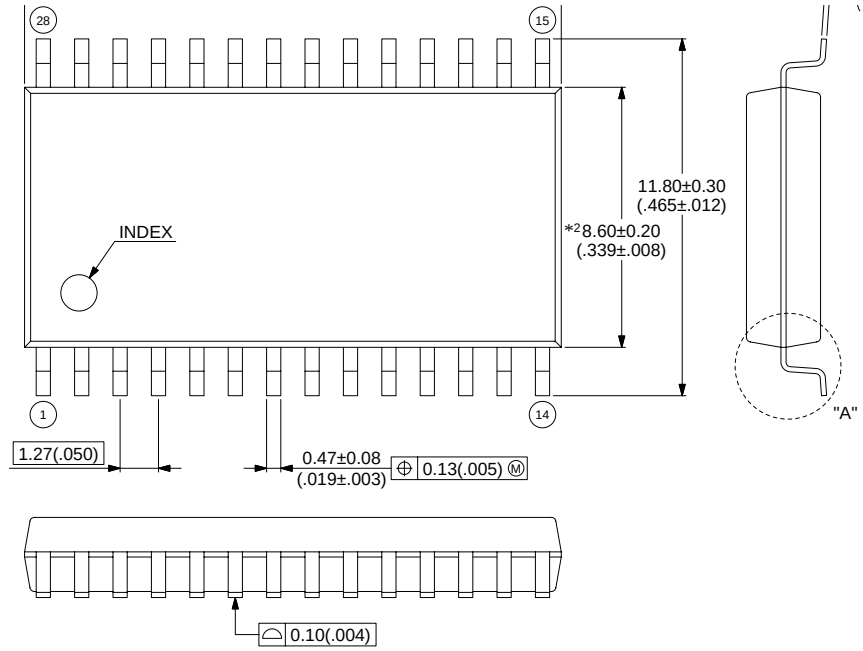


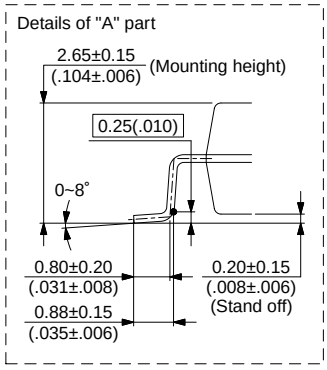
Dimensions in mm (inches) .

(Continued)

(Continued)

28-pin plastic SOP
(FPT-28P-M17)





Dimensions in mm (inches) .

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0303