FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12547-4E

8-bit Original Microcontroller

CMOS

F²MC-8L MB89530A Series

MB89535A/537A/537AC/538A/538AC/F538
MB89P538/PV530

■ DESCRIPTION

The MB89530A series is a one-chip microcontroller featuring the F²MC-8L core supporting low-voltage and high-speed operation. Built-in peripheral functions include timers, serial interface, A/D converter, and external interrupt. This product is an ideal general-purpose one-chip microcontroller for a wide variety of applications from household to industrial equipment, as well as use in portable devices.

■ FEATURES

- Wide range of package options
  - Two types of QFP packages (1 mm pitch, 0.65 mm pitch)
  - LQFP package (0.5 mm pitch)
  - SH-DIP package
- Low voltage, high-speed operating capability
  - Minimum instruction execution time 0.32 µs (at base oscillator 12.5 MHz)
- F²MC-8L CPU Core
  - Instruction set optimized for controller operation
  - Multiplication/division instructions
  - 16-bit calculation
  - Branching instructions with bit testing
  - Bit operation instructions, etc.
- Five timer systems
  - 8-bit PWM timer with 2 channels (usable as either interval timer of PWM timer)
  - Pulse width count timer (supports continuous measurement or remote control receiving applications)
  - 16-bit timer counter
  - 21-bit time base timer
  - Watch prescaler (17-bit)
- UART
  - Synchronous or asynchronous operation, switchable
- 2 serial interfaces (Serial I/O)
  - Selection of transfer direction (specify MSB first or LSB first) for communication with a variety of devices

(Continued)

FUJITSU

(Continued)

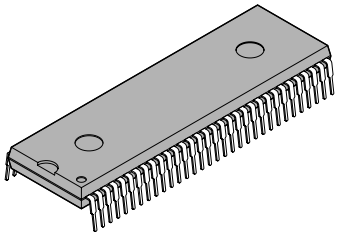
- 10-bit A/D converter (8 channels)
  - External clock input for startup support
  - Time base timer output for startup support (except MB89F538)
- Pulse generators (PPG) with 2-program capability
  - 6-bit PPG with selection of pulse width and pulse period
  - 12-bit PPG (2 channels) with selection of pulse width and pulse period
- I^2C interface circuits
- External interrupt 1 (single-clock system : 4 channels, dual-clock system : 3 channels)
  - 4 or 3 independent inputs, release enabled from standby mode (includes edge detection function)
- External interrupt 2 (8 channels)
  - 8 independent inputs, release enabled form standby mode (includes level edge detection function)
- Standby modes (low power consumption modes)
  - Stop mode (oscillator stops, virtually no power consumed)
  - Sleep mode (CPU stops, power consumption reduced to one-third)
  - Sub clock mode
  - Watch mode
- Watchdog timer reset
- I/O ports
  - Maximum ports

Single-clock system	: Except MB89F538	53 ports
	: MB89F538	52 ports
Dual-clock system	: Except MB89F538	51 ports
	: MB89F538	50 ports

  - 38 general-purpose I/O ports (CMOS) (MB89F538 : 37 general-purpose I/O ports)
  - 2 general-purpose I/O ports (N-ch open drain)
  - 8 general-purpose output ports (N-ch open drain)
  - General-purpose input ports (CMOS) : single-clock system : 5 ports, dual-clock system : 3 ports

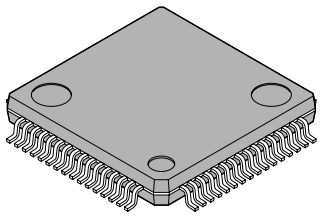
■ PACKAGES

64-pin, Plastic SH-DIP



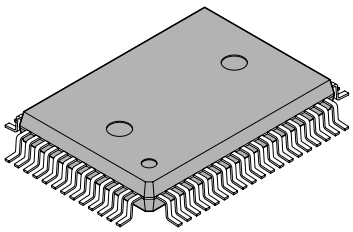
(DIP-64P-M01)

64-pin, Plastic LQFP



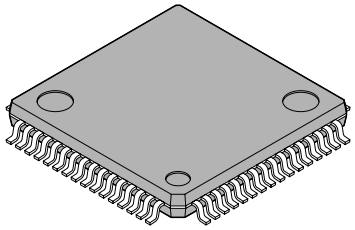
(FPT-64P-M03)

64-pin, Plastic QFP



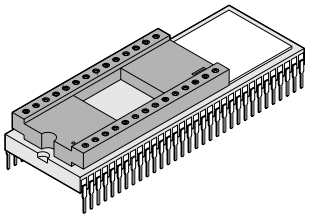
(FPT-64P-M06)

64-pin, Plastic QFP



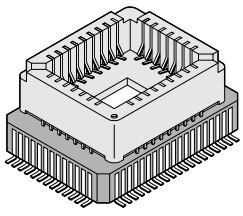
(FPT-64P-M09)

64-pin, Ceramic MDIP



(MDP-64C-P02)

64-pin, Ceramic MQFP



(MQP-64C-P01)

■ PRODUCT LINEUP

Parameter \ Part number		MB89535A	MB89537A/ 537AC	MB89538A/ 538AC	MB89F538	MB89P538	MB89PV530
Type		Mass produced (Mask ROM)			Flash memory	One-time programmable	Evaluation
ROM capacity		16 K × 8-bit (built-in ROM)	32 K × 8-bit (built-in ROM)	48 K × 8-bit (built-in ROM)	48 K × 8-bit (built-in Flash memory) (write from general purpose EPROM writer)	48 K × 8-bit (built-in ROM) (write from general purpose EPROM writer)	48 K × 8-bit (external ROM) *2
RAM capacity		512 byte × 8-bit	1 K × 8-bit	2 K × 8-bit			
Operating voltage		2.2 V to 5.5 V *1 (MB89535A/537A/538A/537AC/538AC)			3.5 V to 5.5 V	2.7 V to 5.5 V	2.7 V to 5.5 V
CPU functions		Basic instructions : 136 Instruction bit length : 8-bits Instruction length : 1 bit to 3 bits Data bit length : 1, 8, 16-bits Minimum instruction execution time : 0.32 µs / 12.5 MHz Minimum interrupt processing time : 2.88 µs / 12.5 MHz					
Peripheral functions	Ports	Input ports : single-clock system : 5 (4 also usable as external interrupts) dual-clock system : 3 (3 also usable as external interrupts) Output-only ports (N-ch open drain) : 8 (8 also usable as ADC input) I/O ports (N-ch open drain) : 2 (2 also usable as SO2/SDA or SI2/SCL) I/O ports (CMOS) (Except MB89F538) : 38 I/O ports (CMOS) (MB89F538) : 37 (21 have no other function) Total (except MB89F538) : single-clock system : 53 dual-clock system : 51 Total (MB89F538) : single-clock system : 52 dual-clock system : 50					
	Time base timer	21 bits Interrupt periods at main clock oscillation frequency of 12.5 MHz (approx. 0.655 ms, 2.621 ms, 20.97 ms, 335.5 ms)					
	Watchdog timer	Reset period of approx. 167.8 ms to 335.6 ms at main clock frequency of 12.5 MHz Reset period of approx. 500 ms to 1000 ms at sub clock frequency of 32.768 kHz.					
	PWM timer	8-bit interval timer operation (supports square wave output, operating clock period : 1, 8, 16, 64 t_{inst}*3) Pulse width measurement with 8-bit resolution (conversion period : 2^8 t_{inst}*3 to $2^8 \times 64$ t_{inst}*3) 2 channels (can also be used as interval timer, can also be used as ch1 output and ch2 count clock)					
Watch prescaler		Interval times at 17-bit sub clock base frequency of 32.768 kHz (approx. 31.25 ms, 0.25 s, 0.50 s, 1.00 s, 2.00 s, 4.00 s)					

(Continued)

(Continued)

Part number / Parameter		MB89535A	MB89537A/ 537AC	MB89538A/ 538AC	MB89F538	MB89P538	MB89PV530
Peripheral functions	Pulse width count timer	8-bit one-shot timer operation (supports underflow output, operating clock period : 1, 4, 32 t_{inst}*3, external) 8-bit reload timer operation (supports square wave output, operating clock period : 1, 4, 32 t_{inst}*3, external) 8-bit pulse width measurement operation (continuous measurement, H width measurement, L width measurement, ↑ to ↑, ↓ to ↓, H width measurement and ↑ to↑)					
	16-bit timer/ counter	16-bit timer operation (operating clock period : 1 t_{inst}*3, external) 16-bit event counter operation (select rising, falling, or both edges) 16-bit × 1 ch					
	Serial I/O	8 bit length Selection of LSB first or MSB first Transfer clock (2, 8, 32 t_{inst}*3, external)					
	UART/SIO	CLK synchronous/CLK asynchronous data transfer capability (8, 9 bit with parity bit, or 7,8 bit without parity bit) . Built-in baud rate generator provides selection of 14 baud rate settings.					
	UART	CLK synchronous/CLK asynchronous data transfer capability (4, 6, 7, 8 bit with parity bit, or 5, 7, 8, 9 bit without parity bit) . Built-in baud rate generator provides selection of 14 baud rate settings. External clock output, 2-channel 8-bit PWM timer output also available for baud rate settings.					
	External interrupt 1	Single-clock system : 4 channels independent, dual-clock system : 3 channels independent. Selection of rising, falling, or both edge detection. Can be used for recovery from standby mode (edge detection also available in stop mode)					
	External interrupt 2	Except MB89F538 : 8 ch, MB89F538 : 7 ch Can be used for recovery from standby mode.					
	6-bit PPG, 12-bit PPG	Can generate square wave signals with programmable period. 6-bit × 1 channel or 12-bit × 2 channels.					
	I^2C bus interface	—	1-channel , compatible with Intel System Administrator bus version 1.0 and Philips I^2C specifications. 2-line communications (on MB89PV530/P538/F538/537AC/538AC)				
	A/D converter	10-bit resolution × 8 channels. A/D conversion functions (conversion time : 60 t_{inst}*3) Supports repeated calls from external clock (except MB89F538) . Supports repeated calls from internal clock. Standard voltage input provided (AVR)					
Standby modes (power saving modes)		Sleep mode, stop mode, sub clock mode, watch mode.					
Process		CMOS					

*1 : Depends on operating frequency.

*2 : Using external ROM and MBM27C512.

*3 : t_{inst} represents instruction execution time. This can be selected as 1/4, 1/8, 1/16, 1/64 of the main clock cycle or 1/2 of the sub clock cycle.

Note : MB89535A/537A/538A have no built-in I^2C functions.
To use I^2C functions, choose the MB89PV530/MB89P538/F538/537AC/538AC.

■ MODEL DIFFERENCES AND SELECTION CONSIDERATIONS

Part number / Package	MB89535A	MB89537A/ 537AC	MB89538A/ 538AC	MB89F538	MB89P538	MB89PV530
DIP-64P-M01	O	O	O	O	O	X
FPT-64P-M03	O	O	O	X	X	X
FPT-64P-M06	O	O	O	O	O	X
FPT-64P-M09	O	O	O	O	O	X
MDP-64C-P02	X	X	X	X	X	O
MQP-64C-P01	X	X	X	X	X	O

O : Model-package combination available

X : Model-package combination not available

Conversion sockets for pin pitch conversion (manufactured by Sunhayato Corp.) can be used.

Contact : Sunhayato Corp. : TEL : +81-3-3984-7791
FAX : +81-3-3971-0535
E-mail : adapter@sunhayato.co.jp

■ DIFFERENCES AMONG PRODUCTS

1. Memory Capacity

When this product is used in a piggy-back or other evaluation configuration, it is necessary to carefully confirm the differences between the model being used and the product it is evaluating. Particular attention should be given to the following (see "■CPU CORE 1.Memory Space") .

- The program ROM area starts from address 4000_H on the MB89F538, MB89P538 and MB89PV530 models.
- Note upper limits on RAM, such as stack areas, etc.

2. Current Consumption

- On the MB89PV530, the additional current consumed by the EPROM is added at the connecting socket on the back side.
- When operating at low speed, the current consumption in the one-time PROM or EPROM models is greater than on the mask ROM models. However, current consumption in sleep or stop modes is identical.

For details, refer to "■ELECTRICAL CHARACTERISTICS".

3. Mask Options

The options available for use, and the method of specifying options, differ according to the model. Before use, check the "■ MASK OPTIONS" specification section.

4. Wild Register Functions

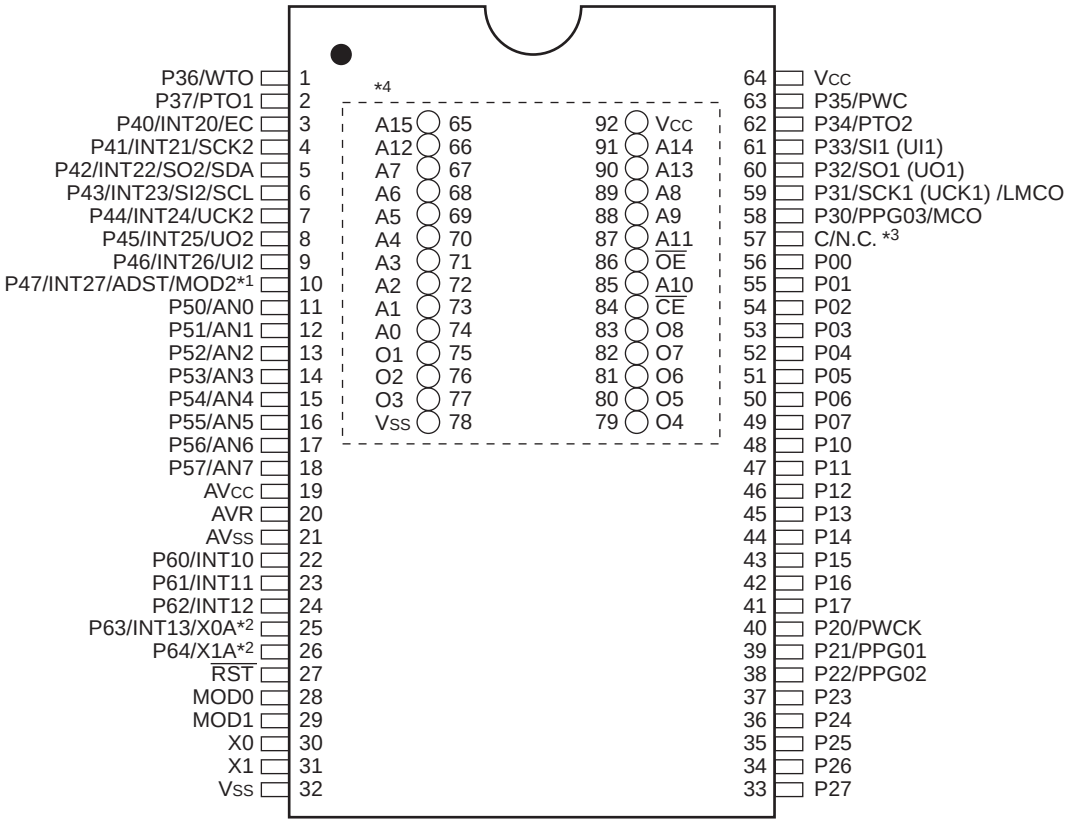
The following table shows areas in which wild register functions can be used.

Wild Register Usage Areas

Part number	Address space
MB89PV530	4000_H to $FFFF_H$
MB89P538	4000_H to $FFFF_H$
MB89F538	4000_H to $FFFF_H$
MB89537A/537AC	8000_H to $FFFF_H$
MB89538A/538AC	4000_H to $FFFF_H$
MB89535A	$C000_H$ to $FFFF_H$

■ PIN ASSIGNMENTS

(TOP VIEW)



(DIP-64P-M01)
(MDP-64C-P02)

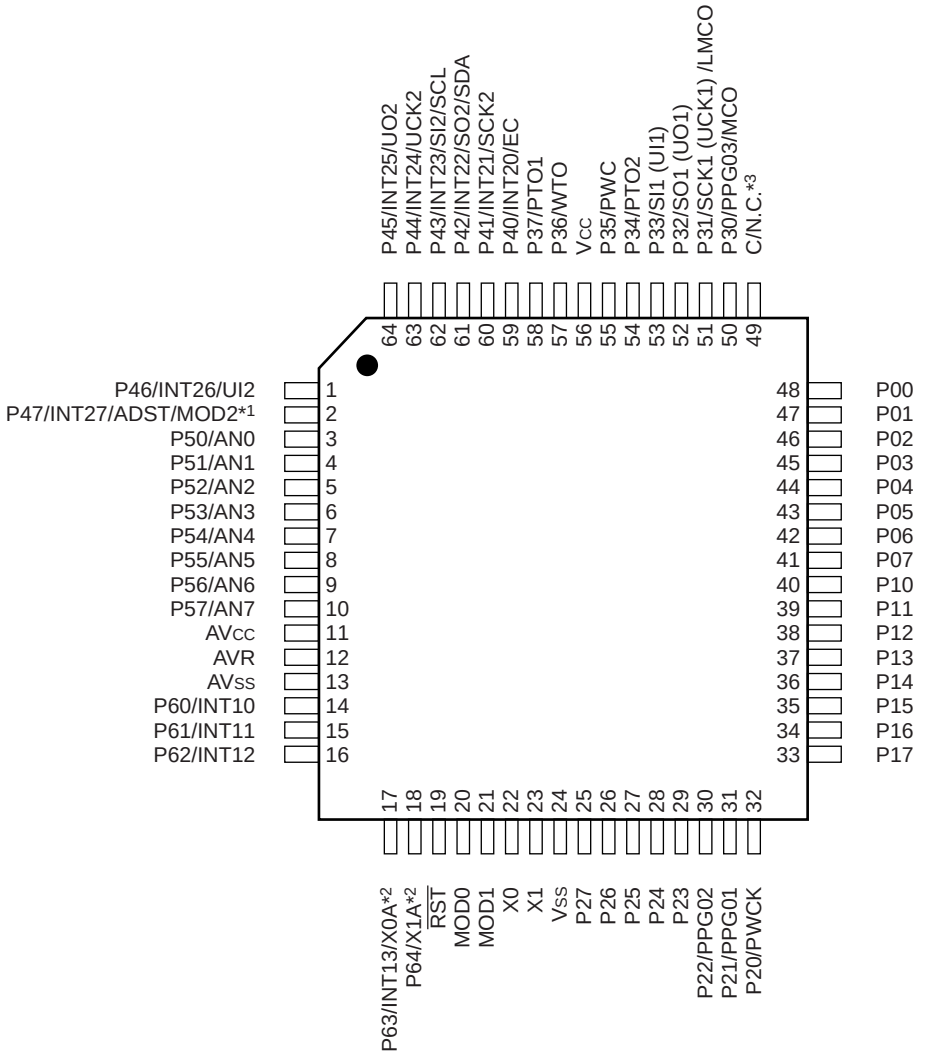
*1 : Pin 10 is MOD2 pin for MB89F538 and P47/INT27/ADST pins except for MB89F538.
*2 : Pin 25 and pin 26 are P63/INT13, P64 pins for single-clock system and X0A, X1A pins for dual-clock system.
*3 : The function of pin 57 depends on the model. For details, see "■PIN DESCRIPTIONS" and "■HANDLING DEVICES".
*4 : Package top pin assignments (MB89PV530 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	A15	73	A1	81	O6	89	A8
66	A12	74	A0	82	O7	90	A13
67	A7	75	O1	83	O8	91	A14
68	A6	76	O2	84	$\overline{CE}$	92	V_{CC}
69	A5	77	O3	85	A10		
70	A4	78	V_{SS}	86	$\overline{OE}$		
71	A3	79	O4	87	A11		
72	A2	80	O5	88	A9		

N.C. : Internal connection only. Not for use.

(Continued)

(TOP VIEW)



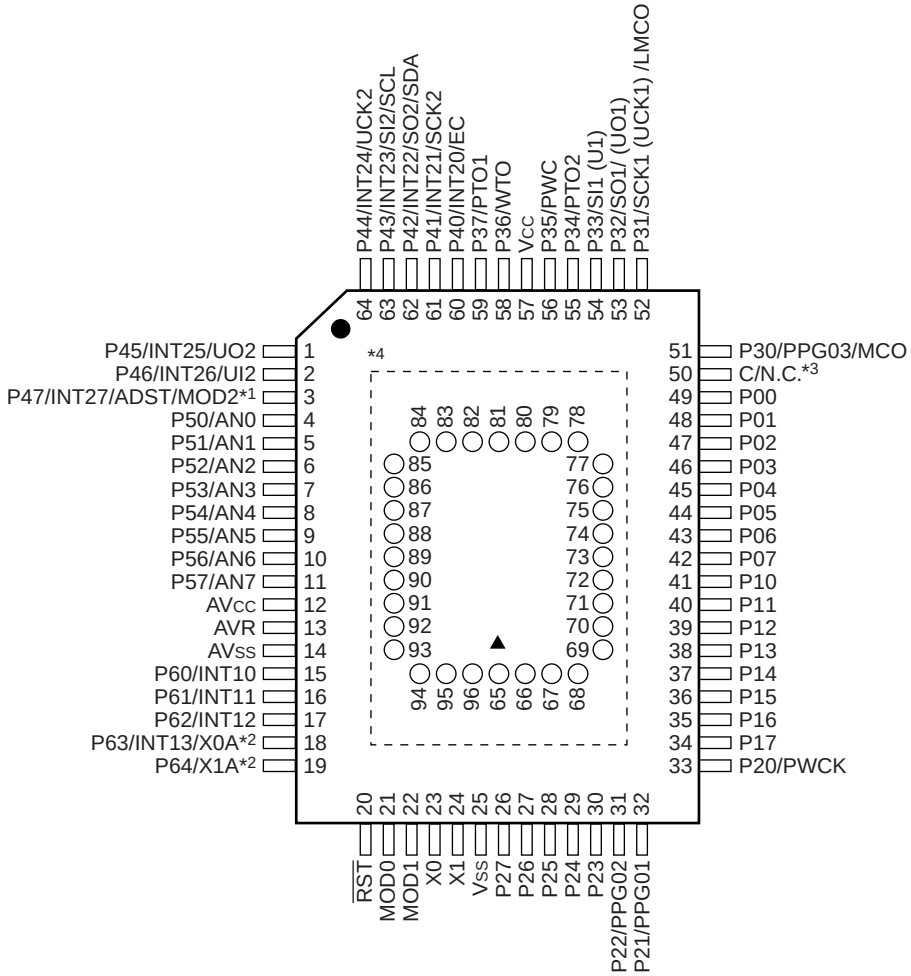
(FPT-64P-M03)
(FPT-64P-M09)

*1 : Pin 2 is MOD2 pin for MB89F538 and P47/INT27/ADST pins except for MB89F538.
*2 : Pin 17 and pin 18 are P63/INT13, P64 pins for single-clock system and X0A, X1A pins for dual-clock system.
*3 : The function of pin 49 depends on the model. For details, see “■PIN DESCRIPTIONS” and “■HANDLING DEVICES”.

(Continued)

(Continued)

(TOP VIEW)



(FPT-64P-M06)
(MQP-64C-P01)

*1 : Pin 3 is MOD2 pin for MB89F538 and P47/INT27/ADST pins except for MB89F538.
*2 : Pin 18 and pin 19 are P63/INT13, P64 pins for single-clock system and X0A, X1A pins for dual-clock system.
*3 : The function of pin 50 depends on the model. For details, see "■PIN DESCRIPTIONS" and "■HANDLING DEVICES".
*4 : Package top pin assignments (MB89PV530 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	A15	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C. : Internal connection only. Not for use.

■ PIN DESCRIPTIONS

Pin no.			Pin name	I/O circuit type	Function
SH-DIP*1 MDIP*2	QFP*3 MQFP*4	LQFP*5 QFP*6			
30	23	22	X0	A	Connecting pins to crystal oscillator circuit or other oscillator circuit. The X0 pin can connect to an external clock. In that case, X1 is left open.
31	24	23	X1		
28	21	20	MOD0	B	Input pins for memory access mode setting. Connect directly to Vss.
29	22	21	MOD1		
27	20	19	$\overline{RST}$	C	Reset I/O pin. This pin has pull-up resistance with CMOS I/O or hysteresis input. At an internal reset request, an 'L' signal is output. An 'L' level input initializes the internal circuits.
56 to 49	49 to 42	48 to 41	P00 to P07	D	General purpose I/O ports.
48 to 41	41 to 34	40 to 33	P10 to P17	D	General purpose I/O ports.
40	33	32	P20/PWCK	E	General purpose I/O port.Resource I/O pin (hysteresis input).Hysteresis input. This pin also functions as a PWC input.
39	32	31	P21/ PPG01	D	General purpose I/O port.This pin also functions as the PPG01 output.
38	31	30	P22/ PPG02	D	General purpose I/O port.This pin also functions as the PPG02 output.
37	30	29	P23	D	General purpose I/O port.
36	29	28	P24	D	General purpose I/O port.
35	28	27	P25	D	General purpose I/O port.
34	27	26	P26	D	General purpose I/O port.
33	26	25	P27	D	General purpose I/O port.
58	51	50	P30/ PPG03/ MCO	D	General purpose I/O port.This pin also functions as the PPG03 output.
59	52	51	P31/SCK1 (UCK1) / LMCO	E	General purpose I/O port.Resource I/O pin (hysteresis input).This pin also functions as the UART/SIO clock input/output pin.
60	53	52	P32/SO1 (UO1)	D	General purpose I/O port.This pin also functions as the UART/SIO data output pin.
61	54	53	P33/SI1 (UI1)	E	General purpose I/O port.Resource input/output pin (hysteresis input).This pin also functions as the UART/SIO serial data input pin.
62	55	54	P34/PTO2	D	General purpose I/O port.This pin also functions as the PWM timer 2 output pin.
63	56	55	P35/PWC	E	General purpose I/O port.Resource I/O pin (hysteresis input).This pin also functions as a PWC input.

(Continued)

Pin no.			Pin name	I/O circuit type	Function
SH-DIP*1 MDIP*2	QFP*3 MQFP*4	LQFP*5 QFP*6			
1	58	57	P36/ WTO	D	General purpose I/O port.Resource output. This pin also functions as the PWC output pin.
2	59	58	P37/ PTO1	D	General purpose I/O port.Resource output. This pin also functions as the PWM timer 1 output pin.
3	60	59	P40/ INT20/ EC	E	General purpose I/O port.Resource I/O pin (hysteresis input)This pin also functions as an external interrupt input or 16-bit timer/counter input.
4	61	60	P41/ INT21/ SCK2	E	General purpose I/O port.Resource I/O pin (hysteresis input)This pin also functions as an external interrupt input or SIO clock I/O pin.
5	62	61	P42/ INT22/ SO2/ SDA	G	N-ch open drain output. Resource I/O pin (hysteresis only for INT22 input) . This pin also functions as an external interrupt input, SIO serial data output, or I^2C data line.
6	63	62	P43/ INT23/ SI2/SCL	G	N-ch open drain output. Resource I/O pin (hysteresis only for INT23 input) . This pin also functions as an external interrupt, SIO serial data input, or I^2C clock I/O pin.
7	64	63	P44/ INT24/ UCK2	E	General purpose I/O port. Resource I/O pin (hysteresis input) . This pin also functions as an external interrupt input or UART clock I/O pin.
8	1	64	P45/ INT25/ UO2	E	General purpose I/O port. Resource I/O pin (hysteresis input) . This pin also functions as an external interrupt input or UART data output pin.
9	2	1	P46/ INT26/ UI2	E	General purpose I/O port. Resource I/O pin (hysteresis input) . This pin also functions as an external interrupt input or UART data input pin.
10	3	2	P47/ INT27/ ADST	E	Except MB89F538 General purpose I/O port. Resource I/O pin (hysteresis input) . This pin also functions as an external interrupt input or A/D converter clock input pin. MB89F538 Input pins for memory access mode setting. Connect directly to Vss.
			MOD2	B	
11 to 18	4 to 11	3 to 10	P50/AN0 to P57/ AN7	H	N-ch open drain output port. This pin also functions as an A/D converter analog input pin.

(Continued)

(Continued)

Pin no.			Pin name	I/O circuit type	Function	
SH-DIP*1 MDIP*2	QFP*3 MQFP*4	LQFP*5 QFP*6				
22 to 24	15 to 17	14 to 16	P60/INT10 to P62/INT12	I	General purpose input port. Resource input pin (hysteresis input) . This pin also functions as an external interrupt input pin.	
25	18	17	P63/INT13	I	Single-clock system	General purpose input port. Resource input (hysteresis input) . This pin also functions as an external interrupt.
			X0A	A	Dual-clock system	Connected pin for sub clock.
26	19	18	P64	J	Single-clock system	General purpose input port.
			X1A	A	Dual-clock system	Connected pin for sub clock.
64	57	56	V_{CC}	—	Power supply pin.	
32	25	24	V_{SS}	—	Ground pin (GND) .	
19	12	11	AV_{CC}	—	A/D converter power supply pin.	
20	13	12	AVR	—	A/D converter reference voltage input pin.	
21	14	13	AV_{SS}	—	A/D converter power supply pin. Used at the same voltage level as the Vss supply.	
57	50	49	C	—	MB89F538	Capacitor connection pin for stabilization power supply. Connect an external ceramic capacitor of approximately 0.1 μF.
					MB89P538	Fixed at Vss.
					MB89PV530 MB89537A/537AC MB89538A/538AC MB89535A	N.C. pin

*1 : DIP-64P-M01

*2 : MDP-64C-P02

*3 : FPT-64P-M06

*4 : MQP-64C-P01

*5 : FPT-64P-M03

*6 : FPT-64P-M09

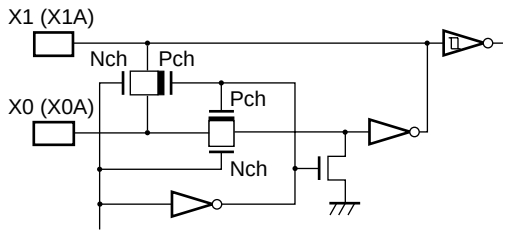
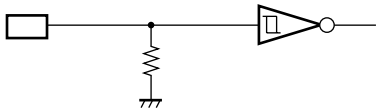
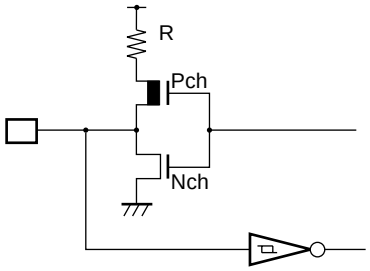
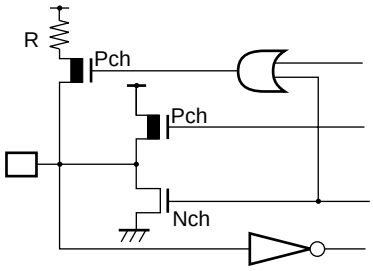
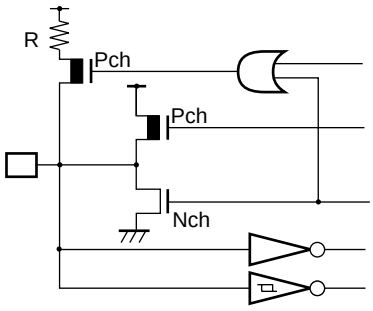
External EPROM Socket Pin Function Descriptions (MB89PV530 only)

Pin no.		Pin name	I/O Circuit type	Function
MDIP*1	MQFP*2			
65 66 67 68 69 70 71 72 73 74	66 67 68 69 70 71 72 73 74 75	A15 A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins.
75 76 77	77 78 79	O1 O2 O3	I	Data input pins
78	80	V_{SS}	O	Power supply pin (GND) .
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins.
84	87	$\overline{CE}$	O	ROM chip enable pin. Outputs an “H” level signal in standby mode.
85	88	A10	O	Address output pin.
86	89	$\overline{OE}$	O	ROM output enable pin. Outputs “L” at all times.
87 88 89	91 92 93	A11 A9 A8	O	Address output pins.
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	EPROM power supply pin.
—	65 76 81 90	N.C.	O	Internally connected. These pins always left open.

*1 : MDP-64C-P02

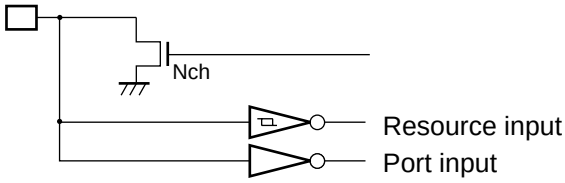
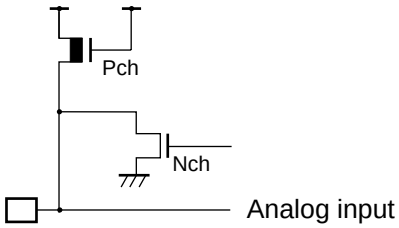
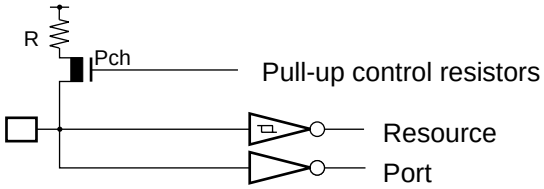
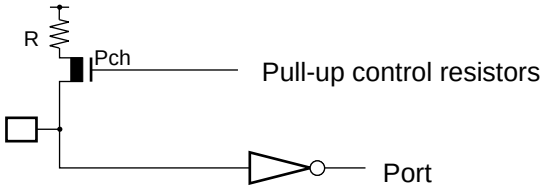
*2 : MQP-64C-P01

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		Oscillator feedback resistance • High speed side = approx. 1 MΩ • Low speed side = approx. 10 MΩ
B		• Hysteresis input • Pull-down resistance built-in to MB89535A MB89537A/537AC MB89538A/538AC
C		• Pull-up resistance approx. 50 kΩ • Hysteresis input
D	 Pull-up control resistor	• CMOS I/O • Software pull-up resistance can be used. Approx. 50 kΩ
E	 Pull-up control resistors Port input Resource input	• CMOS I/O • Software pull-up resistance can be used. Approx. 50 kΩ

(Continued)

(Continued)

Type	Circuit	Remarks
G		• N-ch open drain output • Hysteresis input • CMOS input
H		• N-ch open drain output • Analog input (A/D converter)
I		• Hysteresis input • CMOS input • Software pull-up resistance can be used. Approx. 50 kΩ
J		• CMOS input • Software pull-up resistance can be used. Approx. 50 kΩ

■ HANDLING DEVICES

1.Preventing Latchup

Care must be taken to ensure that maximum voltage ratings are not exceeded (to prevent latchup) . When CMOS integrated circuit devices are subjected to applied voltages higher than Vcc at input and output pins (other than medium- and high-withstand voltage pins), or to voltages lower than Vss, as well as when voltages in excess of rated levels are applied between Vcc and Vss, the phenomenon known as latchup can occur.

When a latchup condition occurs, supply current can increase dramatically and may destroy semiconductor elements. In using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

Also when switching power on or off to analog systems, care must be taken that analog power supplies (AV_{CC}, AVR) and analog input signals do not exceed the level of the digital power supply.

2.Power Supply Voltage Fluctuations

Even within the warranted operating range of the Vcc supply voltage, sudden changes in supply voltage can cause abnormal operation. As a measure for stability, it is recommended that the Vcc ripple fluctuation (peak to peak value) should be kept within 10% of the reference Vcc value on commercial power supply (50 Hz-60 Hz), and instantaneous voltage fluctuations such as at power-on and shutdown should be kept within a transient variability limit of 0.1V/ms.

3.Treatment of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistance.

4. Treatment of N.C. Pins

Any pins marked 'NC' (not connected) must be left open.

5. Treatment of Power Supply Pins on Models with Built-in A/D Converter

Even when A/D converters are not in use, pins should be connected so that $AV_{CC} = V_{CC}$, and $AV_{SS} = AVR = V_{SS}$.

6. Precautions for Use of External Clock

Even when an external clock signal is used, an oscillator stabilization wait period is used after a power-on reset, or escape from sub clock mode or stop mode.

7. Execution of Programs on RAM

Debugging of programs executed on RAM cannot be performed even when using the MB89PV530.

8. Wild Register Functions

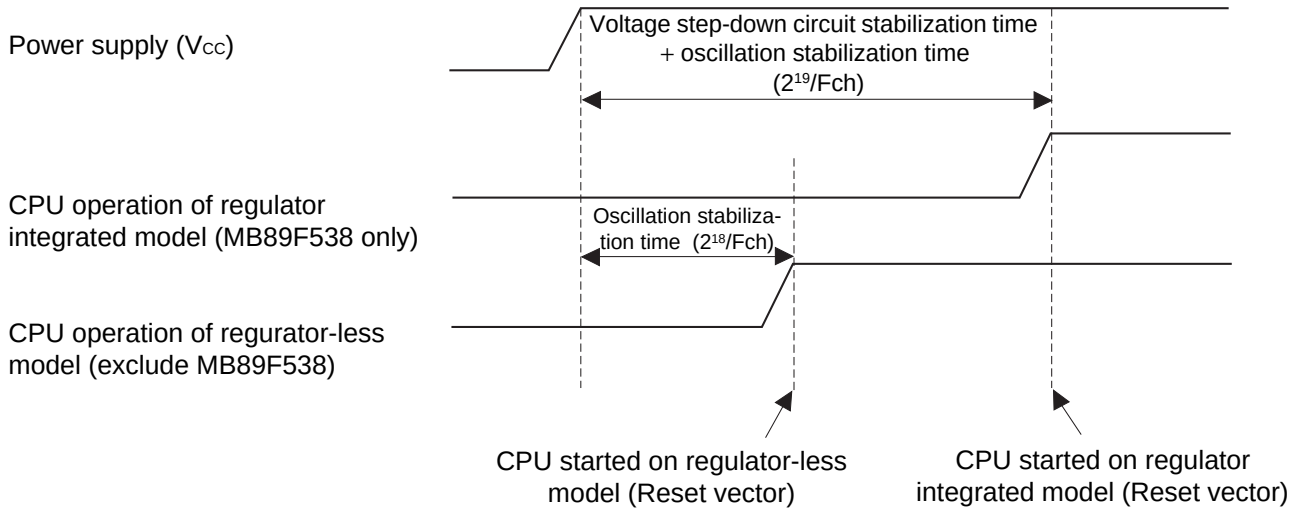
Wild registers cannot be debugged with the MB89PV530 and tools. To verify operations, actual in-device testing on the MB89P538 or MB89F538 is advised.

9. Details on handling the C terminal of the MB89530 series

The MB89530 series contains the following products. The regulator integrated model and the regulator-less model have different performance characteristics.

Part No.	Operation Voltage	integrated model	Terminal type	Terminal treatments
MB89PV530	2.7 V to 5.5 V	Not included	N.C terminal	Not required
MB89P538		Included	C terminal	Fixed to V_{CC}
		Not included		Fixed to V_{SS}
MB89F538	3.5 V to 5.5 V	Included		0.1 µF capacitor connected
MB89537A/537AC	2.2 V to 5.5 V	Not included	N.C terminal	Not required
MB89538A/538AC				
MB89535A				

Although these product models have the same internal resources, the operation sequence after a power-on reset is different between the regulator integrated model and regulator-less model.
The operation sequence after a power-on reset of each model is shown below.



Fch : Crystal oscillator frequency

As avobe, the regulator integrated model starts the CPU behind the regulator-less model. This is because the regulator requires a settling time for normal operation.
The MB89P538 offers a choice of regulator-integrated and regulator-less models selectable depending on the C-terminal treatment. Use the right one for your mask board.

10. Note to Noise in the External Reset Pin ($\overline{RST}$)

If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).

■ PROGRAMMING AND ERASING FLASH MEMORY ON THE MB89F538

1. Flash Memory

The flash memory is located between 4000_H and $FFFF_H$ in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mask ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the CPU, providing an efficient method of updating program and data.

2. Flash Memory Features

- 48 K byte × 8-bit configuration (16 K + 8 K + 8 K + 16 K sectors)
- Automatic programming algorithm (Embedded algorithm* : Equivalent to MBM29LV200)
- Includes an erase pause and restart function
- Data polling and toggle bit for detection of program/erase completion
- Detection of program/erase completion via CPU interrupt
- Compatible with JEDEC-standard commands
- Sector Protection (sectors can be combined in any combination)
- No. of program/erase cycles : 10,000 (Min)

*: Embedded Algorithm is a trademark of Advanced Micro Devices.

3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

4. Flash Memory Register

- Control status register (FMCS)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
$007A_H$	INTE	RDYINT	WE	RDY	Reserved	Reserved	—	Reserved	$000X00\text{-}0_B$
	R/W	R/W	R/W	R	R/W	R/W	—	R/W	

5. Sector Configuration

The table below shows the sector configuration of flash memory and lists the addresses of each sector for both during CPU access a flash memory programming.

- Sector configuration of flash memory

Flash Memory	CPU Address	Programmer Address*
16 K bytes	$FFFF_H$ to $C000_H$	$1FFFF_H$ to $1C000_H$
8 K bytes	$BFFF_H$ to $A000_H$	$1BFFF_H$ to $1A000_H$
8 K bytes	$9FFF_H$ to 8000_H	$19FFF_H$ to 18000_H
16 K bytes	$7FFF_H$ to 4000_H	$17FFF_H$ to 14000_H

* : Programmer address
The programmer address is the address to be used instead of the CPU address when programming data from a parallel flash memory programmer. Use the programmer address on programming or erasing using a general-purpose parallel programmer.

6. ROM Programmer Adaptor and Recommended ROM Programmers

Part number	Package	Adaptor Part No.	Recommended Programmer Manufacturer and Model
		Sunhayato Corp.	Ando Electric Co. Ltd.
MB89F538-101PF MB89F538-201PF	FPT-64P-M06	FLASH-64QF-32DP-8LF	AF9708* AF9709*
MB89F538-101PFM MB89F538-201PFM	FPT-64P-M09	FLASH-64QF2-32DP-8LF2	
MB89F538-101P-SH MB89F538-201P-SH	DIP-64P-M01	FLASH-64SD-32DP-8LF	

* : For the version of the programmer, contact the Flash Support Group, Inc.

- Enquiries

Sunhayato Corp. : TEL : +81-3-3984-7791
FAX : +81-3-3971-0535
E-mail : adapter@sunhayato.co.jp

Flash Support Group, Inc. : FAX : +81-53-428-8377
E-mail : support@j-fsg.co.jp

■ ONE-TIME WRITING SPECIFICATIONS WITH PROM AND EPROM MICROCONTROLLERS

The MB89P538 has a PROM mode with functions equivalent to the MBM27C1001, allowing writing with a general purpose ROM writer using a proprietary adapter. Note, however, that the use of electronic signature mode is not supported.

• ROM writer adapters

With some ROM writers, stability of writing performance is enhanced by placing an 0.1µF capacitor between the Vcc and Vss pins. The following table lists adapters for use with ROM writers.

ROM Writer Adapters

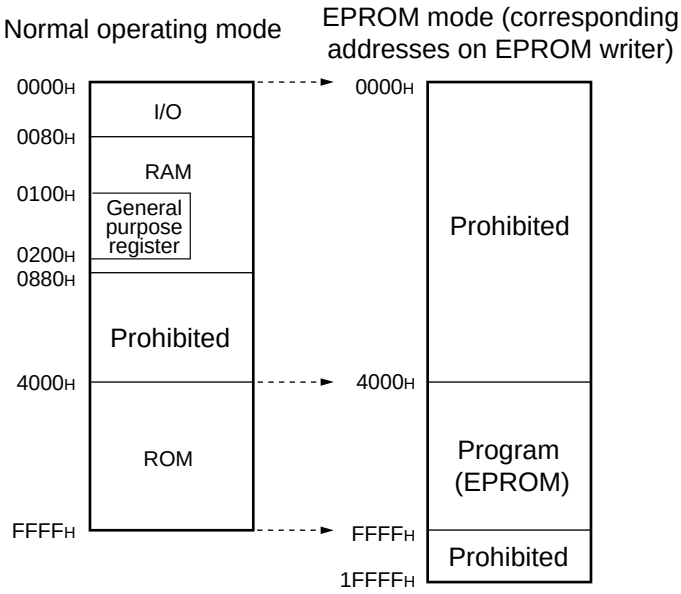
Part number	Package	Compatible adapter
MB89P538-101PF MB89P538-201PF	FPT-64P-M06	ROM-64QF-32DP-8LA2*
MB89P538-101PFM MB89P538-201PFM	FPT-64P-M09	ROM-64QF2-32DP-8LA
MB89P538-101P-SH MB89P538-201P-SH	DIP-64P-M01	ROM-64SD-32DP-8LA2*

Inquiries should be addressed to Sunhayato Corp. : TEL : +81-3-3984-7791
FAX : +81-3-5396-9106
E-mail : adapter@sunhayato.co.jp

* : Version 3 or later should be used.

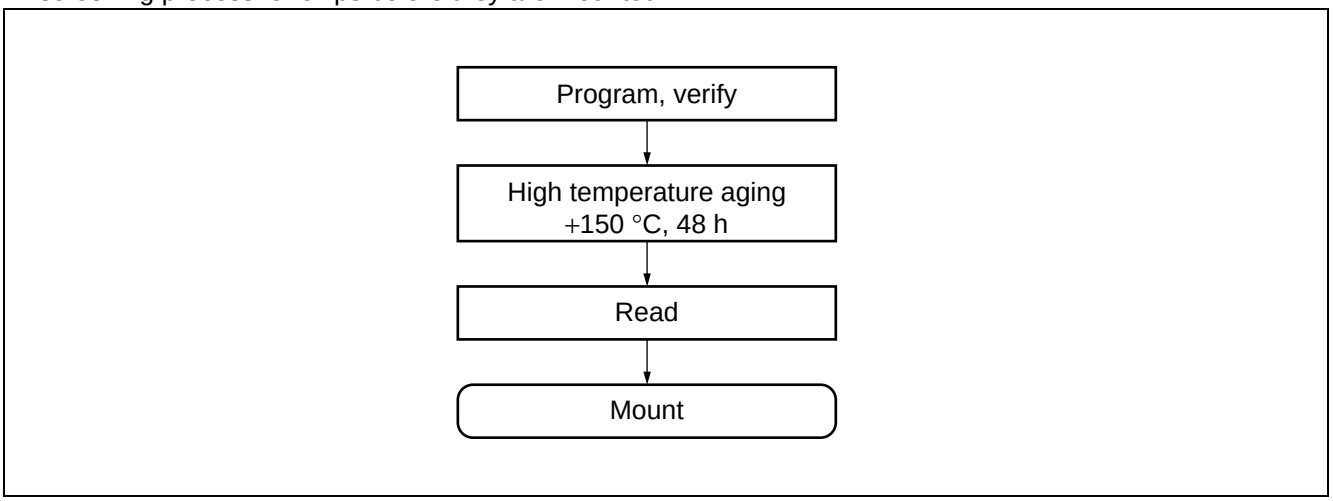
• Memory map for EPROM mode

The following illustration shows a memory map for EPROM mode. There are no PROM options.



● Recommended screening conditions

Before one-time writing of microcontroller programs to PROM, high temperature aging is recommended as a screening process for chips before they are mounted.



● About writing yields

The nature of chips before one-time writing of microcontroller programs to PROM prevents the use of all-bit writing tests. Therefore it is not possible to guarantee writing yields of 100% in some cases.

■ EPROM WRITING TO PIGGY-BACK/EVALUATION CHIPS

This section describes methods of writing to EPROM on piggy-back/evaluation chips.

• EPROM model

MBM27C512-20TV

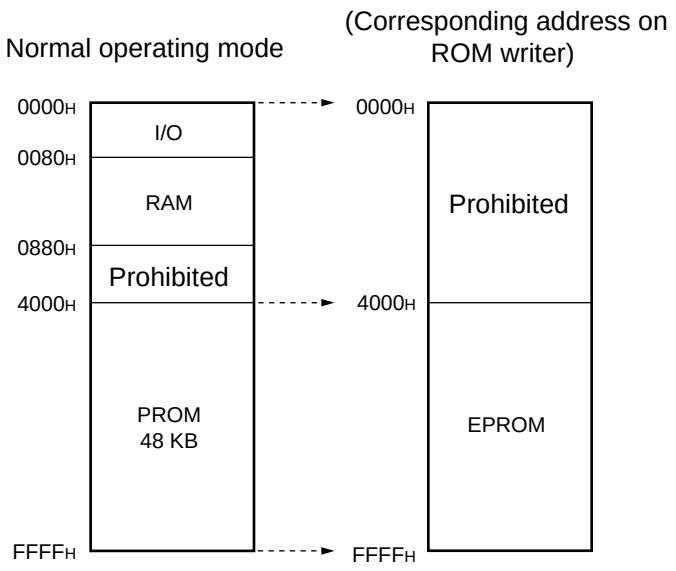
• Writer adapter

For writing to EPROM using a ROM writer, use one of the writer adapters shown below (manufactured by Sunhayato Corp.) .

Package	Adapter socket model
LCC-32 (rectangular)	ROM-32LC-28DP-YG

Inquiries should be addressed to Sunhayato Corp. : TEL : +81-3-3984-7791
FAX : +81-3-3971-0535
E-mail : adapter@sunhayato.co.jp

• Memory Space



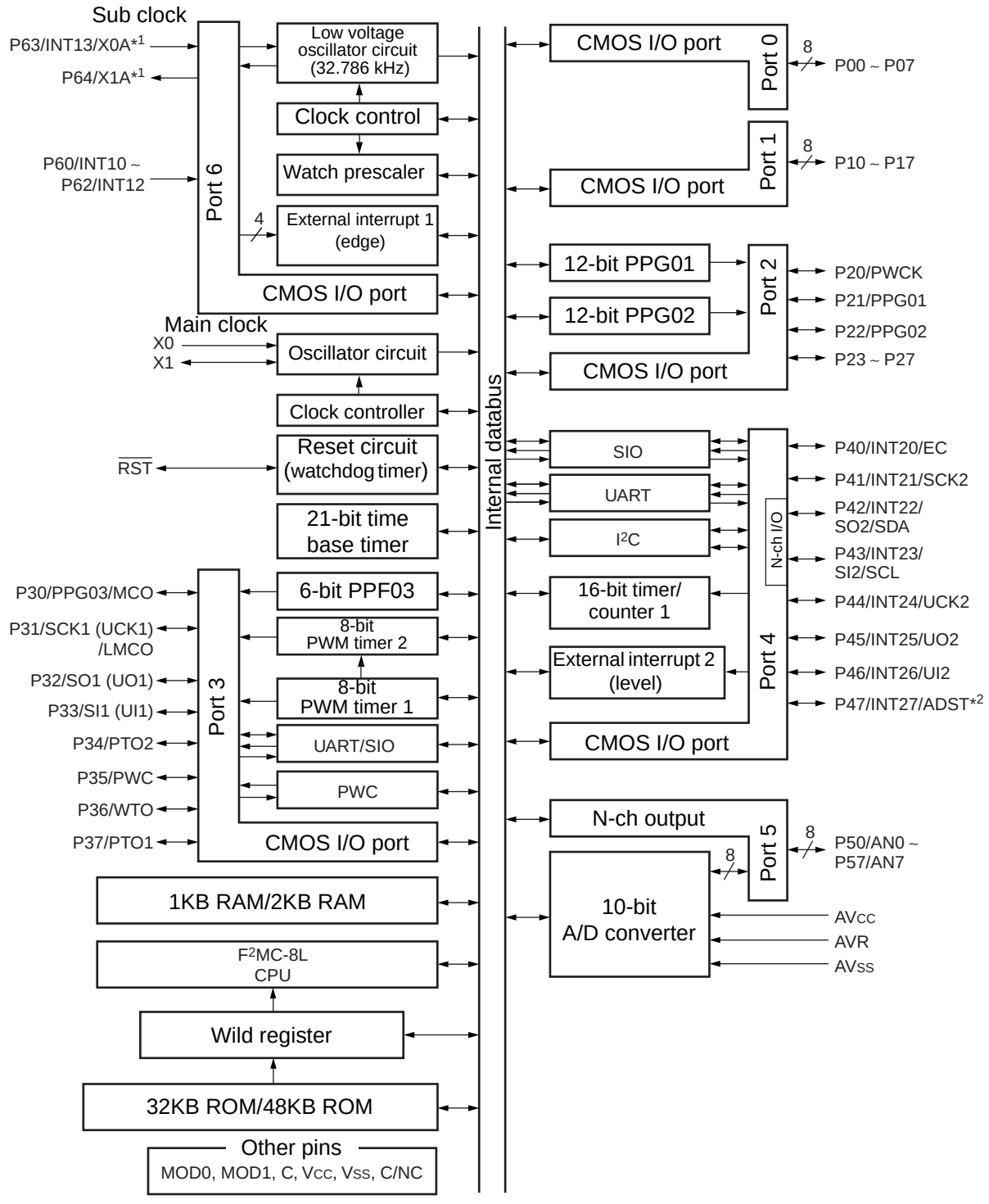
• Writing to EPROM

1) Set up the EPROM writer for the MBM27C512.

2) Load program data to the ERPOM writer, in the area 4000H - FFFFH.

3) Use the EPROM writer to write to the area 4000H - FFFFH.

■ BLOCK DIAGRAM



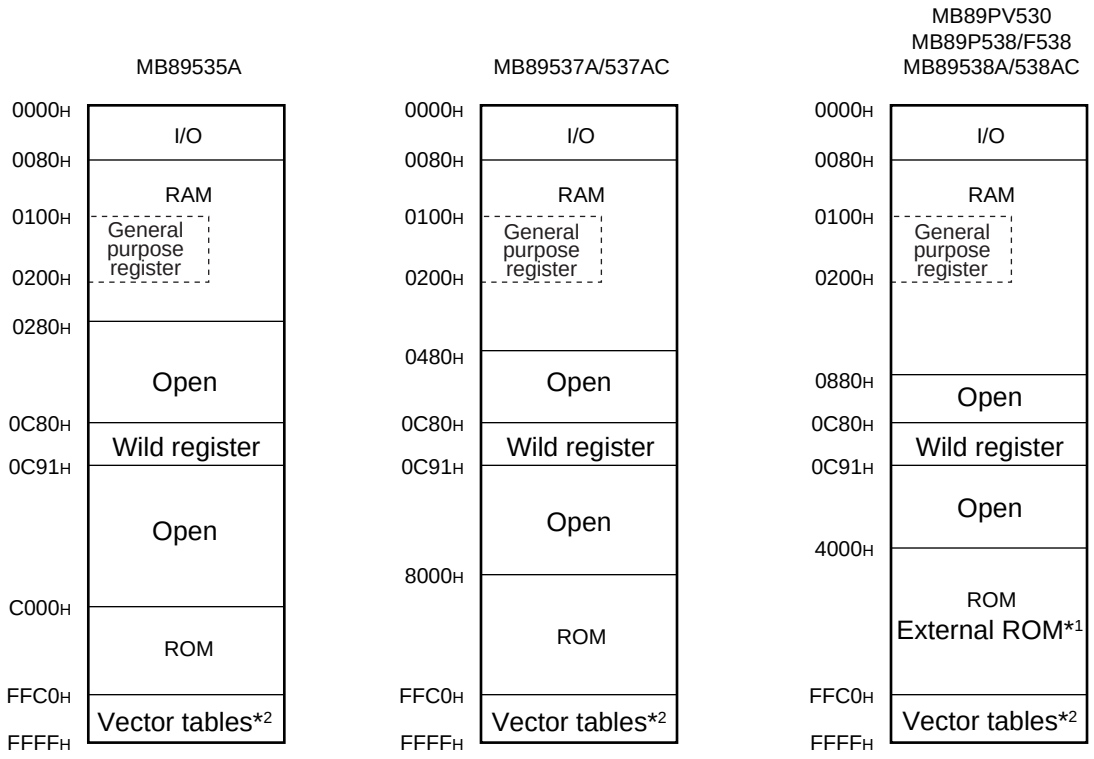
*1 : P63/INT13, P64 pins for single-clock system and X0A, X1A pins dual-clock system
*2 : P47/INT27/ADST pins are MOD2 pin for MB89F538.

■ CPU CORE

1. Memory Space

The MB89530A series has 64 KB of memory space, containing all I/O, data areas, and program areas. The I/O area is located at the lowest addresses, with the data area placed immediately above. The data area can be partitioned into register areas, stack areas, or direct access areas depending on the application. The program area is located at the opposite end of memory, closest to the highest addresses, and the highest part of this area is assigned to the tables of interrupt and reset vectors and vector call instructions. The following diagram shows the structure of memory space in the MB89530A series.

• Memory Map

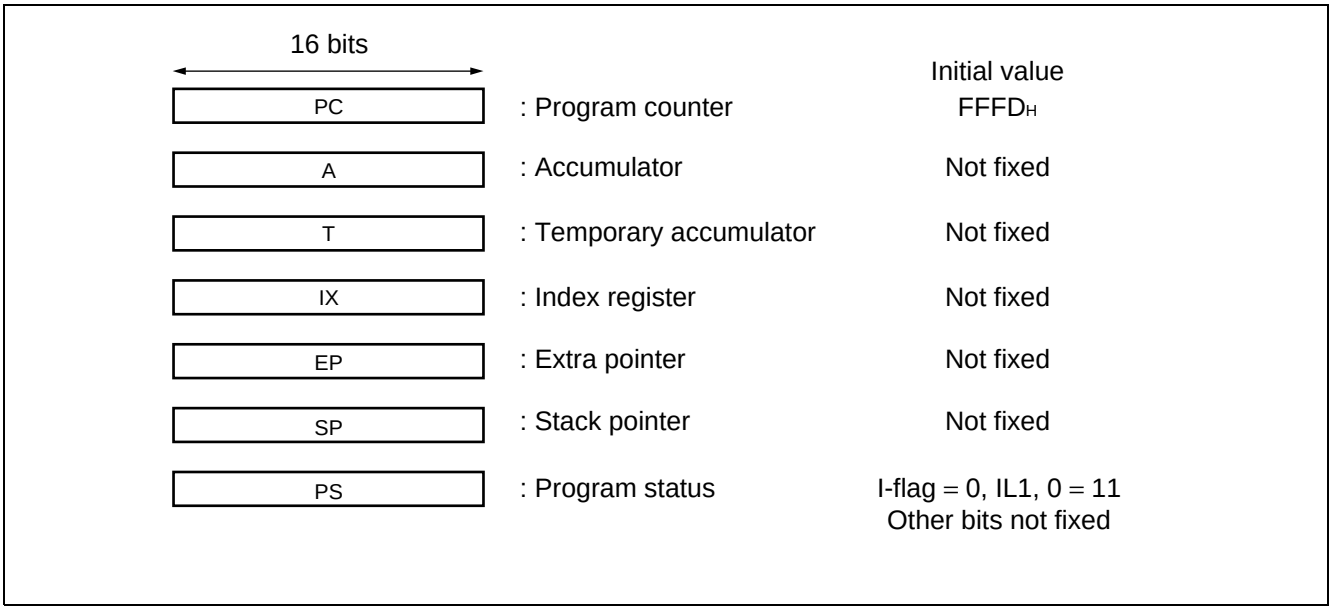


*1 : The external ROM area is on the MB89PV530 only.
*2 : Vector tables (reset, interrupt, vector call instructions)

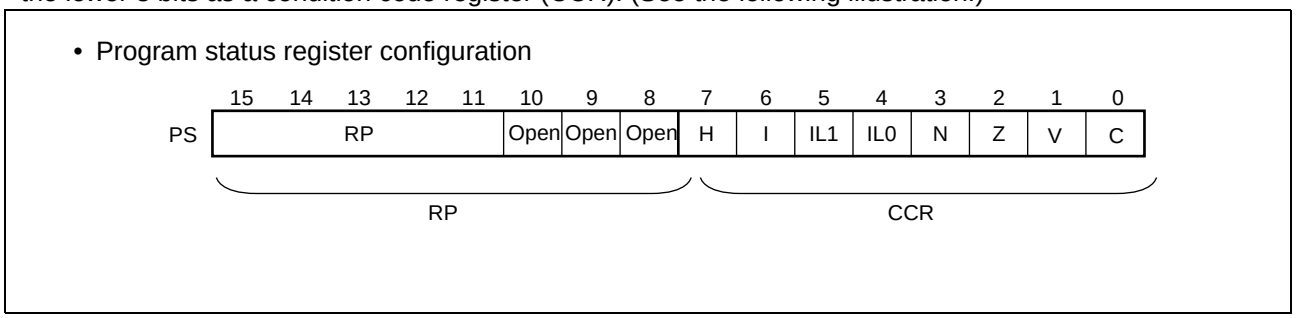
2. Registers

The F²MC-8L series has two types of registers, dedicated-use registers within the CPU, and general-purpose registers in memory.

Program counter (PC)	:	16-bit length, shows the location where instructions are stored.
Accumulator (A)	:	16-bit length, a temporary memory register for calculation operations. The lower byte is used for 8-bit data processing instructions.
Temporary accumulator (T)	:	16-bit length, performs calculations with the accumulator. The lower byte is used for 8-bit data processing instructions.
Index register (IX)	:	16-bit length, a register for index modification.
Extra pointer (EP)	:	16-bit length, a pointer indicating memory addresses.
Stack pointer (SP)	:	16-bit length, indicates stack areas.
Program status (PS)	:	16-bit length, contains register pointer and condition code.

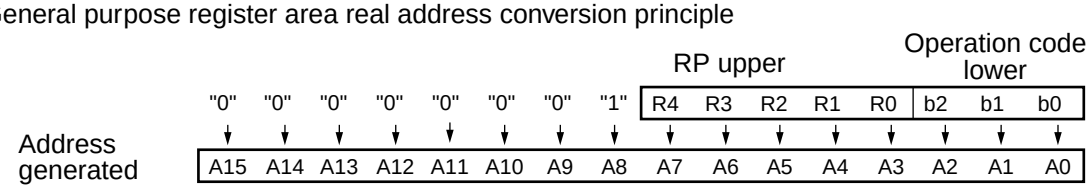


In addition, the PS register can be divided so that the upper 8 bits are used as a register bank pointer (RP), and the lower 8 bits as a condition code register (CCR). (See the following illustration.)



The RP register shows the address of the register bank currently being used, so that the RP value and the actual address are related by the conversion rule shown in the following illustration.

- General purpose register area real address conversion principle



The CCR register has bits that show the content of results of calculations and transferred data, and bits that control CPU operation during interrupts.

H-flag : Set to 1 if calculations result in carry or borrow operations from bit 3 to bit 4, otherwise set to 0.
This flag is used for decimal correction instructions.

I-flag : This flag is set to 1 if interrupts are enabled, and 0 if interrupts are prohibited.
The default value at reset is 0.

IL1, 0 : Indicates the level of the currently permitted interrupts.
Only interrupt requests having a more powerful level than the value of these bits will be processed.

IL1	IL0	Interrupt level	Strength
0	0	1	Strong ↕ Weak
0	1		
1	0	2	
1	1	3	

N-flag : Set to 1 if the highest bit is 1 after a calculation, otherwise cleared to 0.

Z-flag : Set to 1 if a calculation result is 0, otherwise cleared to 0.

V-flag : Set to 1 if a two's complement overflow results during a calculation, otherwise cleared to 0.

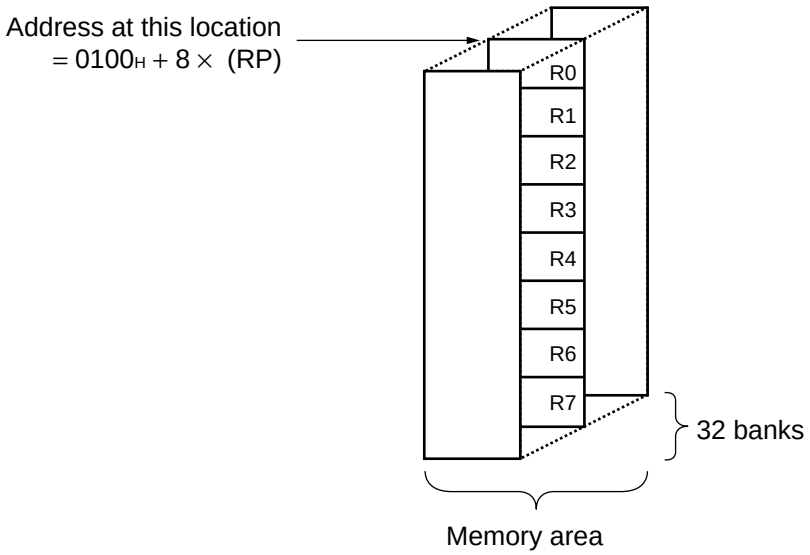
C-flag : Set to 1 if a calculation results in a carry or borrow operation from bit 7, otherwise cleared to 0.
This is also the shift-out value in a shift instruction.

In addition, the following general purpose registers are available.

General purpose registers: 8-bit length, used to contain data.

The general purpose registers are 8-bit registers located in memory. There are eight such registers per bank, and the MB89530A series have up to 32 banks for use. The bank currently in use is indicated by the register bank pointer (RP).

•Register bank configuration



■ I/O MAP

Address	Register name	Register description	Write/Read	Initial value
00H	PDR0	Port 0 data register	R/W	XXXXXXXXB
01H	DDR0	Port 0 direction register	W	00000000B
02H	PDR1	Port 1 data register	R/W	XXXXXXXXB
03H	DDR1	Port 1 direction register	W	00000000B
04H to 06H	(Reserved area)			
07H	SYCC	System clock control register	R/W	X-1MM100B
08H	STBC	Standby control register	R/W	00010---B
09H	WDTC	Watchdog control register	R/W	0---XXXXB
0AH	TBTC	Time base timer control register	R/W	00---000B
0BH	WPCR	Watch prescaler control register	R/W	00--0000B
0CH	PDR2	Port 2 data register	R/W	XXXXXXXXB
0DH	DDR2	Port 2 direction register	R/W	00000000B
0EH	PDR3	Port 3 data register	R/W	XXXXXXXXB
0FH	DDR3	Port 3 direction register	R/W	00000000B
10H	PDR4	Port 4 data register	R/W	XXXX11XXB
11H	DDR4	Port 4 direction register	R/W	0000--00B
12H	PDR5	Port 5 data register	R/W	11111111B
13H	PDR6	Port 6 data register	R	XXXXXXXXB
14H to 21H	(Reserved area)			
22H	SMC11	Serial mode control register 1 (UART)	R/W	00000000B
23H	SRC1	Serial rate control register (UART)	R/W	--011000B
24H	SSD1	Serial status and data register (UART)	R/W	00100-1XB
25H	SIDR1/ SODR1	Serial input/output data register (UART)	R/W	XXXXXXXXB
26H	SMC12	Serial mode control register 2 (UART)	R/W	--100001B
27H	CNTR1	PWM control register 1	R/W	00000000B
28H	CNTR2	PWM control register 2	R/W	000-0000B
29H	CNTR3	PWM control register 3	R/W	-000----B
2AH	COMR1	PWM compare register 1	W	XXXXXXXXB
2BH	COMR2	PWM compare register 2	W	XXXXXXXXB
2CH	PCR1	PWC pulse width control register 1	R/W	000--000B
2DH	PCR2	PWC pulse width control register 2	R/W	00000000B
2EH	RLBR	PWC reload buffer register	R/W	XXXXXXXXB
2FH	SMC21	Serial mode control register 1 (UART/SIO)	R/W	00000000B
30H	SMC22	Serial mode control register 2 (UART/SIO)	R/W	00000000B
31H	SSD2	Serial status and data register (UART/SIO)	R/W	00001---B
32H	SIDR2/ SODR2	Serial data register (UART/SIO)	R/W	XXXXXXXXB
33H	SRC2	Baud rate generator reload register	R/W	XXXXXXXXB

(Continued)

Address	Register name	Register description	Write/Read	Initial value
34H	ADC1	A/D control register 1	R/W	000000-0B
35H	ADC2	A/D control register 2	R/W	-0000001B
36H	ADDL	A/D data register low	R/W	XXXXXXXXB
37H	ADDH	A/D data register high	R/W	------00B
38H	PPGC2	PPG2 control register (12-bit PPG)	R/W	00000000B
39H	PRL22	PPG2 reload register 2 (12-bit PPG)	R/W	0X000000B
3AH	PRL21	PPG2 reload register 1 (12-bit PPG)	R/W	XX000000B
3BH	PRL23	PPG2 reload register 3 (12-bit PPG)	R/W	XX000000B
3CH	TMCR	16-bit timer control register	R/W	--000000B
3DH	TCHR	16-bit timer counter register high	R/W	00000000B
3EH	TCLR	16-bit timer counter register low	R/W	00000000B
3FH	EIC1	External interrupt 1 control register 1	R/W	00000000B
40H	EIC2	External interrupt 1 control register 2	R/W	00000000B
41H to 48H	(Reserved area)			
49H	DDCR	DDC select register	R/W	-------0B
4AH to 4BH	(Reserved area)			
4CH	PPGC1	PPG1 control register (12-bit PPG)	R/W	00000000B
4DH	PRL12	PPG1 reload register 2 (12-bit PPG)	R/W	0X000000B
4EH	PRL11	PPG1 reload register 1 (12-bit PPG)	R/W	XX000000B
4FH	PRL13	PPG1 reload register 3 (12-bit PPG)	R/W	XX000000B
50H	IACR	I²C address control register	R/W	-----000B
51H	IBSR	I²C bus status register	R	00000000B
52H	IBCR	I²C bus control register	R/W	00000000B
53H	ICCR	I²C clock control register	R/W	000XXXXXB
54H	IADR	I²C address register	R/W	-XXXXXXXB
55H	IDAR	I²C data register	R/W	XXXXXXXXB
56H	EIE2	External interrupt 2 control register	R/W	00000000B
57H	EIF2	External interrupt 2 flag register	R/W	-------0B
58H	RCR1	6-bit PPG control register 1	R/W	00000000B
59H	RCR2	6-bit PPG control register 2	R/W	0X000000B
5AH	CKR	Clock output control register	R/W	------00B
5BH to 6FH	(Reserved area)			
70H	SMR	Serial mode register (SIO)	R/W	00000000B
71H	SDR	Serial data register (SIO)	R/W	XXXXXXXXB
72H	PURR0	Port 0 pull-up resistance register	R/W	11111111B
73H	PURR1	Port 1 pull-up resistance register	R/W	11111111B
74H	PURR2	Port 2 pull-up resistance register	R/W	11111111B
75H	PURR3	Port 3 pull-up resistance register	R/W	11111111B
76H	PURR4	Port 4 pull-up resistance register	R/W	1111--11B
77H	WREN	Wild register enable register	R/W	--000000B

(Continued)

(Continued)

Address	Register name	Register description	Write/Read	Initial value
78H	WROR	Wild register data test register	R/W	--000000B
79H	PURR6	Port 6 pull-up resistance register	R/W	---11111B
7AH	FMCS	Flash memory control status resister	R/W	000000-0B
7BH	ILR1	Interrupt level setting register 1	W	11111111B
7CH	ILR2	Interrupt level setting register 2	W	11111111B
7DH	ILR3	Interrupt level setting register 3	W	11111111B
7EH	ILR4	Interrupt level setting register 4	W	11111111B
7FH	ITR	Interrupt test register	Access prohibited	XXXXXX00B
C80H	WRARH1	Upper address setting register 1	R/W	XXXXXXXX
C81H	WRARL1	Lower address setting register 1	R/W	XXXXXXXX
C82H	WRDR1	Data setting register 1	R/W	XXXXXXXX
C83H	WRARH2	Upper address setting register 2	R/W	XXXXXXXX
C84H	WRARL2	Lower address setting register 2	R/W	XXXXXXXX
C85H	WRDR2	Data setting register 2	R/W	XXXXXXXX
C86H	WRARH3	Upper address setting register 3	R/W	XXXXXXXX
C87H	WRARL3	Lower address setting register 3	R/W	XXXXXXXX
C88H	WRDR3	Data setting register 3	R/W	XXXXXXXX
C89H	WRARH4	Upper address setting register 4	R/W	XXXXXXXX
C8AH	WRARL4	Lower address setting register 4	R/W	XXXXXXXX
C8BH	WRDR4	Data setting register 4	R/W	XXXXXXXX
C8CH	WRARH5	Upper address setting register 5	R/W	XXXXXXXX
C8DH	WRARL5	Lower address setting register 5	R/W	XXXXXXXX
C8EH	WRDR5	Data setting register 5	R/W	XXXXXXXX
C8FH	WRARH6	Upper address setting register 6	R/W	XXXXXXXX
C90H	WRARL6	Lower address setting register 6	R/W	XXXXXXXX
C91H	WRDR6	Data setting register 6	R/W	XXXXXXXX

- Description of write/read symbols :

R/W : read/write enabled
R : Read only
W : Write only

- Description of initial values :

0 : This bit initialized to “0”.
1 : This bit initialized to “1”.
X : The initial value of this bit is not determined.
M : The initial value of this bit is a mask option.
- : This bit is not used.

Note : Do not use reserved spaces.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AVss = Vss = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}, AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	MB89535A/537A/538A* MB89537AC/538AC MB89F538/P538 MB89PV530
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Other than P42, P43
		V_{SS} – 0.3	V_{SS} + 6.0	V	P42, P43
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	Other than P42, P43
		V_{SS} – 0.3	V_{SS} + 6.0	V	P42, P43
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating duty)
“L” level maximum total output current	ΣI_{OL}	—	100	mA	
“L” level average total output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating duty)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating duty)
“H” level maximum total output current	ΣI_{OH}	—	–50	mA	
“H” level average total output current	ΣI_{OHAV}	—	–20	mA	Average value (operating current × operating duty)
Current consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : AVcc and Vcc are to be used at the same potential. AVR should not exceed AVcc + 0.3V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

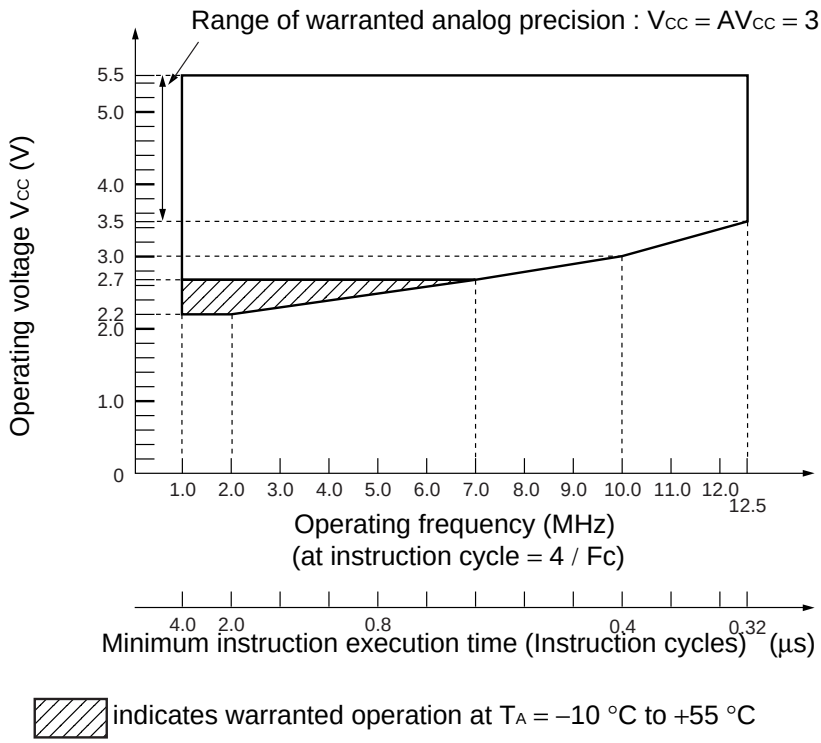
2. Recommended Operating Conditions

(AVss = Vss = 0 V)

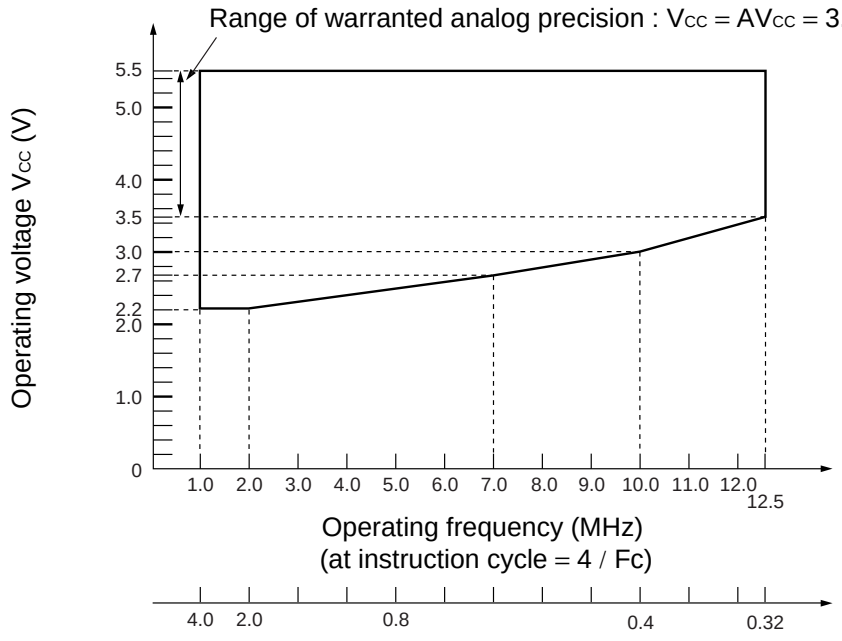
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Supply voltage	V_{CC}, AV_{CC}	2.2*	5.5	V	Range warranted for normal operation	MB89535A MB89537A/538A MB89537AC/ 538AC
		1.5	5.5	V	RAM status in stop mode	
		2.7*	5.5	V	Range warranted for normal operation	MB89P538 MB89PV530
		1.5	5.5	V	RAM status in stop mode	
		3.5	5.5	V	Range warranted for normal operation	MB89F538
		3.0	5.5	V	RAM status in stop mode	
	AVR	3.5	AV_{CC}	V		
Operating temperature	T_A	–40	+85	°C		

* : Varies according to frequency used, and instruction cycle.
See “Operating voltage vs. operating frequency ” and “5. A/D Converter Electrical Characteristics”.

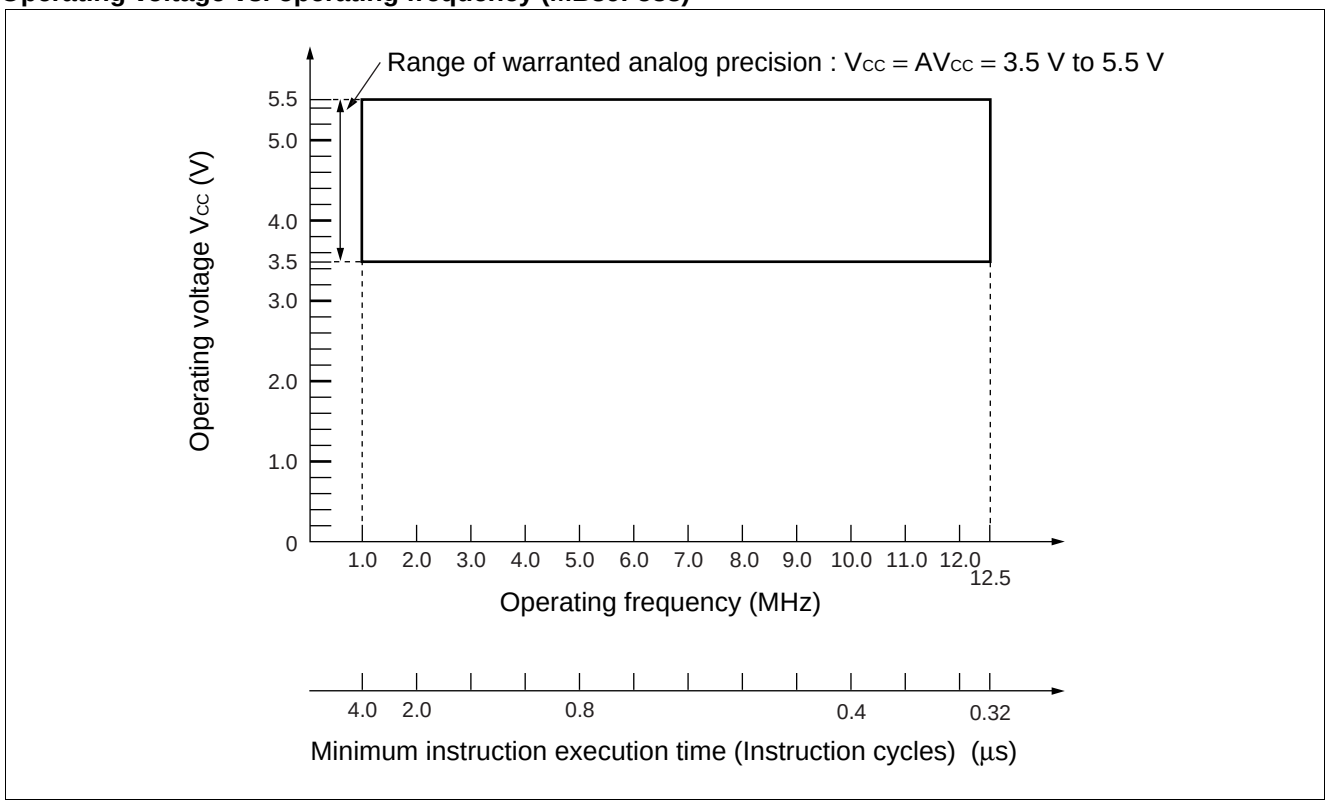
Operating voltage vs. operating frequency (MB89P538/MB89PV530)



Operating voltage vs. operating frequency (MB89535A/537A/538A/537AC/538AC)



Operating voltage vs. operating frequency (MB89F538)



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(1) Supply Voltage at 5.0 (V)

($AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0$ V, $T_A = -40$ °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, SI1, SI2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, INT20 to INT27, UCK1, UI1, INT10 to INT13, SCK1, EC, PWCK, PWC, SCK2, UCK2, UI2, ADST	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHSMB}	SCL, SDA	—	V_{SS} + 1.4	—	V_{SS} + 5.5	V	With SMB input buffer selected*
	V_{IHI2C}		—	0.7 V_{CC}	—	V_{SS} + 5.5	V	With I^2C input buffer selected*
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, SI1, SI2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, INT20 to INT27, UCK1, UI1, INT10 to INT13, SCK1, EC, PWCK, PWC, SCK2, UCK2, UI2, ADST	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILSMB}	SCL, SDA	—	V_{SS} – 0.3	—	V_{SS} + 0.6	V	With SMB input buffer selected*
	V_{ILI2C}		—	V_{SS} – 0.3	—	0.3 V_{CC}	V	With I^2C input buffer selected*
Open drain output applied voltage	V_{D1}	P50 to P57	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
	V_{D2}	P42, P43				V_{SS} + 5.5	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40, P41, P44 to P47	I_{OH} = –2.0 mA	4.0	—	—	V	
		P25 to P27	I_{OH} = –3.0 mA					
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	

(Continued)

($AV_{CC} = V_{CC} = 5.0$ V, $AVss = Vss = 0$ V, $T_A = -40$ °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current (Hi-Z output leak current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	$0.0 V < V_I < V_{CC}$	–5	—	+5	µA	With no pull-up resistance specified
Open drain output leak current	I_{LIOD}	P42, P43	$0.0 V < V_I < V_{SS} + 5.5 V$	—	—	+5	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40, P41, P44 to P47, P60 to P64, $\overline{RST}$	$V_I = 0.0$ V	25	40	100	kΩ	With pull-up resistance specified. The $\overline{RST}$ signal is excluded.
Supply current	I_{CC1}	V_{CC}	$F_{CH} = 10.0$ MHz, $V_{CC} = 5.0$ V, $t_{inst} = 0.4$ µs	—	15	20	mA	MB89P538/ PV530
				—	6	10	mA	MB89F538
				—	8	13	mA	MB89535A/7A/8A MB89537AC/ 538AC
	I_{CC2}		$F_{CH} = 10.0$ MHz, $V_{CC} = 5.0$ V, $t_{inst} = 6.4$ µs	—	5	8.5	mA	MB89P538/ PV530
				—	1.5	3	mA	MB89F538
				—	1.5	3	mA	MB89535A/7A/8A MB89537AC/ 538AC
	I_{CCS1}		$F_{CH} = 10.0$ MHz, $V_{CC} = 5.0$ V, $t_{inst} = 0.4$ µs	—	5	7	mA	Sleep mode MB89P538/ PV530
				—	3	5	mA	Sleep mode MB89F538
				—	2.5	5	mA	Sleep mode MB89535A/7A/8A MB89537AC/ 538AC
	I_{CCS2}		$F_{CH} = 10.0$ MHz, $V_{CC} = 5.0$ V, $t_{inst} = 6.4$ µs	—	1.5	3	mA	Sleep mode MB89P538/ PV530
				—	1	2	mA	Sleep mode MB89F538
				—	1	2	mA	Sleep mode MB89535A/7A/8A MB89537AC/ 538AC

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Supply current	I_{CCL}	V_{CC}	F_{CL} = 32.768 kHz, V_{CC} = 5.0 V, T_A = +25 °C	—	3	7	mA	Sub mode MB89P538/ PV530
				—	400	800	µA	Sub mode MB89F538
				—	50	85	µA	Sub mode MB89535A/7A/8A MB89537AC/ 538AC
	I_{CCLS}		F_{CL} = 32.768 kHz, V_{CC} = 5.0 V, T_A = +25 °C	—	30	50	µA	Sub, sleep mode MB89P538/ PV530
				—	15	30	µA	Sub, sleep mode MB89F538
				—	15	30	µA	Sub, sleep mode MB89535A/7A/8A MB89537AC/ 538AC
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 5.0 V, T_A = +25 °C	—	5	15	µA	Watch mode, main stop
	I_{CCH}		T_A = +25 °C	—	3	10	µA	Sub, stop modes
	I_A	AV_{CC}	F_{CH} = 10.0 MHz	—	4	6	mA	A/D conversion running
	I_{AH}		T_A = +25 °C	—	1	5	µA	A/D stopped
Input capacitance	C_{IN}	Except V_{CC}, V_{SS}, AV_{CC}, AV_{SS}	f = 1 MHz	—	5	15	pF	

* : The MB89PV530/P538/537AC/538AC have a built-in I^2C function, and a choice of input buffers by software setting. MB89535A/537A/538A have no built-in I2C functions, and therefore this standard does not apply.

(2) Supply Voltage at 3.0 (V) (except MB89F538)

(AV_{CC} = V_{CC} = 3.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, SI1, SI2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, INT20 to INT27, UCK1, UI1, INT10 to INT13, SCK1, EC, PWCK, PWC, SCK2, UCK2, UI2, ADST	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHSMB}	SCL, SDA	—	V_{SS} + 1.4	—	V_{SS} + 5.5	V	With SMB input buffer selected*
	V_{IHI2C}		—	0.7 V_{CC}	—	V_{SS} + 5.5	V	With I^2C input buffer selected*
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, SI1, SI2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, INT20 to INT27, UCK1, UI1, INT10 to INT13, SCK1, EC, PWCK, PWC, SCK2, UCK2, UI2, ADST	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILSMB}	SCL, SDA	—	V_{SS} – 0.3	—	V_{SS} + 0.6	V	With SMB input buffer selected*
	V_{ILI2C}		—	V_{SS} – 0.3	—	0.3 V_{CC}	V	With I^2C input buffer selected*
Open drain output applied voltage	V_{D1}	P50 to P57	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
	V_{D2}	P42, P43				V_{SS} + 5.5	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40, P41, P44 to P47	I_{OH} = –2.0 mA	2.4	—	—	V	
		P25 to P27	I_{OH} = –3.0 mA					
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 3.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current (Hi-Z output leak current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	0.0 V < V_I < V_{CC}	–5	—	+5	µA	With no pull-up resistance specified
Open drain output leak current	I_{LIOD}	P42, P43	0.0 V < V_I < V_{SS} + 5.5 V	—	—	+5	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40, P41, P44 to P47, P60 to P64, $\overline{RST}$	V_I = 0.0 V	25	70	100	kΩ	With pull-up resistance specified. The $\overline{RST}$ signal is excluded.
Supply current	I_{CC1}	V_{CC}	F_{CH} = 10.0 MHz t_{inst} = 0.4 µs	—	6	10	mA	
	I_{CC2}		F_{CH} = 10.0 MHz t_{inst} = 6.4 µs	—	1.5	3	mA	
	I_{CCS1}		F_{CH} = 10.0 MHz t_{inst} = 0.4 µs	—	2	4	mA	Sleep mode
	I_{CCS2}		F_{CH} = 10.0 MHz t_{inst} = 6.4 µs	—	1	2	mA	Sleep mode
	I_{CCL}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V T_A = +25 °C	—	1	3	mA	Sub modes MB89P538/ PV530
				—	20	50	µA	Sub modes MB89535A/7A/ 8A MB89537AC/ 538AC
	I_{CCLS}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V T_A = +25 °C	—	15	30	µA	Sub, sleep modes
	I_{CCT}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V T_A = +25 °C	—	5	15	µA	Watch mode, main stop
	I_{CCH}		T_A = +25 °C	—	1	5	µA	Sub, stop modes
	I_A	AV_{CC}	F_{CH} = 10.0 MHz	—	1	3	mA	A/D conversion running
	I_{AH}		T_A = +25 °C	—	1	5	µA	A/D stopped
Input capacitance	C_{IN}	Except V_{CC}, V_{SS}, AV_{CC}, AV_{SS}	f = 1 MHz	—	5	15	pF	

* : The MB89PV530/P538/537AC/538AC have a built-in I^2C function, and a choice of input buffers by software setting. MB89535A/537A/538A have no built-in I2C functions, and therefore this standard does not apply.

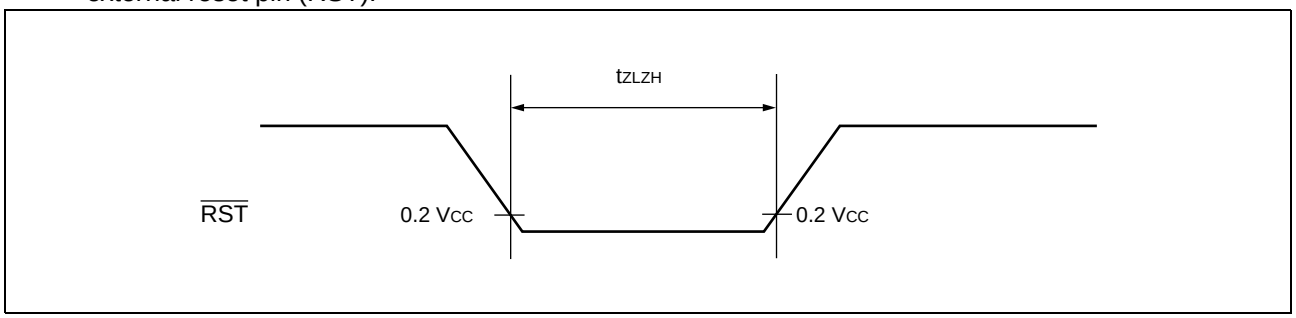
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

Notes: • t_{HCYL} is the main clock oscillator period.
• If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).

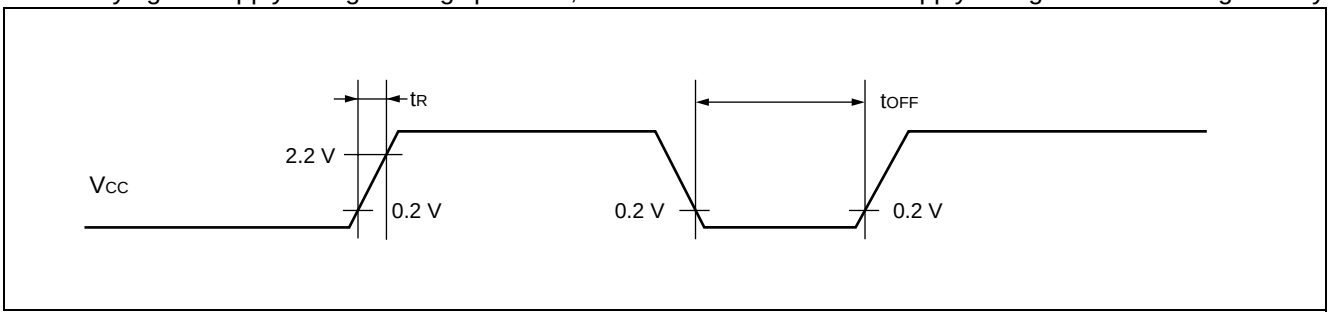


(2) Power-on Reset

(AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power on time	t_R	—	0.5	50	ms	
Power shutoff time	t_{OFF}	—	1	—	ms	For repeated operation

Note : Be sure that the power supply will come on within the selected oscillator stabilization period. Also, when varying the supply voltage during operation, it is recommended that the supply voltage be increased gradually.

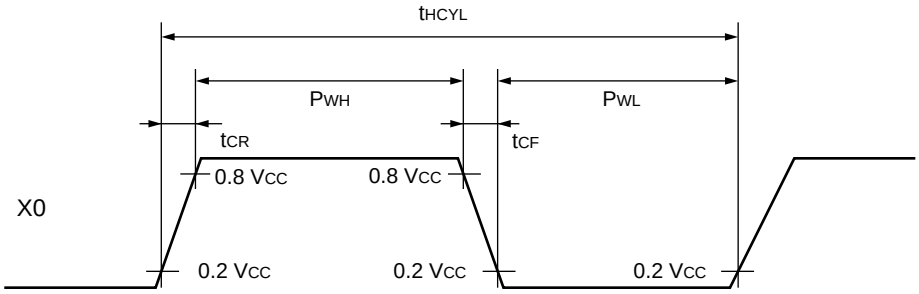


(3) Clock Timing Standards

(AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

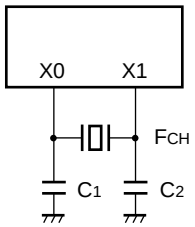
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	12.5	MHz	Main clock
	F_{CL}	X0A, X1A		—	32.768	—	kHz	Sub clock
Clock cycle time	t_{HCYL}	X0, X1		80	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	Sub clock
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WHH} P_{WLL}	X0A		—	15.2	—	µs	External clock
Input clock rise, fall time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

• X0, X1 timing and application conditions

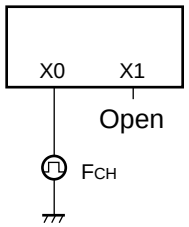


• Clock application conditions

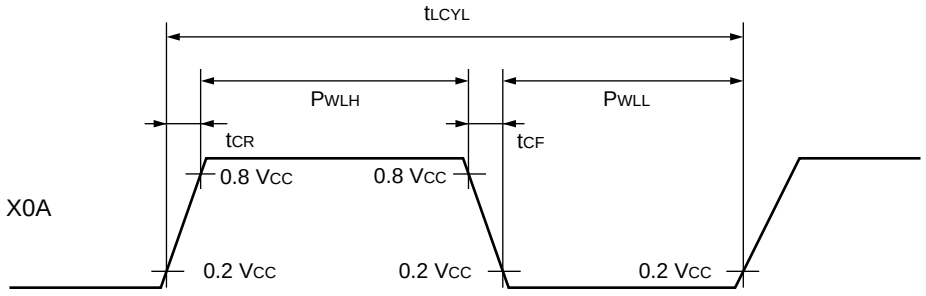
Using a crystal oscillator
or
ceramic oscillator



Using an external clock
signal

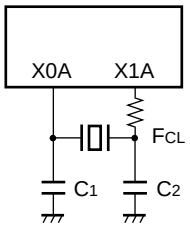


• X0A, X1A timing and application conditions

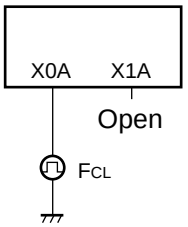


• Clock application conditions

Using a crystal oscillator
or
ceramic oscillator



Using an external clock
signal



(4) Instruction Cycle

(AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Rated value	Unit	Remarks
Instruction cycle (minimum instruction execution time)	t_{inst}	4/F_{CH}, 8/F_{CH}, 16/F_{CH}, 64/F_{CH}	µs	Operating at F_{CH} = 12.5 MHz (4/F_{CH}) t_{inst} = 0.32 µs
		2/F_{CL}	µs	Operating at F_{CL} = 32.768 kHz t_{inst} = 61.036 µs

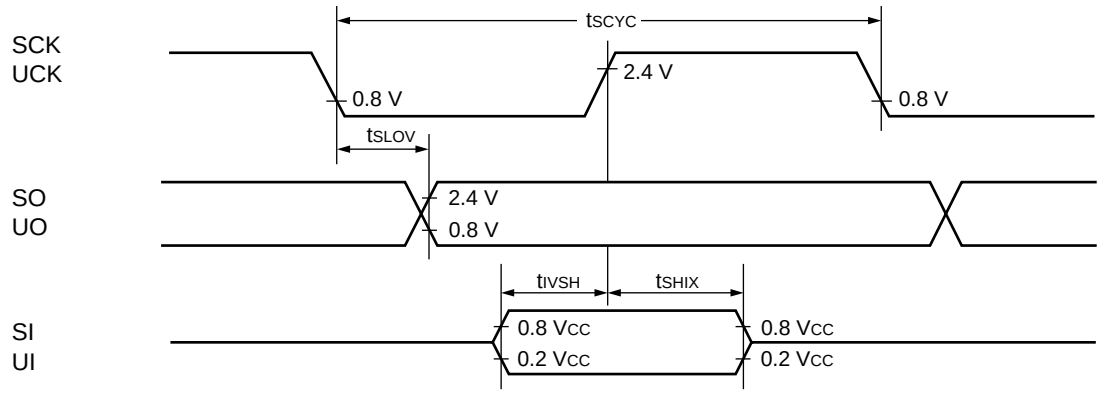
(5) Serial I/O Timing

(V_{CC} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

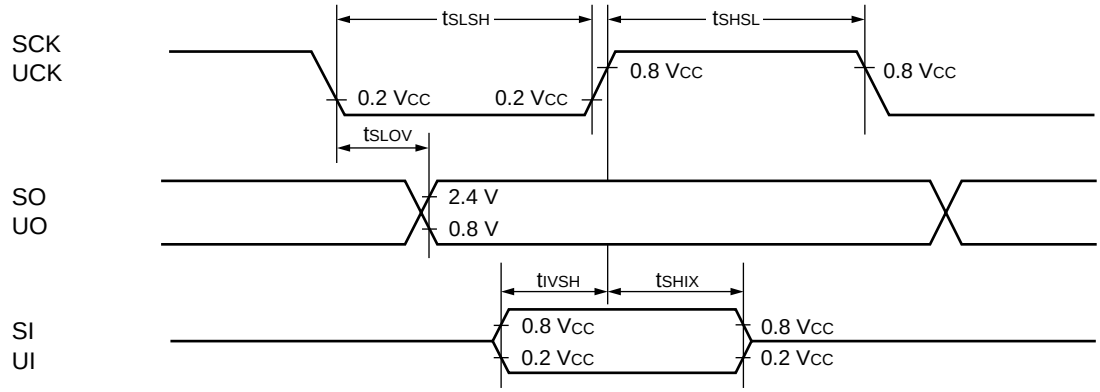
Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK, UCK	Internal clock operation	2 t_{inst}	—	µs	
SCK↓→SO	t_{SLOV}	SCK, SO, UCK, UO		–200	+200	ns	
Valid SI→SCK↑	t_{IVSH}	SI, SCK, UI, UCK		200	—	ns	
SCK↑→valid SI hold time	t_{SHIX}	SCK, SI, UCK, UI		200	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK, UCK	External clock operation	1 t_{inst}	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}	—	µs	
SCK↓→SO time	t_{SLOV}	SCK, SO, UCK, UO		0	200	ns	
Valid SI→SCK↑	t_{IVSH}	SI, SCK, UI, UCK		200	—	ns	
SCK↑→ valid SI hold time	t_{SHIX}	SCK, SI, UCK, UI		200	—	ns	

Note : For t_{inst} see “ (4) Instruction Cycle”.

Internal shift clock mode



External shift clock mode

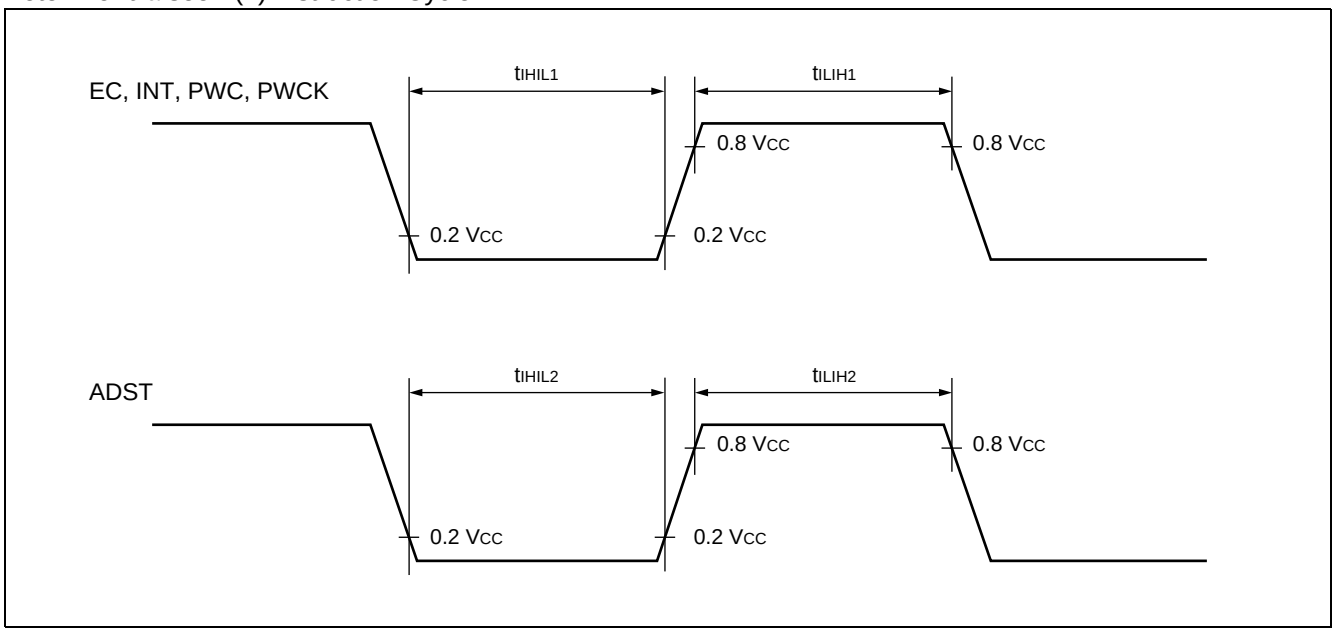


(6) Peripheral Input Timing

(V_{CC} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Peripheral input "H" level pulse width 1	t_{ILIH1}	INT10 to INT13, INT20 to INT27, EC, PWC, PWCK	—	2 t_{inst}	—	µs	
Peripheral input "L" level pulse width 1	t_{IHIL1}		—	2 t_{inst}	—	µs	
Peripheral input "H" level pulse width 2	t_{ILIH2}	ADST	—	2^8 t_{inst}	—	µs	
Peripheral input "L" level pulse width 2	t_{IHIL2}		—	2^8 t_{inst}	—	µs	

Note : For t_{inst} see " (4) Instruction Cycle".



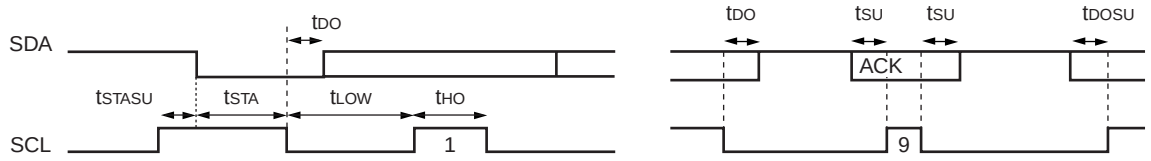
(7) I²C Timing

(V_{CC} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

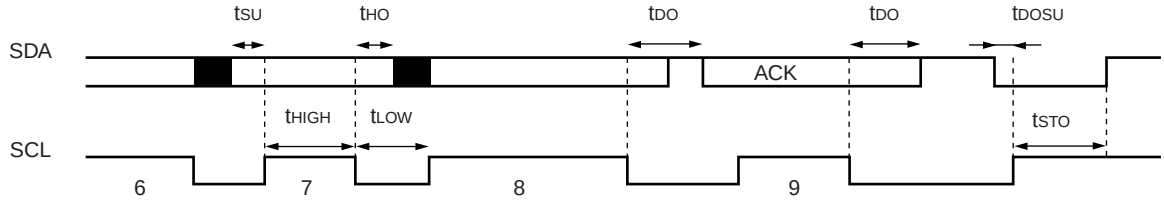
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Start condition output	t_{STA}	SCL SDA	—	$1 / 4\ t_{inst} \times m \times n - 20$	$1 / 4\ t_{inst} \times m \times n + 20$	ns	Master only
Stop condition output	t_{STO}	SCL SDA	—	$1 / 4\ t_{inst} \times (m \times n + 8) - 20$	$1 / 4\ t_{inst} \times (m \times n + 8) + 20$	ns	Master only
Start condition detection	t_{STA}	SCL SDA	—	$1 / 4\ t_{inst} \times 6 + 40$	—	ns	
Stop condition detection	t_{STO}	SCL SDA	—	$1 / 4\ t_{inst} \times 6 + 40$	—	ns	
Restart condition output	t_{STASU}	SCL SDA	—	$1 / 4\ t_{inst} \times (m \times n + 8) - 20$	$1 / 4\ t_{inst} \times (m \times n + 8) + 20$	ns	Master only
Restart condition detection	t_{STASU}	SCL SDA	—	$1 / 4\ t_{inst} \times 4 + 40$	—	ns	
SCL output “L” width	t_{LOW}	SCL	—	$1 / 4\ t_{inst} \times m \times n - 20$	$1 / 4\ t_{inst} \times m \times n + 20$	ns	Master only
SCL output “H” width	t_{HIGH}	SCL	—	$1 / 4\ t_{inst} \times (m \times n + 8) - 20$	$1 / 4\ t_{inst} \times (m \times n + 8) + 20$	ns	Master only
SDA output delay time	t_{DO}	SDA	—	$1 / 4\ t_{inst} \times 4 - 20$	$1 / 4\ t_{inst} \times 4 + 20$	ns	
Setup after SDA output interrupt interval	t_{DOSU}	SDA	—	$1 / 4\ t_{inst} \times 4 - 20$	—	ns	
SCL input “L” width	t_{LOW}	SCL	—	$1 / 4\ t_{inst} \times 6 + 40$	—	ns	
SCL input “H” width	t_{HIGH}	SCL	—	$1 / 4\ t_{inst} \times 2 + 40$	—	ns	
SDA input setup	t_{SU}	SDA	—	40	—	ns	
SDA input hold	t_{HO}	SDA	—	0	—	ns	

Notes :
- For t_{inst} see “ (4) Instruction Cycle”.
- The value “m” in the above table is the value from the shift clock frequency setting bits (CS4-CS3) in the clock control register “ICCR”. For details, refer to the register description in the hardware manual.
- The value ’n’ in the above table is the value from the shift clock frequency setting bits (CS2-CS0) in the clock control register “ICCR”. For details, refer to the register description in the hardware manual.
- t_{DOSU} appears when the interrupt period is longer than the SCL “L” width.
- The rated values for SDA and SCL assume a start up time of 0 ns.

• I²C interface [Data sending (master/slave)]



• I²C interface [Data receiving (master/slave)]



5. A/D Converter Electrical Characteristics

(1) MB89535A/537A/537AC/538A/538AC/P538/PV538

(V_{CC} = 3.5 V to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution capability	—	—	—	—	—	10	bit	AV_{CC} = V_{CC}
Total error			AVR = AV_{CC}	—	—	±3.0	LSB	
Linear error				—	—	±2.5	LSB	
Differential linear error				—	—	±1.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full scale transition voltage	V_{FST}			AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	
Inter-channel variation	—			—	—	4.0	LSB	
Conversion time	—		—	—	60 t_{inst}	—	µs	*
Sampling time				—	16 t_{inst}	—	µs	
Analog input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	V_{AIN}			0	—	AVR	V	
Reference voltage	—	AVR		AV_{SS} + 3.5	—	AV_{CC}	V	
Reference voltage supply current	I_R		A/D running	—	400	—	µA	
	I_{RH}		A/D off	—	—	5	µA	

* : Includes sampling time.

Note : For t_{inst} see “ (4) Instruction Cycle”.

(2) MB89F538

(V_{CC} = 3.5 V to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution capability	—	—	—	—	—	10	bit	AV_{CC} = V_{CC}
Total error			AVR = AV_{CC}	—	—	±5.0	LSB	
Linear error				—	—	±2.5	LSB	
Differential linear error				—	—	±1.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 4.5 LSB	mV	
Full scale transition voltage	V_{FST}			AVR – 6.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	
Inter-channel variation	—			—	—	4.0	LSB	
Conversion time	—		—	—	60 t_{inst}	—	µs	*
Sampling time				—	16 t_{inst}	—	µs	
Analog input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	V_{AIN}			0	—	AVR	V	
Reference voltage	—	AVR		AV_{SS} + 3.5	—	AV_{CC}	V	
Reference voltage supply current	I_R		A/D running	—	400	—	µA	
	I_{RH}		A/D off	—	—	5	µA	

* : Includes sampling time.

Note : For t_{inst} see “ (4) Instruction Cycle”.

(3) A/D Converter Terms and Definitions

- **Resolution**

The level of analog variation that can be distinguished by the A/D converter.

- **Linear error (unit : LSB)**

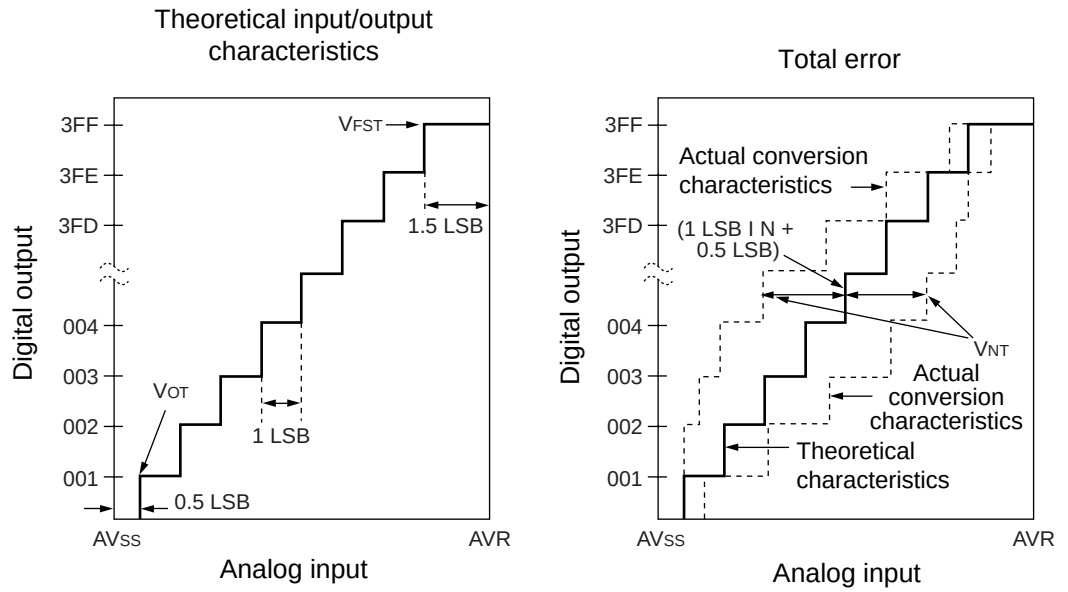
The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000”←→“00 0000 0001”) of a device and the full-scale transition point (“11 1111 1110”←→“11 1111 1111”) , compared with the actual conversion values obtained.

- **Differential linear error (Unit : LSB)**

The deviation from the theoretical input voltage required to produce a change of 1 LSB in output code.

- **Total error (Unit : LSB)**

The difference between theoretical conversion value and actual conversion value.



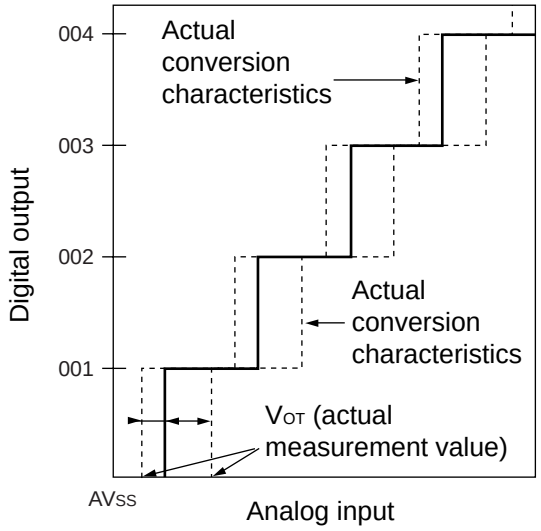
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{(V)}$$

$$\text{Total error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

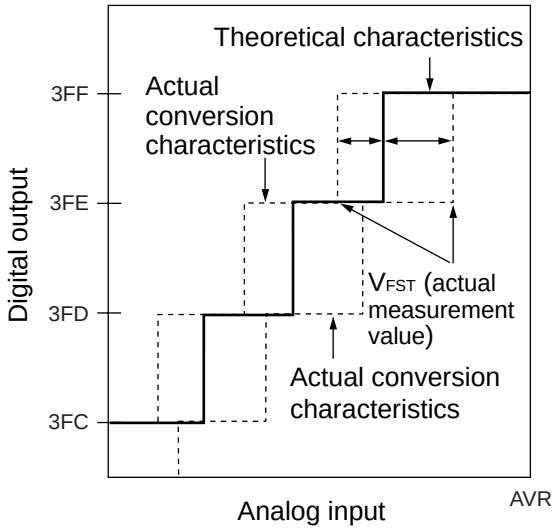
(Continued)

(Continued)

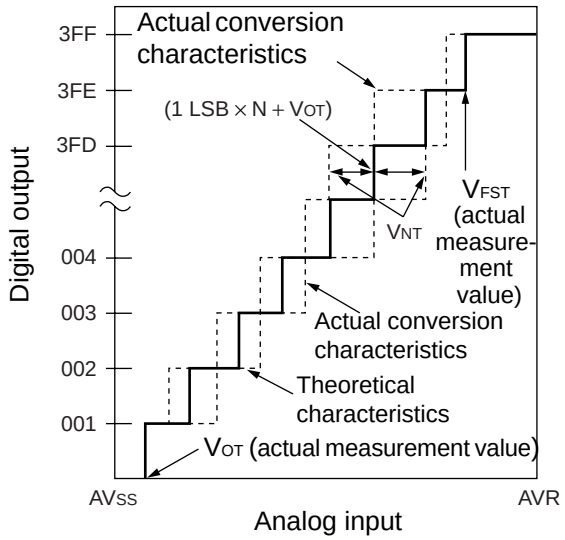
Zero transition error



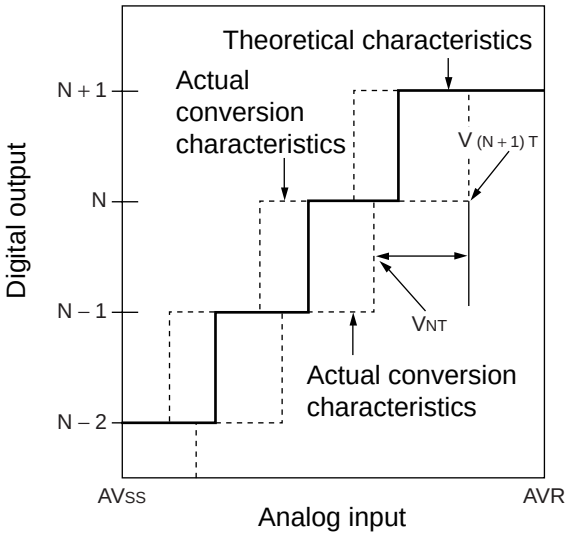
Full-scale transition error



Linear error



Differential linear error



$$\text{Analog input linear error in digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

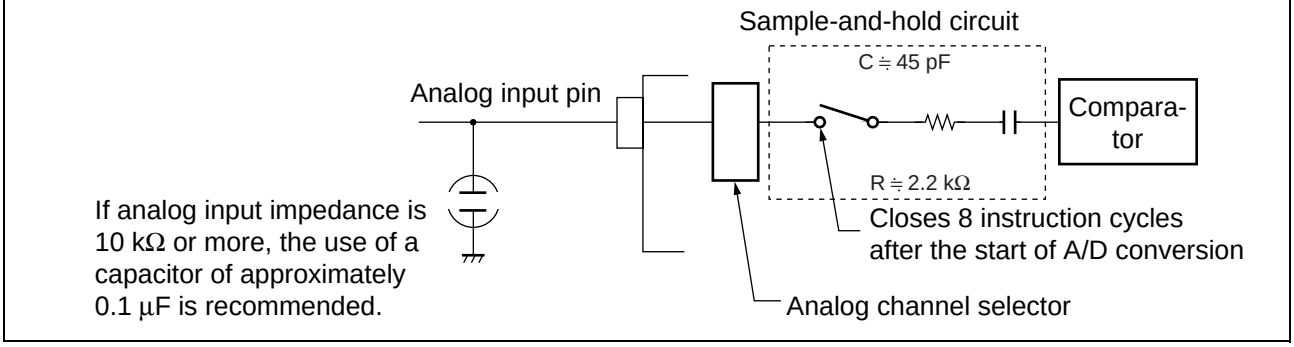
$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

(4) Precautionary Information

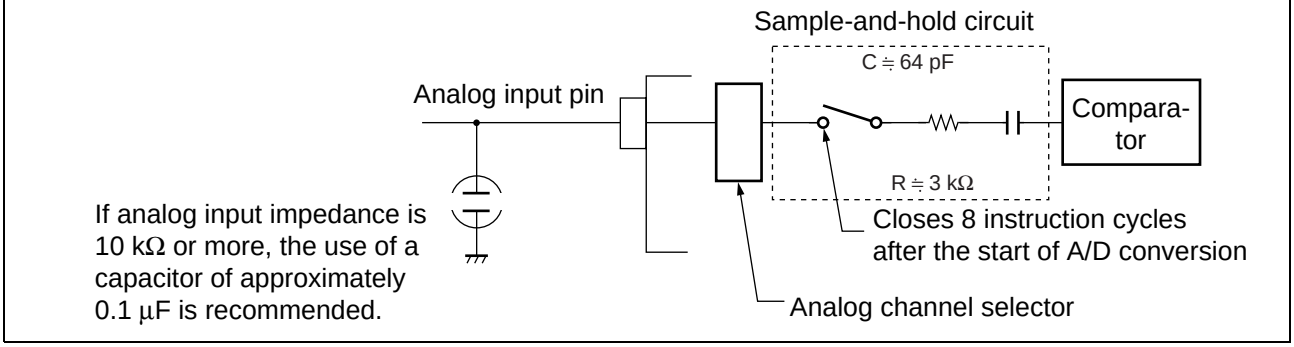
• Input Impedance of Analog Input Pins

The A/D converter of MB89530A has a sample & hold circuit as shown below, which uses a sample-and-hold capacitor to obtain the voltage at the analog input pin for 8 instruction cycles following the start of A/D conversion. For this reason if the external circuits providing the analog input signal have high output impedance, the analog input voltage may not stabilize within the analog input sampling time. It is therefore recommended that the output impedance of external circuits be reduced to 10 kΩ or less.

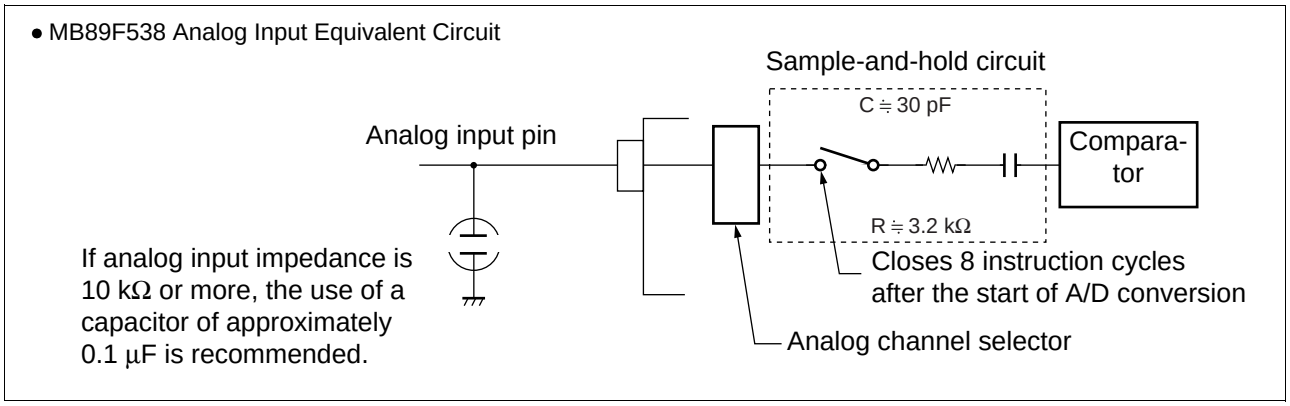
• MB89535A/537A/537AC/538A/538AC Analog Input Equivalent Circuit



• MB89P538 and MB89PV530 Analog Input Equivalent Circuit



• MB89F538 Analog Input Equivalent Circuit

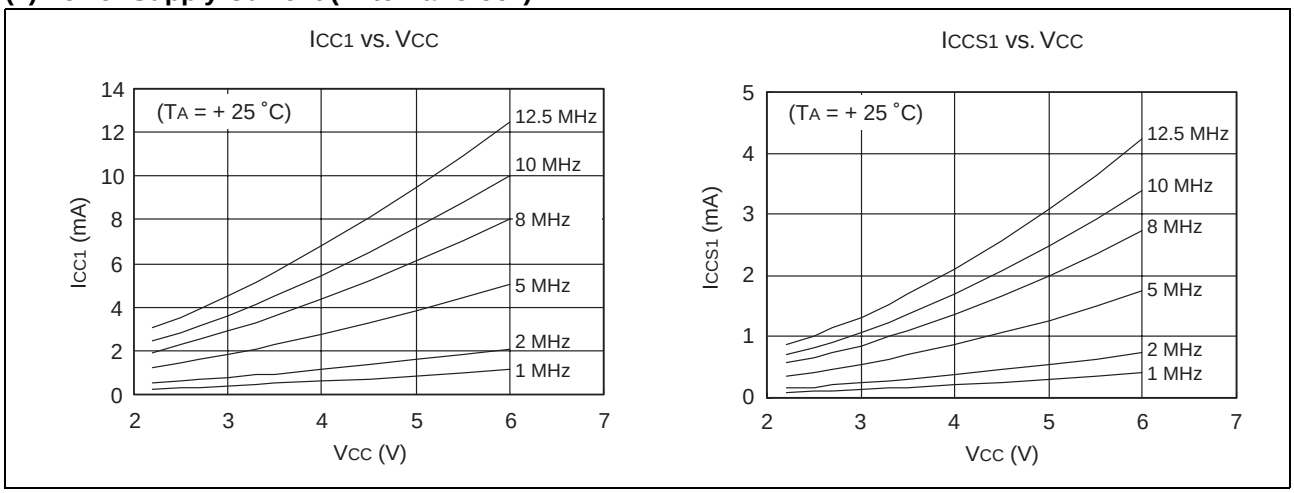


• About error

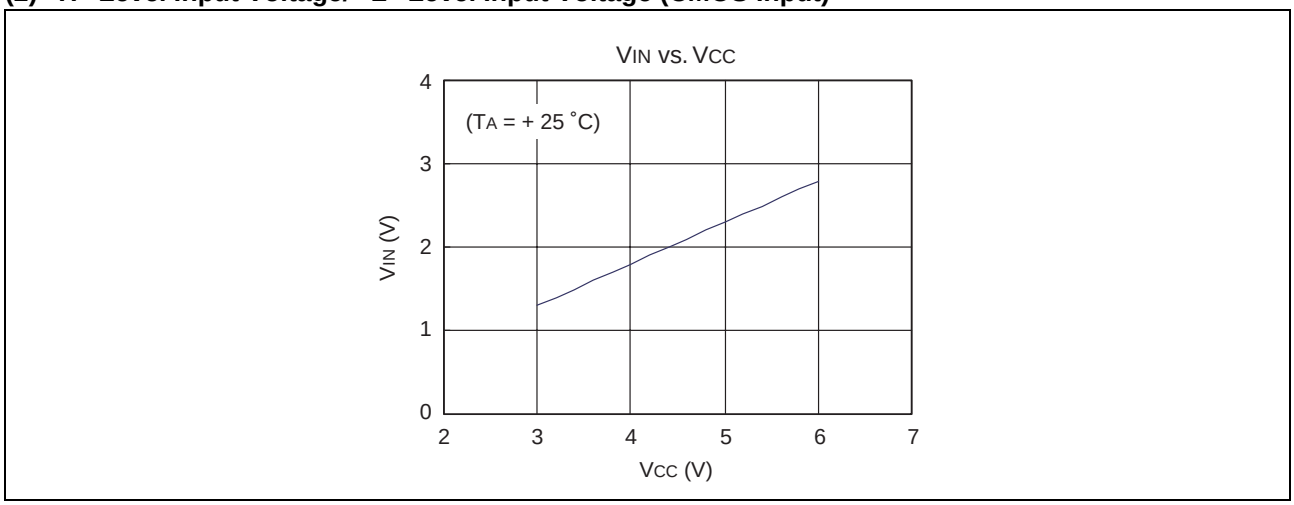
The smaller the absolute value |AVR - AVss| is, the greater the relative error becomes.

■ EXAMPLE CHARACTERISTICS (MB89538A)

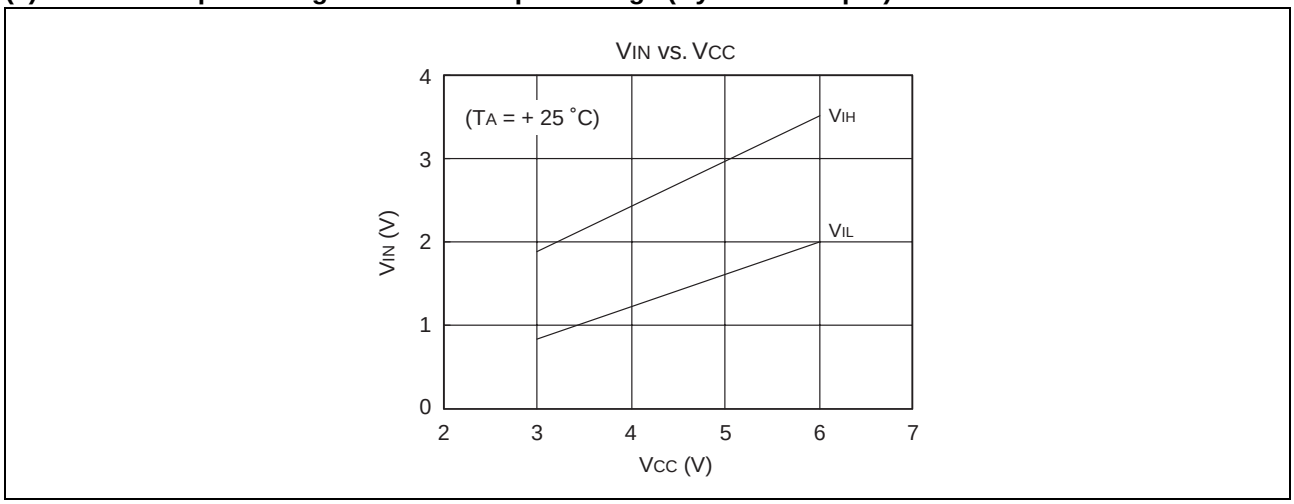
(1) Power Supply Current (External Clock)



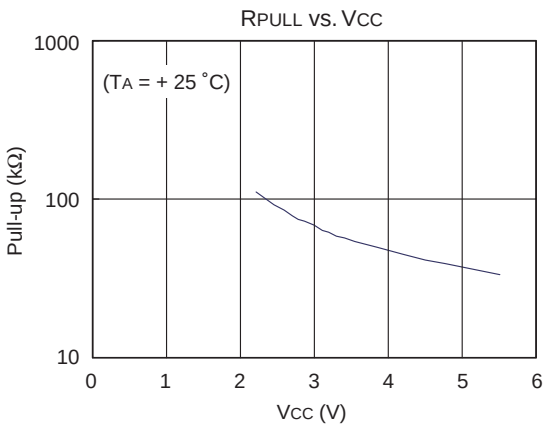
(2) "H" Level Input Voltage/ "L" Level Input Voltage (CMOS Input)



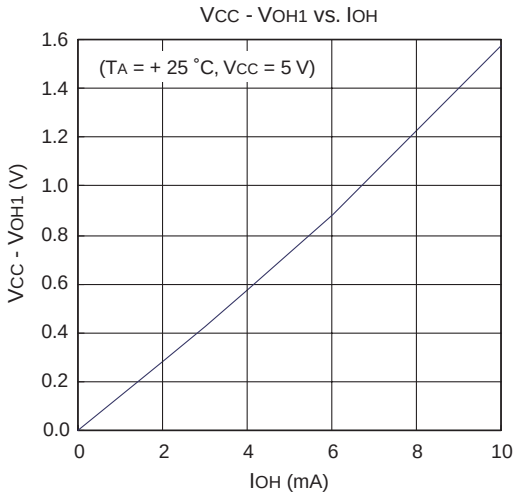
(3) "H" Level Input Voltage / "L" Level Input Voltage (Hysteresis Input)

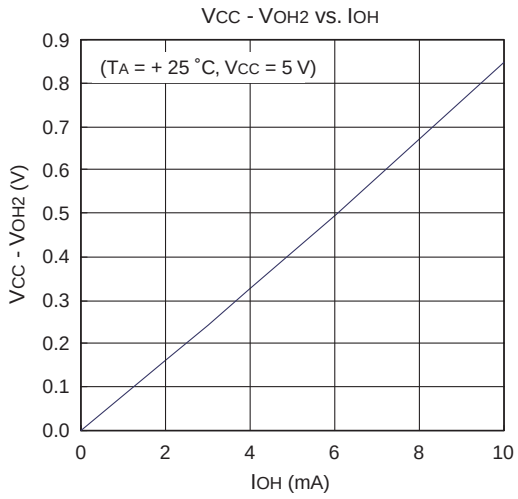


(4) Pull-up Resistor Value

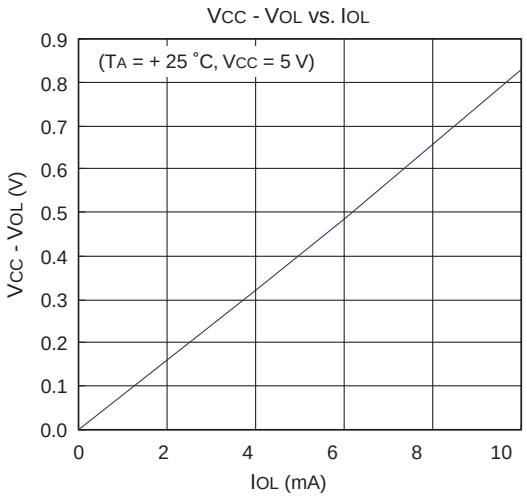


(5) "H" Level Output Voltage

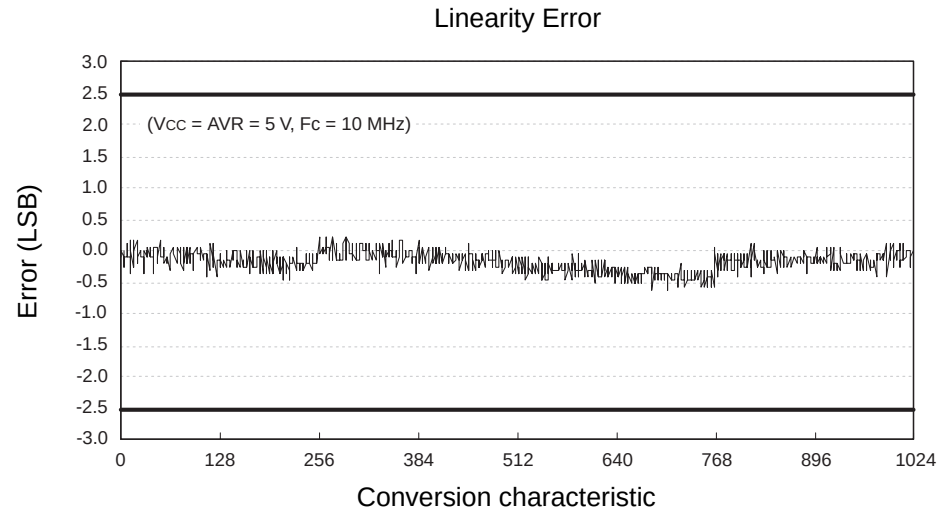


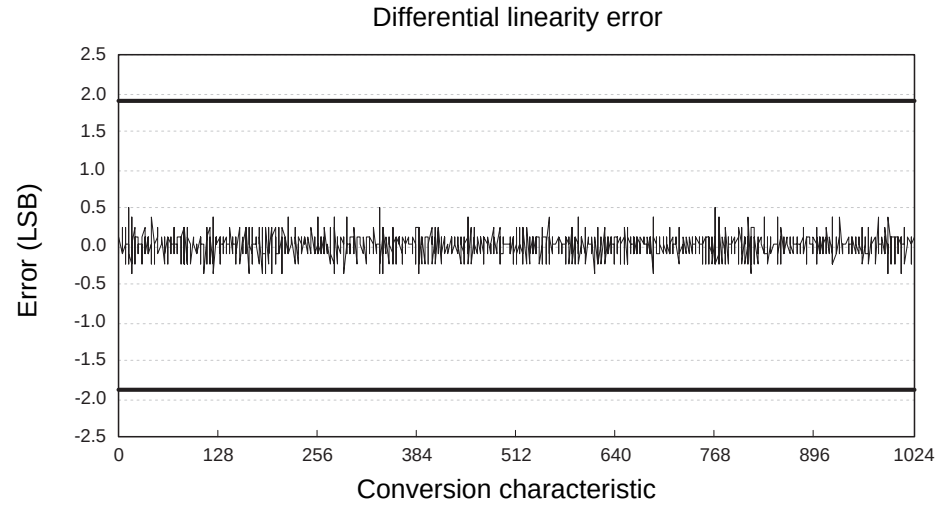


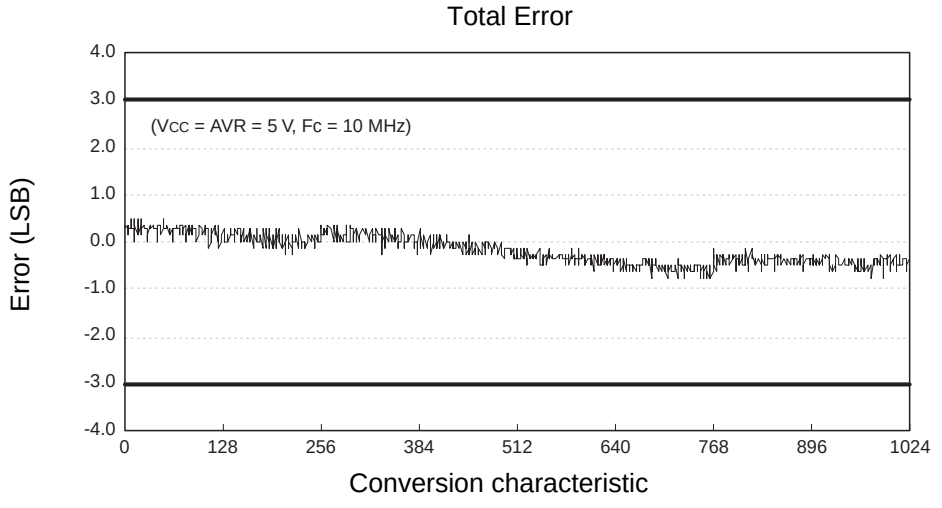
(6) "L" Level Output Voltage



(7) AD Converter Characteristic Example







■ MASK OPTIONS

No	Part number	MB89535A MB89537A MB89537AC MB89538A MB89538AC	MB89F538-101 MB89F538-201	MB89P538-101 MB89P538-201	MB89PV530-101 MB89PV530-201
	Method of specification	**Specify at time of mask order**	**Setting not possible**	**Setting not possible**	**Setting not possible**
1	Main clock Select oscillator stabilization wait period (F_{CH}* = 10 MHz) approx.$2^{14}/F_{CH}$* (approx.1.6 ms) approx.$2^{17}/F_{CH}$* (approx.13.1 ms) approx.$2^{18}/F_{CH}$* (approx.26.2 ms)	Selection available	$2^{18}/F_{CH}$* (approx. 26.2 ms)	$2^{18}/F_{CH}$* (approx. 26.2 ms)	$2^{18}/F_{CH}$* (approx. 26.2 ms)
2	Clock mode selection • 2-system clock mode • 1-system clock mode	Selection available	• 101 : 1-system clock mode • 201 : 2-system clock mode		

* : F_{CH}: Main clock frequency

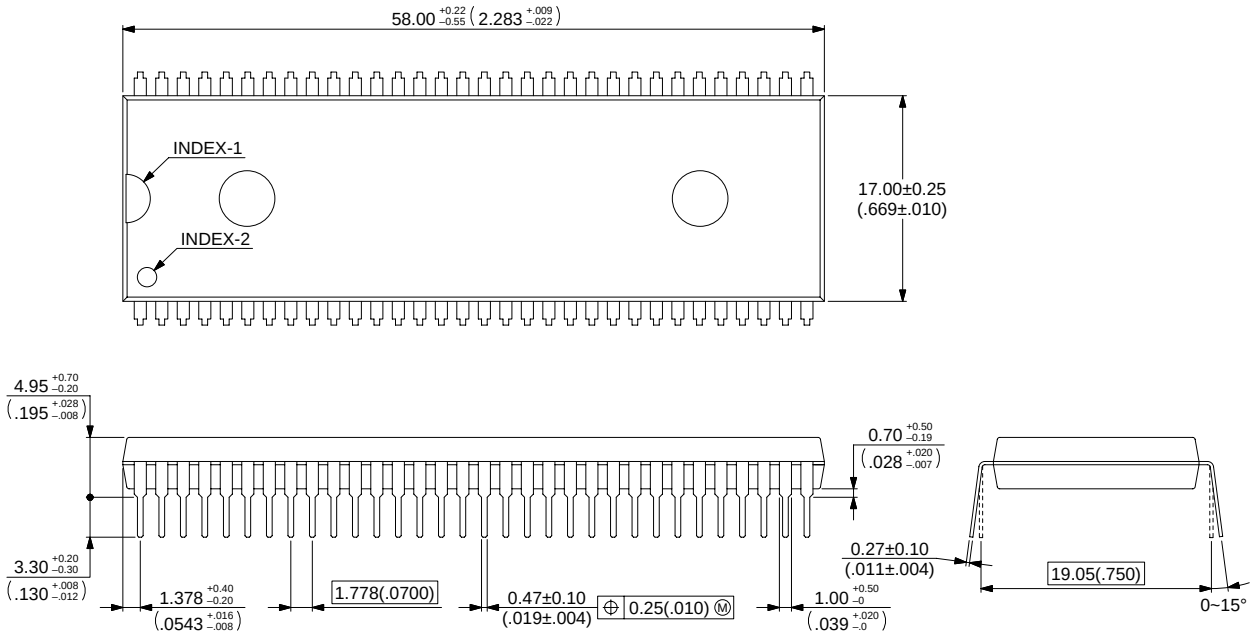
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89535AP MB89537AP MB89537ACP MB89538AP MB89538ACP MB89P538P-101 MB89P538P-201 MB89F538P-101 MB89F538P-201	DIP-64P-M01	MB89535AP, MB89537AP and MB89538AP do not have I²C functions.
MB89535APF MB89537APF MB89537ACPF MB89538APF MB89538ACPF MB89P538PF-101 MB89P538PF-201 MB89F538PF-101 MB89F538PF-201	FPT-64P-M06	MB89535APF, MB89537APF and MB89538APF do not have I²C functions.
MB89535APFM MB89537APFM MB89537ACPFM MB89538APFM MB89538ACPFM MB89P538PFM-101 MB89P538PFM-201 MB89F538PFM-101 MB89F538PFM-201	FPT-64P-M09	MB89535APFM, MB89537APFM and MB89538APFM do not have I²C functions.
MB89535APFV MB89537APFV MB89537ACPFV MB89538APFV MB89538ACPFV	FPT-64P-M03	MB89535APFV, MB89537APFV and MB89538APFV do not have I²C functions.
MB89PV530C-101 MB89PV530C-201	MDP-64C-P02	
MB89PV530CF-101 MB89PV530CF-201	MQP-64C-P01	

■ PACKAGE DIMENSIONS

64-pin plastic SH-DIP
(DIP-64P-M01)

Note : Pins width and pins thickness include plating thickness.

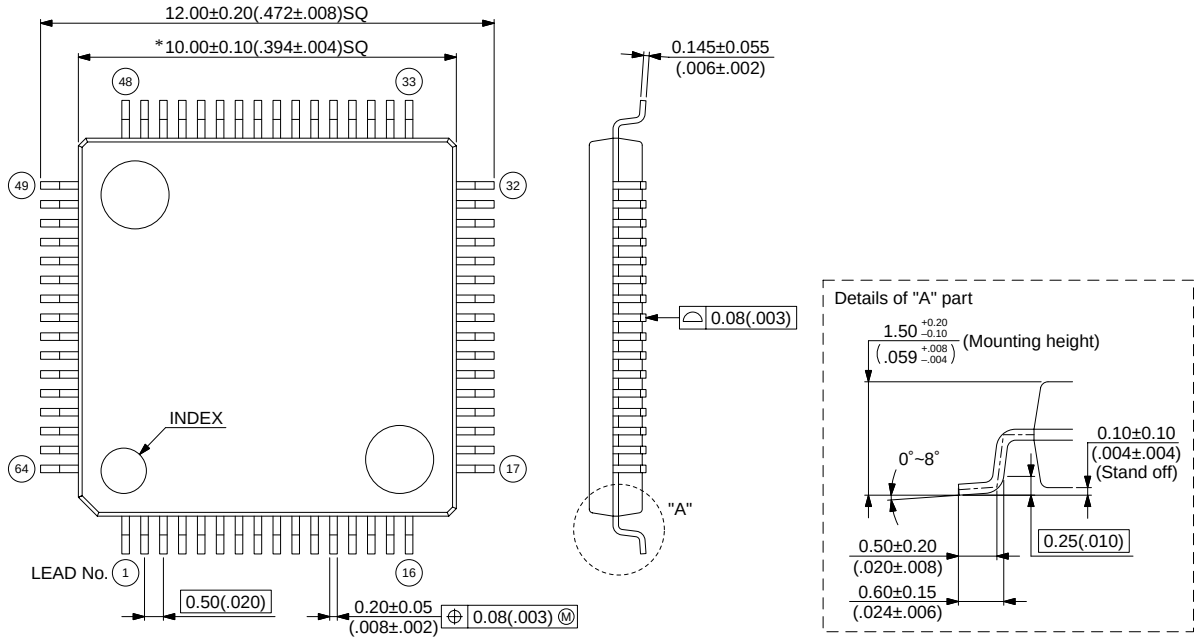


Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

64-pin, Plastic LQFP
(FPT-64P-M03)

Note 1)* : These dimensions do not include resin protrusion.
Note 2)Pins width and pins thickness include plating thickness.
Note 3)Pins width do not include tie bar cutting remainder.

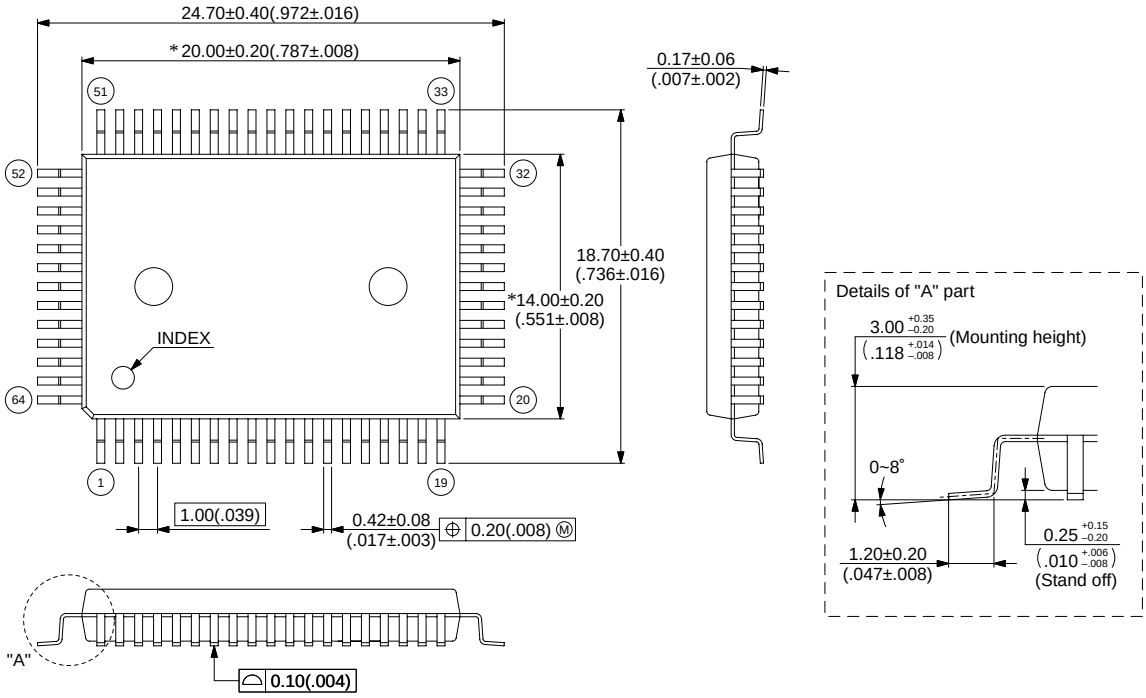


Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

64-pin, Plastic QFP
(FPT-64P-M06)

Note 1)* : These dimensions do not include resin protrusion.
Note 2)Pins width and pins thickness include plating thickness.
Note 3)Pins width do not include tie bar cutting remainder.

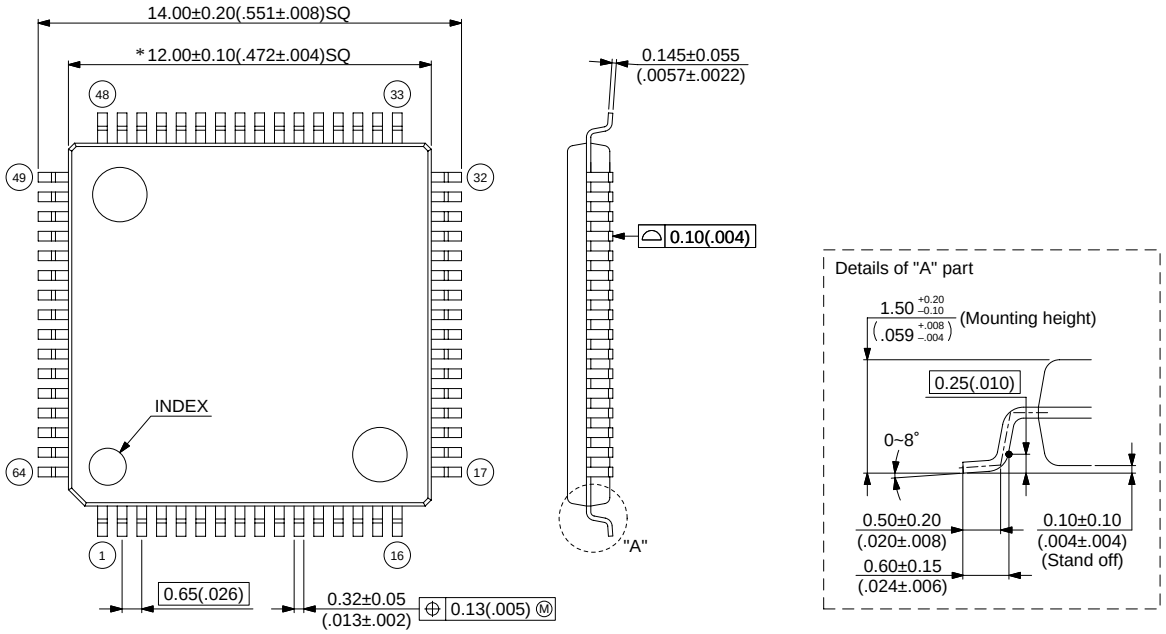


Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

64-pin, Plastic QFP
(FPT-64P-M09)

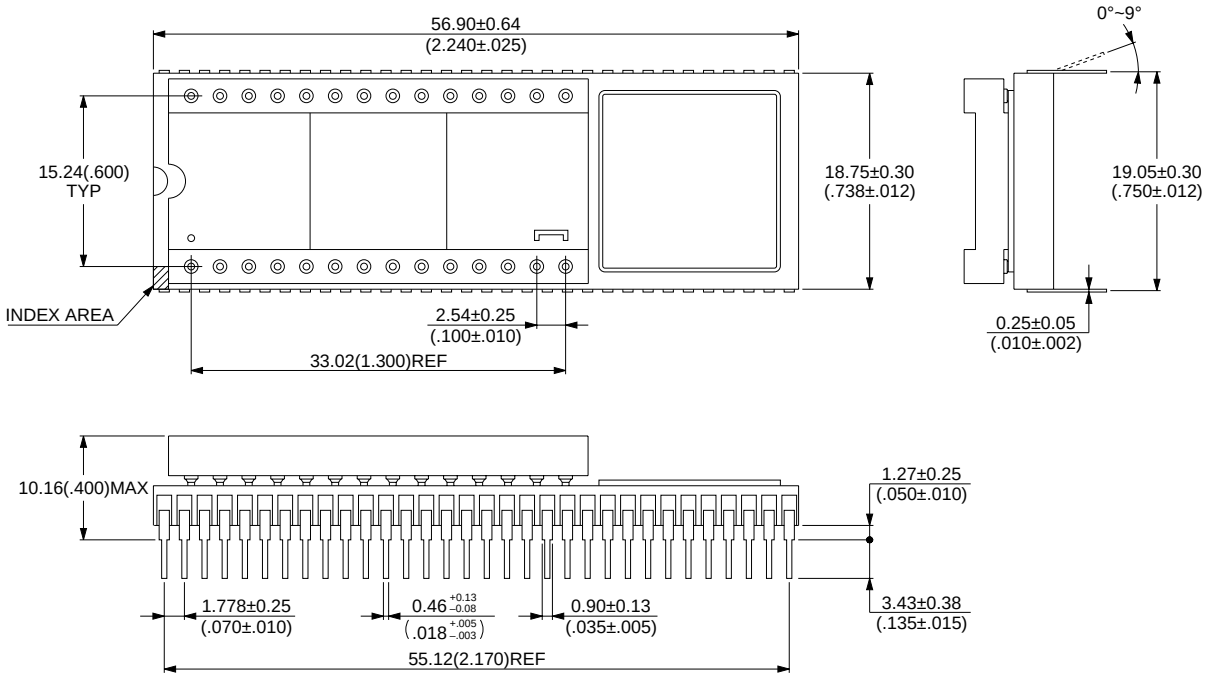
Note 1)* : These dimensions do not include resin protrusion.
Note 2)Pins width and pins thickness include plating thickness.
Note 3)Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

64-pin, Ceramic MDIP
(MDP-64C-P02)

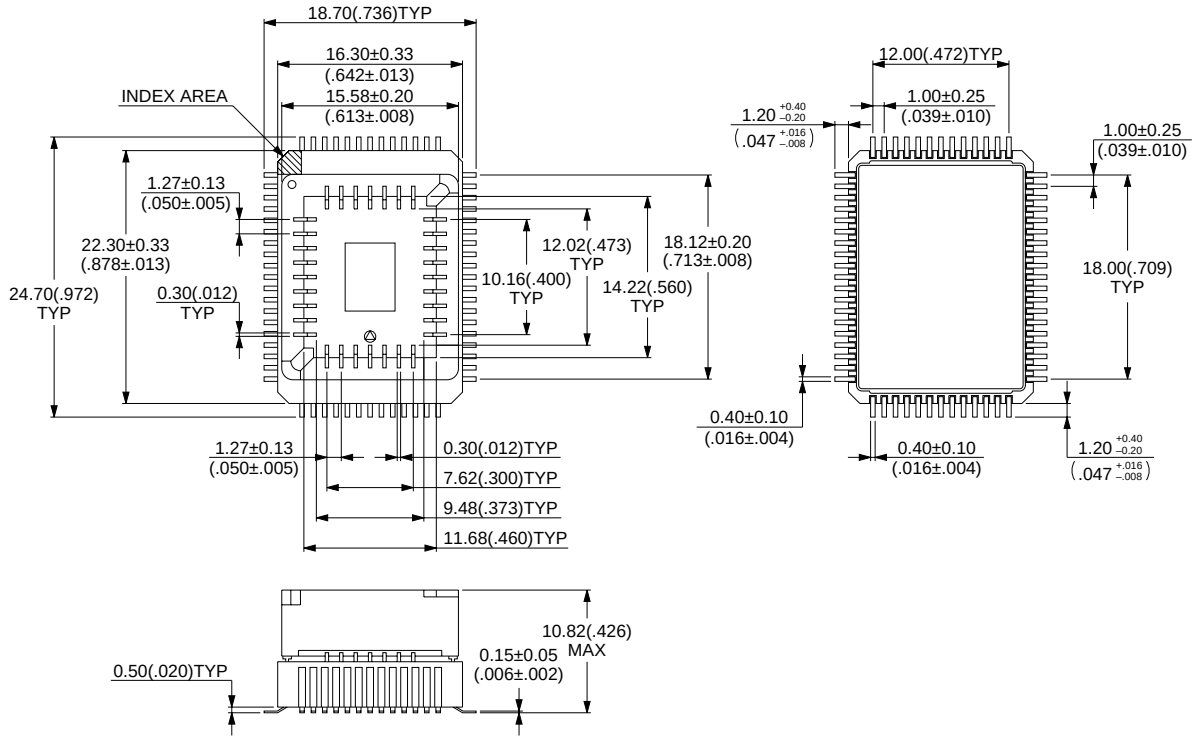


Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

(Continued)

64-pin, Ceramic MQFP
(MQP-64C-P01)



Dimensions in mm (inches).
Note: The values in parentheses are reference values

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0303