DS07-12405-3E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89160/160A Series

MB89161/163/165/P165/PV160/W165
MB89161A/163A/165A

■ DESCRIPTION

The MB89160 series is a line of the general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as an LCD controller/driver, an A/D converter, timers, a serial interface, PWM timers, and external interrupts.

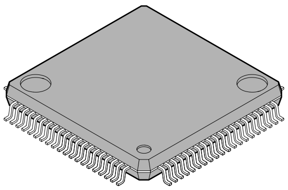
■ FEATURES

- F^2MC-8L family CPU core
- Dual-clock control system
- Maximum memory size: 16-Kbyte ROM, 512-byte RAM (max.)
- Minimum execution time: 0.95 µs/4.2 MHz
- I/O ports: max. 54 channels
- 21-bit time-base counter
- 8/16-bit timer/counter: 2 or 1 channels
- 8-bit serial I/O: 1 channel
- External interrupts (wake-up function): Four channels with edge selection plus eight level-interrupt channels
- 8-bit A/D converter: 8 channels
- 8-bit PWM timers: 2 channels
- Watch prescaler (15 bits)
- LCD controller/driver: 24 segments × 4 commons (max. 96 pixels)
- LCD driving reference voltage generator and booster (option)
- Remote control transmission output
- Buzzer output
- Power-on reset function (option)
- Low-power consumption modes (stop, sleep, and watch mode)
- CMOS technology

FUJITSU

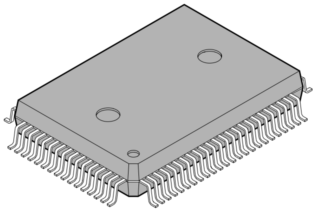
■ PACKAGE

80-pin Plastic SQFP



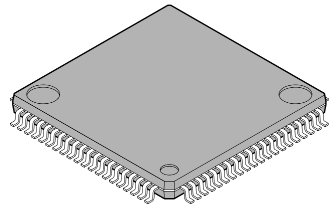
(FTP-80P-M05)

80-pin Plastic QFP



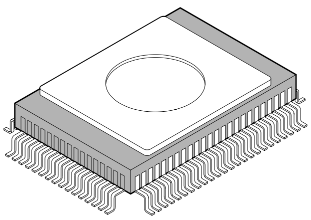
(FTP-80P-M06)

80-pin Plastic QFP



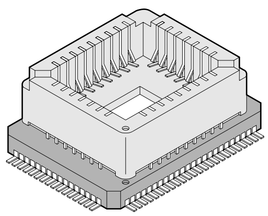
(FTP-80P-M11)

80-pin Ceramic QFP



(FPT-80C-A02)

80-pin Ceramic MQFP



(MQP-80C-P01)

■ PRODUCT LINEUP

<table>
<tr><th>Part number / Parameter</th><th>MB89161/
MB89161A[*1]</th><th>MB89163/
MB89163A[*1]</th><th>MB89165/
MB89165A[*1]</th><th>MB89P165</th><th>MB89W165</th><th>MB89PV160</th></tr>
<tr><td>Classification</td><td colspan="3">Mass production products
(mask ROM products)</td><td>One-time PROM product</td><td>EPROM product</td><td>Piggyback/ evaluation product (for development)</td></tr>
<tr><td>ROM size</td><td>4 K × 8 bits (internal mask ROM)</td><td>8 K × 8 bits (internal mask ROM)</td><td>16 K × 8 bits (internal mask ROM)</td><td colspan="2">16 K × 8 bits
(internal PROM, programming with general-purpose EPROM programmer)</td><td>32 K × 8 bits (external ROM)</td></tr>
<tr><td>RAM size</td><td>128 × 8 bits</td><td>256 × 8 bits</td><td colspan="4">512 × 8 bits</td></tr>
<tr><td>CPU functions</td><td colspan="6">Number of instructions: 136
Instruction bit length: 8 bits
Instruction length: 1 to 3 bytes
Data bit length: 1, 8,16 bits
Minimum execution time: 0.95 µs/4.2 MHz
Interrupt processing time: 9 µs/4.2 MHz</td></tr>
<tr><td>Ports</td><td colspan="6">I/O port (N-ch open-drain): 8 (6 ports also serve as peripherals, 3 ports are a heavy-current drive type.)
Output ports (N-ch open-drain): 28 (16 ports also serve as segment pins, 2 ports serve as booster capacitor connection pins, 2 ports serve as common pins.)[*3] (8 ports also serve as an A/D input)
I/O ports (CMOS): 16 (12 ports also serve as an external interrupt)
Output ports (CMOS): 2 (Also serve as peripherals)
Total: 54 (max.)</td></tr>
<tr><td>Timer/counter</td><td colspan="6">8-bit timer operation (toggled output capable, operating clock cycle 1.9 µs to 486 µs)
16-bit timer operation (toggled output capable, operating clock cycle 1.9 µs to 486 µs)</td></tr>
<tr><td>Serial I/O</td><td colspan="6">8 bits
LSB first/MSB first selectability
One clock selectable from four operation clocks
(one external shift clock, three internal shift clocks: 1.9 µs, 7.6 µs, 30.4 µs)</td></tr>
<tr><td>LCD controller/ driver</td><td colspan="5">Common output: 4 (max.)
Segment output: 24 (max.) [*3]
Bias power supply pins: 4
LCD display RAM size: 24 × 4 bits
Booster for LCD driving: Built-in (product with a booster)[*3]
Dividing resistor for LCD driving: Built-in (an external resistor selectability)</td><td>Without a booster for LCD driving</td></tr>
<tr><td>A/D converter</td><td colspan="6">8-bit resolution × 8 channels
A/D conversion mode (conversion time 43 µs/4.2 MHz (44 instruction cycles))
Sense mode (conversion time 11.9 µs/4.2 MHz)
Continuous activation by an internal timer capable
Reference voltage input</td></tr>
</table>

(Continued)

(Continued)

Part number / Parameter	MB89161/ MB89161A*1	MB89163/ MB89163A*1	MB89165/ MB89165A*1	MB89P165	MB89W165	MB89PV160
PWM timer 1, PWM timer 2	8 bits × 2 channels 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.95 µs to 124 ms) 8-bit resolution PWM operation (conversion cycle: 243 µs to 32 s)					
External interrupt 1 (wake-up function)	4 independent channels (edge selectability) Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)					
External interrupt 2	"L" level interrupts × 8 channels					
Buzzer output	1 (7 frequencies are selectable by the software.)					
Remote control transmission output	1 (Pulse width and cycle are software selectable.)					
Standby modes	Subclock mode, sleep mode, stop mode, and watch mode					
Process	CMOS					
Operating voltage*2	2.2 V to 6.0 V (single clock)/ 2.2 V to 4.0 V (dual clock)			2.7 V to 6.0 V		
EPROM for use	—					MBM27C256A-20TV

*1: Products with an internal booster.

*2: Varies with conditions such as the operating frequency. (The operating voltage of the A/D converter is assured separately. See section "■ Electrical Characteristics.")

*3: See section "■ Mask Options."

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89161 MB89161A	MB89163 MB89163A	MB89165 MB89165A	MB89PW165	MB89W165	MB89PV160
FPT-80P-M05	○	○	○	○	×	×
FPT-80P-M06	○	○	○	○	×	×
FPT-80P-M11	○	○	○	○	×	×
MQP-80C-P01	×	×	×	×	○	×
FPT-80C-A02	×	×	×	×	×	○

○ : Available   × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89161/A and MB89163/A, the upper half of each register bank cannot be used.
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV160, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in the sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

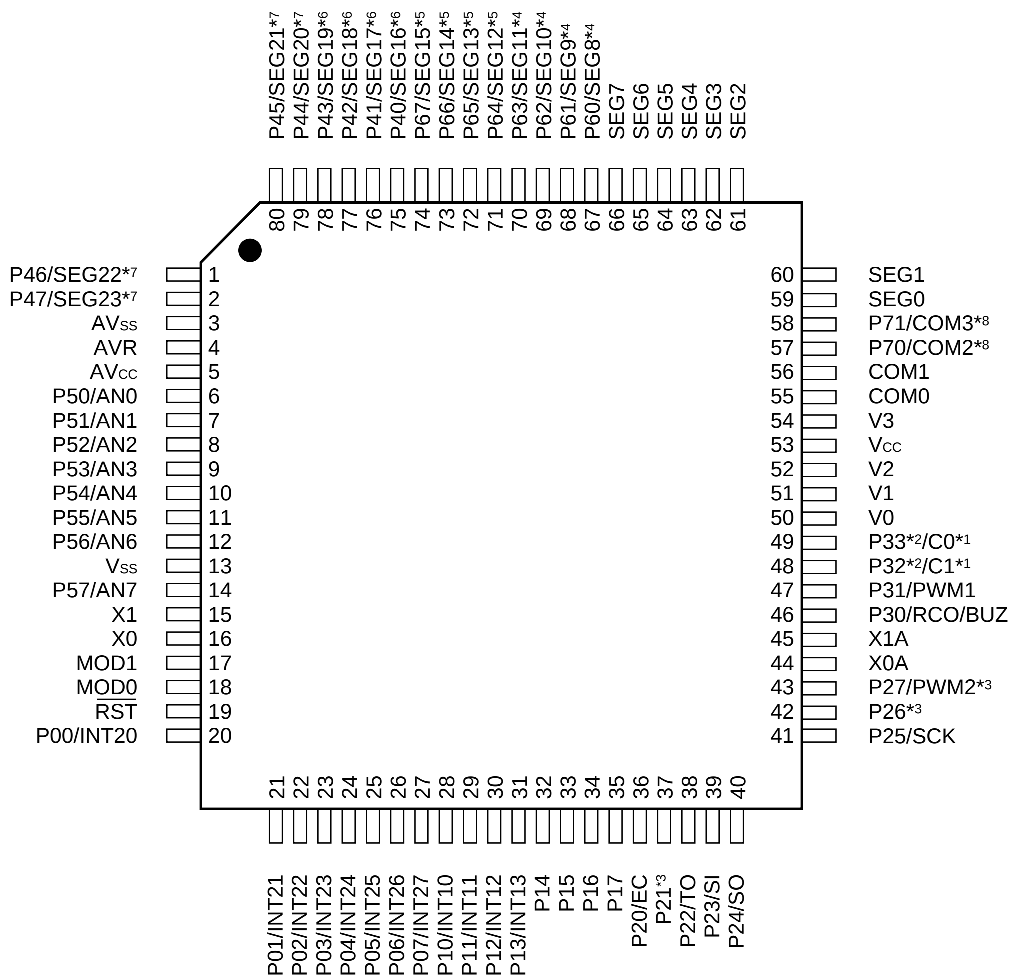
Before using options check section "■ Mask Options."

Take particular care on the following points:

- A pull-up resistor cannot be set for P20 to P27 on the MB89P165.
- A pull-up resistor is not selectable for P40 to P47 and P60 to P67 if they are used as LCD pins.
- Options are fixed on the MB89PV160.

■ PIN ASSIGNMENT

(Top view)

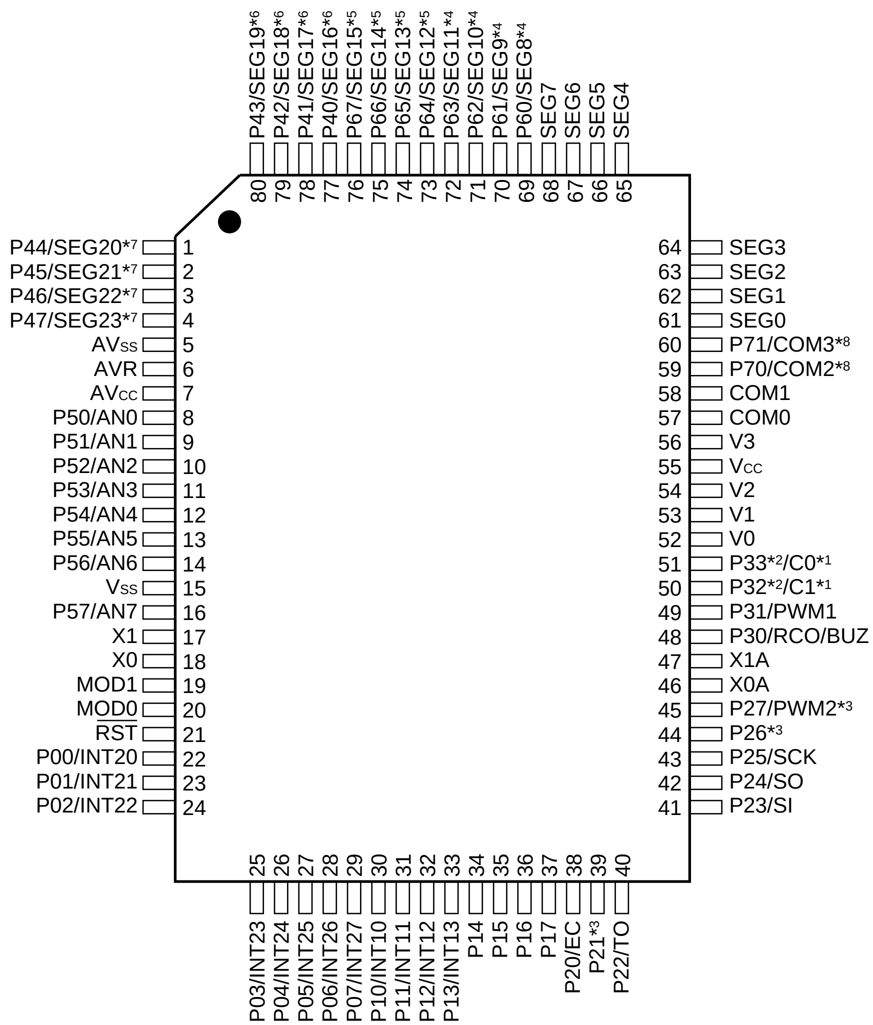


(FPT-80P-M11)

*1: For products with a booster circuit
*2: For products without a booster circuit
*3: N-ch open-drain heavy-current drive type
*4 to *7: Selected using the mask option (in units of 4 pins)
*8: Selected using the mask option (in units of 2 pins)

Note: For more information on mask option combinations of *4 to *8, see section "■ Mask Options."

(Top view)

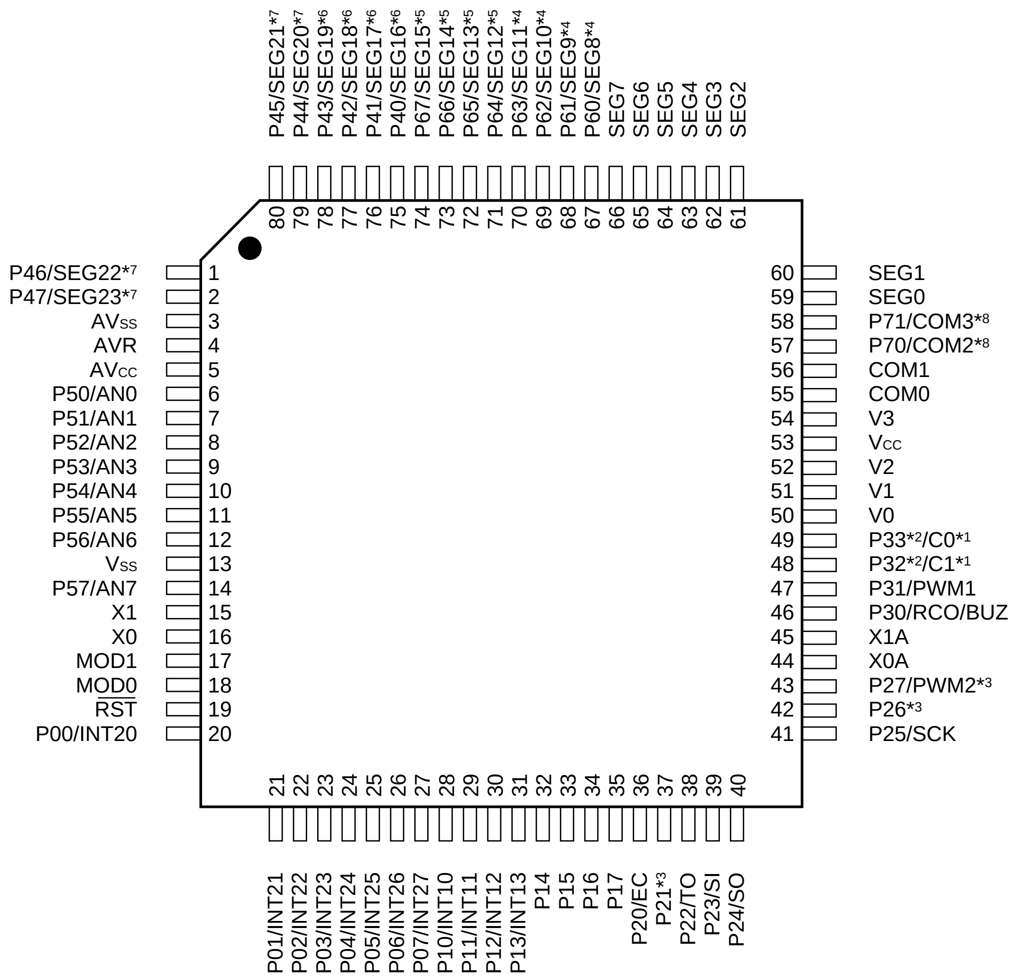


(FPT-80P-M06)
(FPT-80C-A02)

*1: For products with a booster circuit
*2: For products without a booster circuit
*3: N-ch open-drain heavy-current drive type
*4 to *7: Selected using the mask option (in units of 4 pins)
*8: Selected using the mask option (in units of 2 pins)

Note: For more information on mask option combinations of *4 to *8, see section “■ Mask Options.”

(Top view)

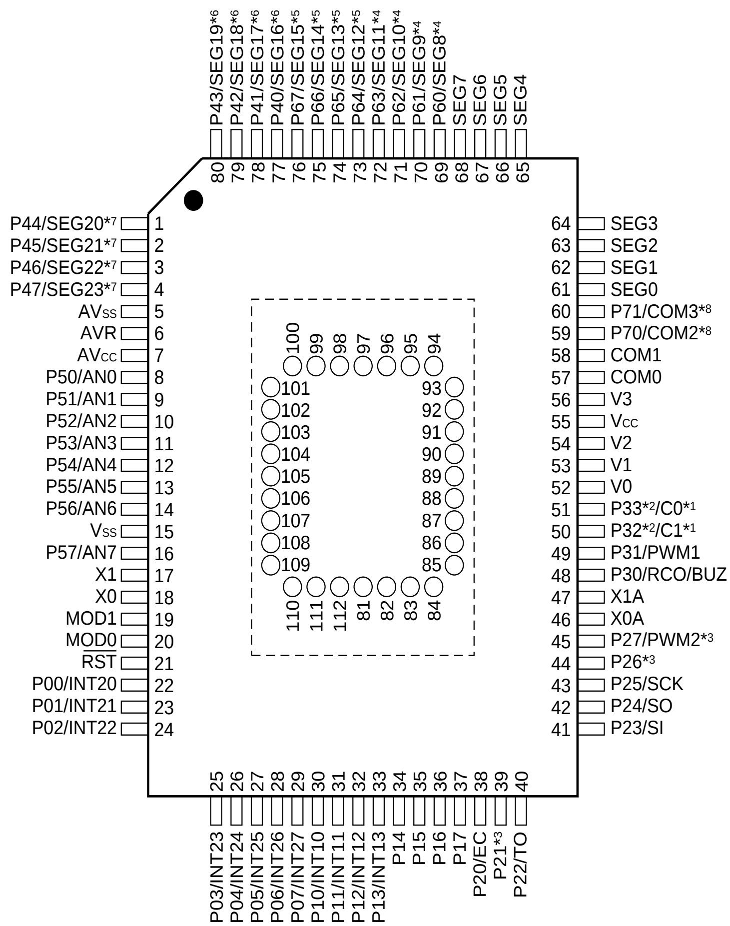


(FPT-80P-M05)

*1: For products with a booster circuit
*2: For products without a booster circuit
*3: N-ch open-drain heavy-current drive type
*4 to *7: Selected using the mask option (in units of 4 pins)
*8: Selected using the mask option (in units of 2 pins)

Note: For more information on mask option combinations of *4 to *8, see section "■ Mask Options."

(Top view)



(MQP-80C-P01)

*1: For products with a booster circuit
*2: For products without a booster circuit
*3: N-ch open-drain heavy-current drive type
*4 to *7: Selected using the mask option (in units of 4 pins)
*8: Selected using the mask option (in units of 2 pins)

Note: For more information on mask option combinations of *4 to *8, see section "■ Mask Options."

- **Pin assignment on package top (MB89PV160 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	A2	97	N.C.	105	$\overline{\text{OE}}$
82	V_{PP}	90	A1	98	O4	106	N.C.
83	A12	91	A0	99	O5	107	A11
84	A7	92	N.C.	100	O6	108	A9
85	A6	93	O1	101	O7	109	A8
86	A5	94	O2	102	O8	110	A13
87	A4	95	O3	103	$\overline{\text{CE}}$	111	A14
88	A3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SQFP*1 QFP*2	MQFP*3 QFP*4			
16	18	X0	A	Main clock crystal oscillator pins CR oscillation selectability (mask products only)
15	17	X1		
18	20	MOD0	C	Operating mode selection pins Connect directly to V_{SS}.
17	19	MOD1		
19	21	$\overline{\text{RST}}$	D	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
20 to 27	22 to 29	P00/INT20 to P07/INT27	E	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input is hysteresis input.
28 to 31	30 to 33	P10/INT10 to P13/INT13	E	General-purpose I/O ports Also serve as an external interrupt 1 input. External interrupt 1 input is hysteresis input.
32 to 35	34 to 37	P14 to P17	F	General-purpose I/O ports
36	38	P20/EC	H	N-ch open-drain general-purpose I/O port Also serves as the external clock input for the timer. The peripheral is a hysteresis input type.
37	39	P21	I	N-ch open-drain general-purpose I/O port
38	40	P22/TO	I	N-ch open-drain general-purpose I/O port Also serves as a timer output.
39	41	P23/SI	H	N-ch open-drain general-purpose I/O port Also serves as the data input for the serial I/O. The peripheral is a hysteresis input type.
40	42	P24/SO	I	N-ch open-drain general-purpose I/O port Also serves as the data output for the serial I/O.
41	43	P25/SCK	H	N-ch open-drain general-purpose I/O port Also serves as the clock I/O for the serial I/O. The peripheral is a hysteresis input type.
42	44	P26	I	N-ch open-drain general-purpose I/O port
43	45	P27/PWM2	I	N-ch open-drain general-purpose I/O port Also serves as the square wave or PWM wave output for the 8-bit PWM timer 2.
49	51	P33	J	Functions as an N-ch open-drain general-purpose output port only in the products without a booster.
		C0	—	Functions as a capacitor connection pin in the products with a booster.

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*1: FPT-80P-M05
*2: FPT-80P-M11
*3: MQP-80C-P01
*4: FPT-80P-M06

(Continued)

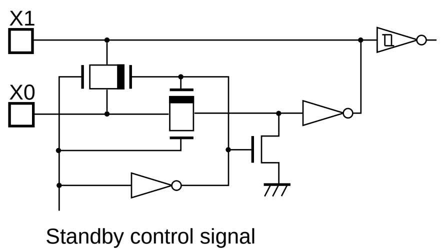
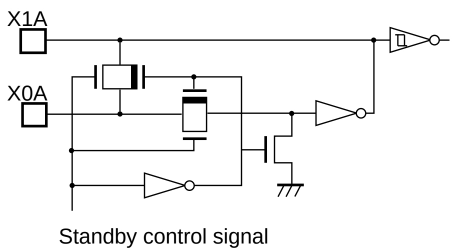
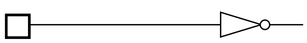
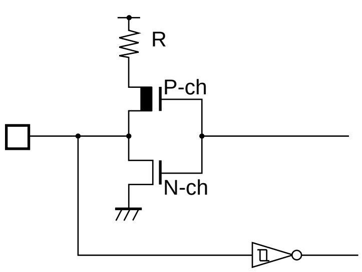
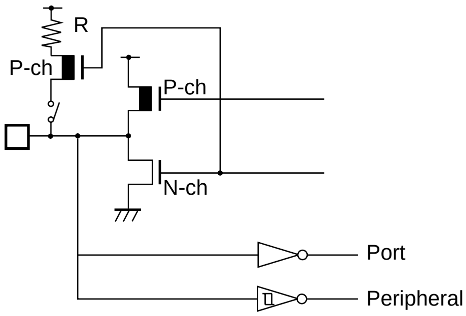
Pin no.		Pin name	Circuit type	Function
SQFP[*1] QFP[*2]	**MQFP[*3] QFP[*4]**			
48	50	P32	J	Functions as an N-ch open-drain general-purpose output port only in the products without a booster.
		C1	—	Functions as a capacitor connection pin in the products with a booster.
47	49	P31/PWM1	G	General-purpose output-only port Also serves as the square wave or PWM wave output for the 8-bit PWM timer 1.
46	48	P30/RCO/BUZ	G	General-purpose output-only port Also serves as a buzzer output and a remote control transmission frequency output.
14, 12 to 6	16, 14 to 8	P57/AN7 to P50/AN0	L	N-ch open-drain general-purpose output ports Also serve as an analog input.
2, 1, 80 to 75	4 to 1 80 to 77	P47/SEG23 to P40/SEG16	J/K	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver segment output. Switching between port and segment output is done by the mask option.
74 to 67	76 to 69	P67/SEG15 to P60/SEG8	J/K	
66 to 59	68 to 61	SEG7 to SEG0	K	LCD controller/driver segment output pins
58, 57	60, 59	P71/COM3, P70/COM2	J/K	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver common output. Switching between port and common output is done by the mask option.
56, 55	58, 57	COM1, COM0	K	LCD controller/driver common output-only pins
54, 52 to 50	56, 54 to 52	V3, V2 to V0	—	LCD driving power supply pins
44	46	X0A	B	Subclock crystal oscillator pins (32.768 KHz)
45	47	X1A		
53	55	V_{CC}	—	Power supply pin
13	15	V_{SS}	—	Power supply (GND) pin
5	7	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{CC}.
4	6	AVR	—	A/D converter reference voltage input pin
3	5	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.

*1: FPT-80P-M05
*2: FPT-80P-M11
*3: MQP-80C-P01
*4: FPT-80P-M06

- **External EPROM pins (MB89PV160 only)**

Pin no.	Pin name	I/O	Function
82	V_{PP}	O	“H” level output pin
83 84 85 86 87 88 89 90 91	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V_{SS}	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
104	A10	O	Address output pin
105	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	V_{CC}	O	EPROM power supply pin
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Main clock • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V • CR oscillation is selectable (MB8916X/A only).
B		Subclock • At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V
C		
D		• At an output pull-up resistor of approximately 50 kΩ/5.0 V • Hysteresis input
E		• CMOS I/O • The peripheral is a hysteresis input type. • Pull-up resistor optional (Not available on the MB89PV160.)

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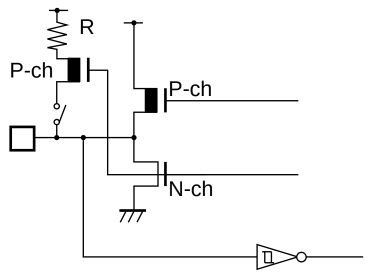
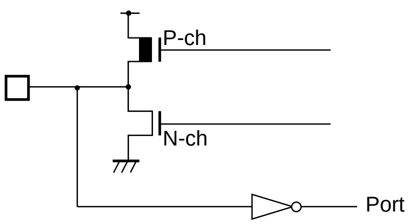
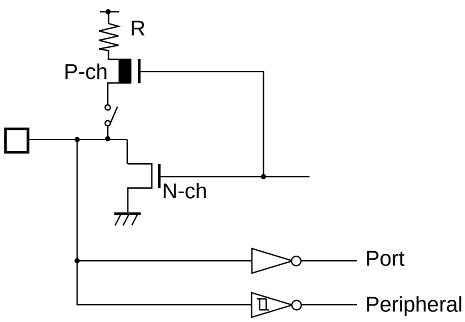
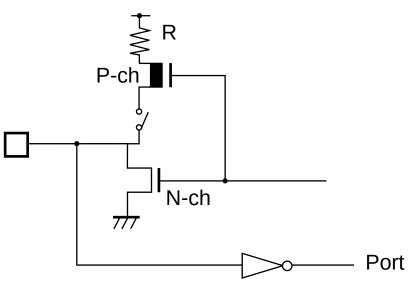
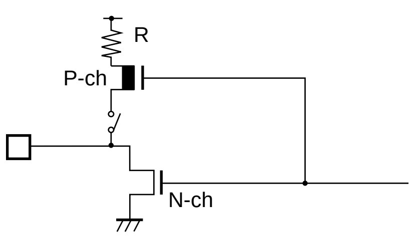
<table>
<tr><th>Type</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>F</td><td>
</td><td>• CMOS I/O
• Pull-up resistor optional
(Not available on the MB89PV160)</td></tr>
<tr><td>G</td><td>
</td><td>• CMOS output
• P-ch output is a heavy-current drive type.</td></tr>
<tr><td>H</td><td>
</td><td>• N-ch open-drain I/O
• CMOS input
• The peripheral is a hysteresis input type.
• P21, P26, and P27 are a heavy-current drive type.
• Pull-up resistor optional
(Not available on the MB89P165/A, MB89W165/A and MB89PV160)</td></tr>
<tr><td>I</td><td>
</td><td>• N-ch open-drain output
• CMOS input
• Pull-up resistor optional
(Not available on the MB89P165/A, MB89W165/A and MB89PV160)</td></tr>
<tr><td>J</td><td>
</td><td>• N-ch open-drain output
• Pull-up resistor optional
(Not available on the MB89P165/A, MB89W165/A and MB89PV160)
• P32 and P33 are not provided with a pull-up resistor.</td></tr>
</table>

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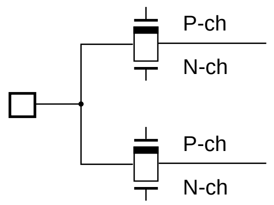
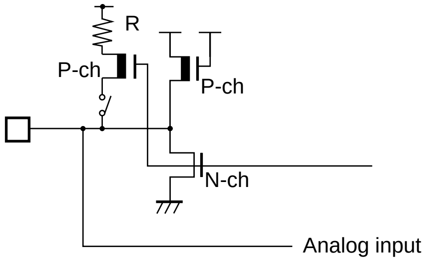
Type	Circuit	Remarks
K		• LCD controller/driver segment output
L		• N-ch open-drain output • Analog input • Pull-up resistor optional (Not available on the MB89PV160)

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on " 1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between V_{CC} to V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pin

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P165

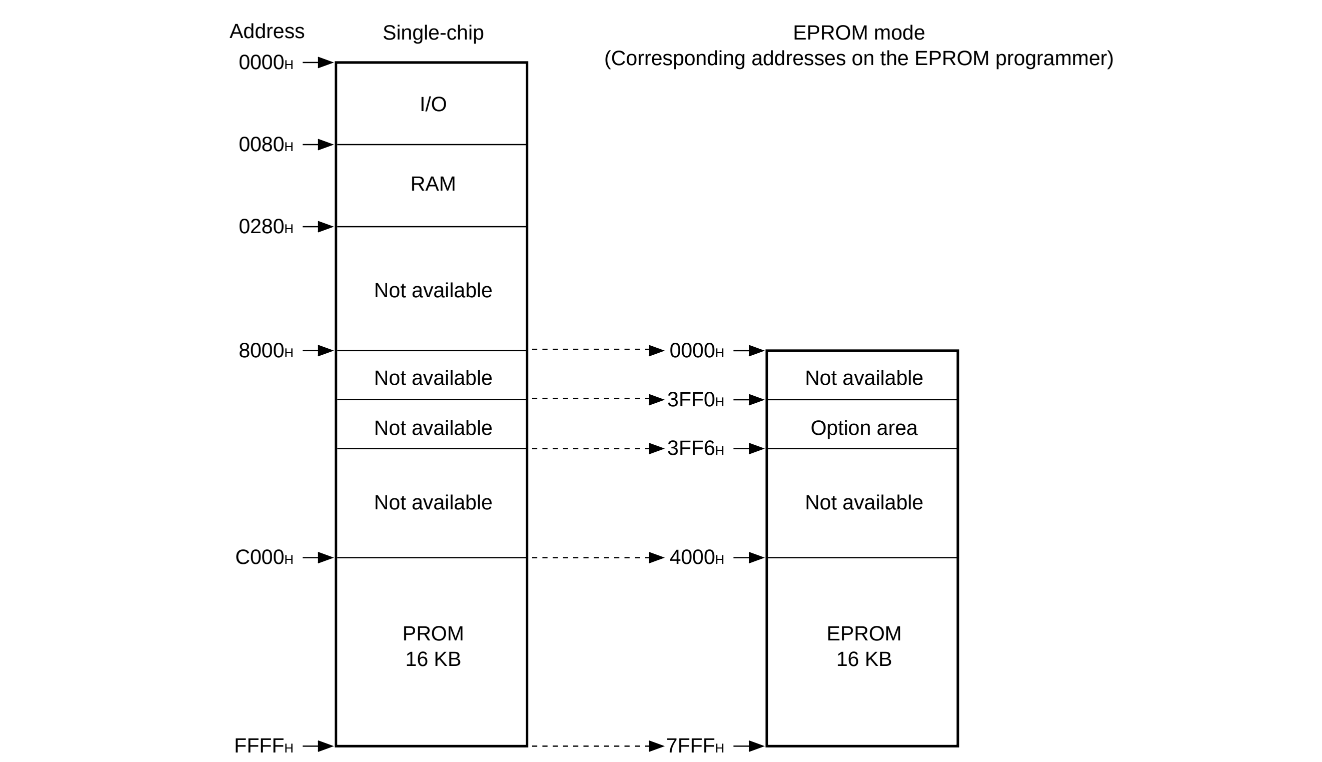
The MB89P165 is an OTPROM version of the MB89160 series.

1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P165 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating area for a single chip is 16 Kbyte ($C000_H$ to $FFFF_H$) the PROM can be programmed as follows:

- **Programming procedure**

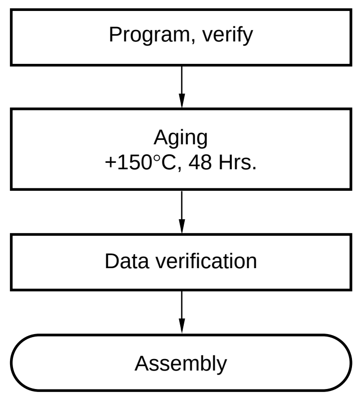
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program into the EPROM programmer at 4000_H to $7FFF_H$.
(Note that addresses $C000_H$ to $FFFF_H$ while operating as a single chip assign to 4000_H to $7FFF_H$ in EPROM mode.)
Load option data into address $3FF0_H$ to $3FF5_H$ of the EPROM programmer.
(For information about each corresponding option, see “8. Setting OTPROM Options.”)

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Adapter Socket

Package	Compatible adapter socket
FPT-80P-M05	ROM-80SQF-28DP-8L
FPT-80P-M06	ROM-80QF-28DP-8L3
FPT-80P-M11	ROM-80QF2-28DP-8L2

7. Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the internal EPROM to an ultraviolet light source. A dosage of 10 W-seconds/cm^2 is required to completely erase an internal EPROM. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000 μW/cm$_2$ for 15 to 21 minutes. The internal EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the internal EPROM and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the internal EPROM, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

8. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming value at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$3FF0_H$	Vacancy Readable	Vacancy Readable	Oscillation stabilization time WTM1 See section "■ Mask Option."	WTM0	Vacancy Readable	Reset pin output 1: Yes 0: No	Clock mode selection 1: Dual clock 0: Single clock	Power-on reset 1: Yes 0: No
$3FF1_H$	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
$3FF2_H$	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
$3FF3_H$	P57 Pull-up 1: No 0: Yes	P56 Pull-up 1: No 0: Yes	P55 Pull-up 1: No 0: Yes	P54 Pull-up 1: No 0: Yes	P53 Pull-up 1: No 0: Yes	P52 Pull-up 1: No 0: Yes	P51 Pull-up 1: No 0: Yes	P50 Pull-up 1: No 0: Yes
$3FF4_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
$3FF5_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable

Notes:
- Set each bit to 1 to erase.
- Do not write 0 to the vacant bit.
  The read value of the vacant bit is 1, unless 0 is written to it.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

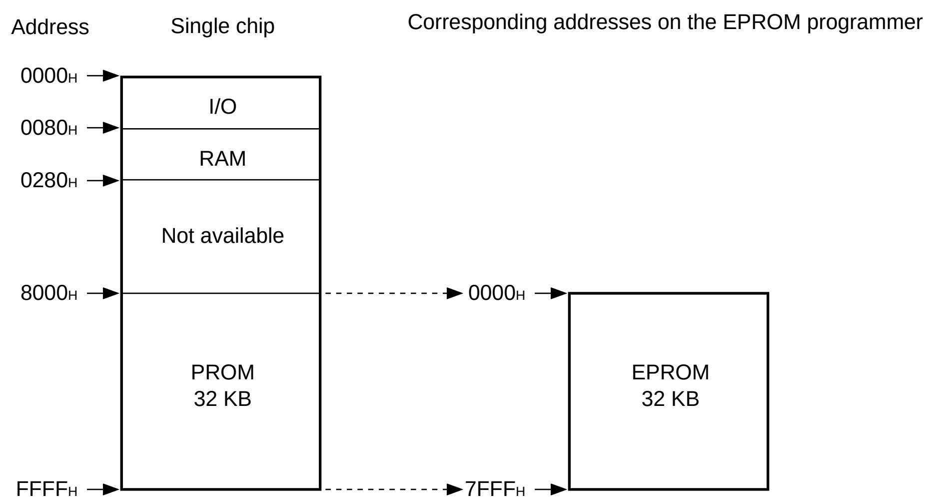
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



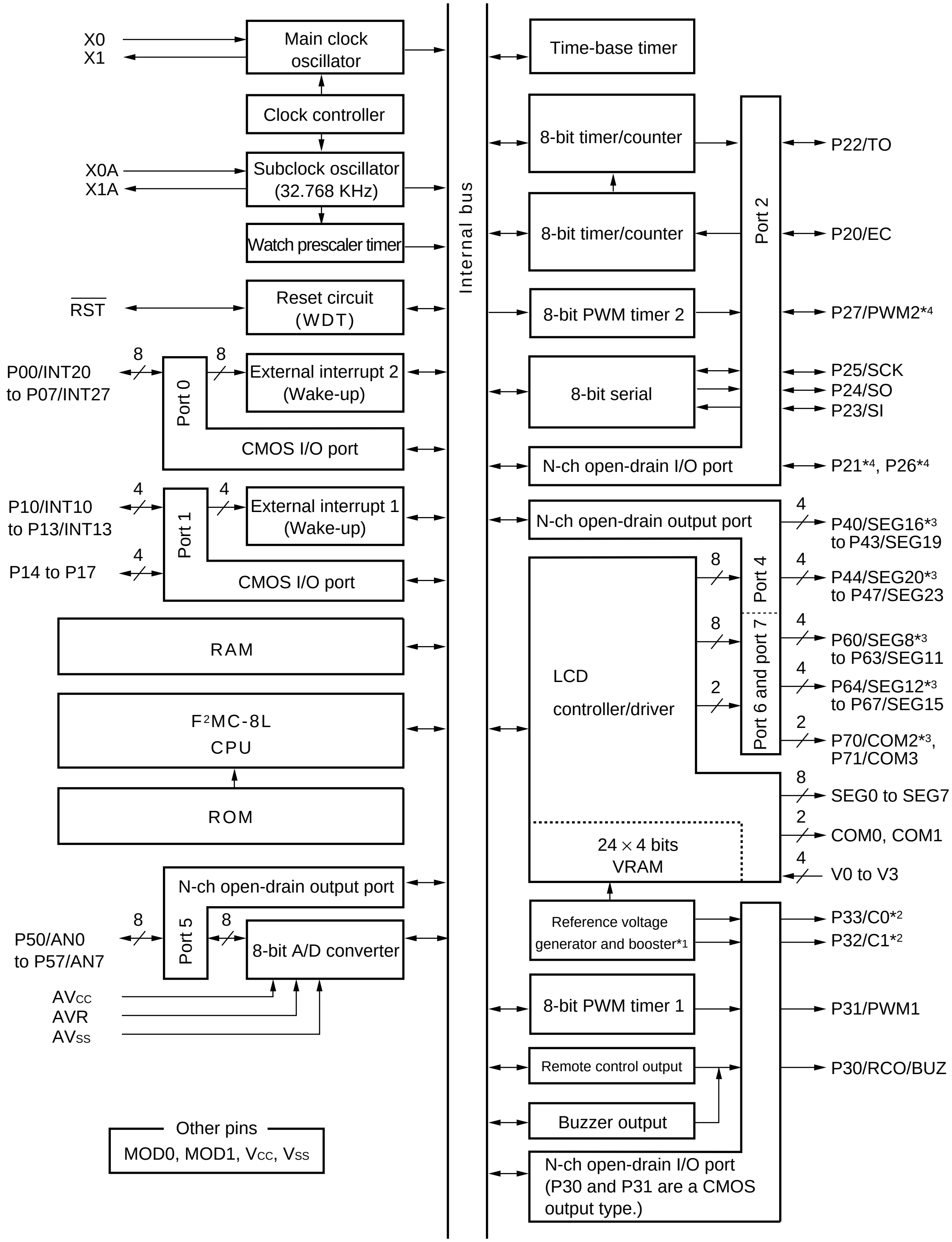
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM



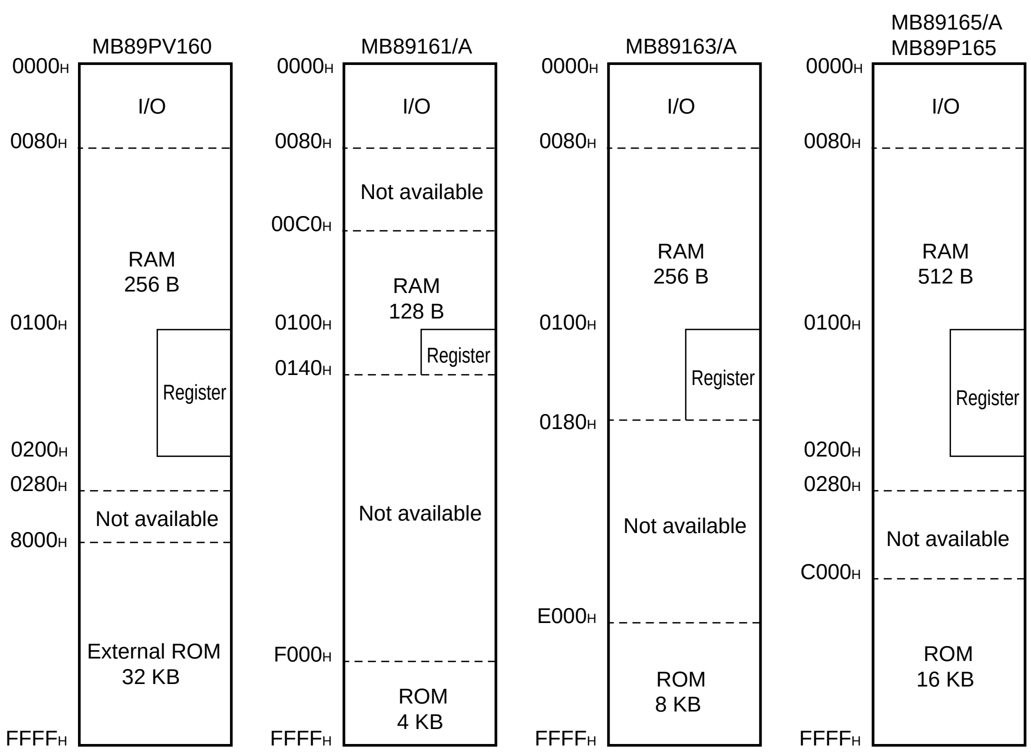
*1: Selected by mask option
*2: Used as ports without a reference voltage generator and booster
*3: Functions selected by mask option. (For information on selecting procedure, see section "■ Mask Options.")
*4: Heavy-current drive type

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89160 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89160 series is structured as illustrated below.

Memory Space



2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 18-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code

16 bits		Initial value
PC	: Program counter	FFFD$_H$
A	: Accumulator	Undefined
T	: Temporary accumulator	Undefined
IX	: Index register	Undefined
EP	: Extra pointer	Undefined
SP	: Stack pointer	Undefined
PS	: Program status	I-flag = 0, IL1, 0 = 11 Other bits are undefined.

The PS can further be divide into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS	RP					Vacancy	Vacancy	Vacancy	H	I	IL1, 0		N	Z	V	C
	RP								CCR							

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area

									RP					Lower OP codes		
	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	R4	R3	R2	R1	R0	b2	b1	b0
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Generated addresses	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		↕
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set the shift-out value in the case of a shift instruction.

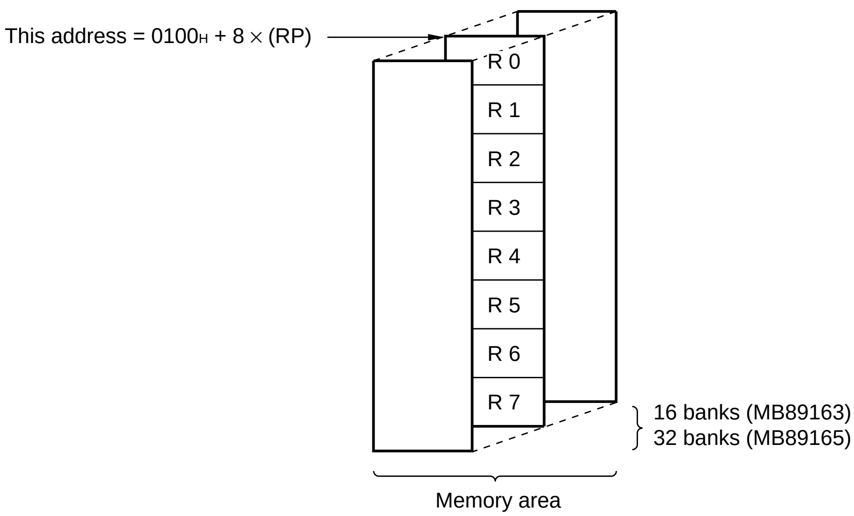
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 16 banks can be used on the MB89163 (RAM 256 × 8 bits), and a total of 32 banks can be used on the MB89165 (RAM 256 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuraiton



■ I/O MAP

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	DDR0	Port 0 data direction register
02_H	(R/W)	PDR1	Port 1 data register
03_H	(W)	DDR1	Port 1 data direction register
04_H	(R/W)	PDR2	Port 2 data register
05_H	(W)	DDR2	Port 2 data direction register
06_H	Vacancy		
07_H	(R/W)	SYCC	System clock control register
08_H	(R/W)	STBC	Standby control register
09_H	(R/W)	WDTE	Watchdog timer control register
$0A_H$	(R/W)	TBTC	Time-base timer control register
$0B_H$	(R/W)	WPCR	Watch prescaler control register
$0C_H$	(R/W)	PDR3	Port 3 data register
$0D_H$	Vacancy		
$0E_H$	(R/W)	PDR4	Port 4 data register
$0F_H$	(R/W)	PDR5	Port 5 data register
10_H	(R/W)	BUZR	Buzzer register
11_H	Vacancy		
12_H	(R/W)	PDR6	Port 6 data register
13_H	(R/W)	PDR7	Port 7 data register
14_H	(R/W)	RCR1	Remote control transmission register 1
15_H	(R/W)	RCR2	Remote control transmission register 2
16_H	Vacancy		
17_H	Vacancy		
18_H	(R/W)	T2CR	Timer 2 control register
19_H	(R/W)	T1CR	Timer 1 control register
$1A_H$	(R/W)	T2DR	Timer 2 data register
$1B_H$	(R/W)	T1DR	Timer 1 data register
$1C_H$	(R/W)	SMR	Serial mode register
$1D_H$	(R/W)	SDR	Serial data register
$1E_H$	(R/W)	CNTR1	PWM 1 control register
$1F_H$	(W)	COMP1	PWM 1 compare register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20_H	(R/W)	CNTR2	PWM 2 control register
21_H	(W)	COMP2	PWM 2 compare register
22_H to $2C_H$	Vacancy		
$2D_H$	(R/W)	ADC1	A/D converter control register 1
$2E_H$	(R/W)	ADC2	A/D converter control register 2
$2F_H$	(R/W)	ADCD	A/D converter data register
30_H	(R/W)	EIE1	External interrupt 1 enable register 1
31_H	(R/W)	EIF1	External interrupt 1 flag register 1
32_H	(R/W)	EIE2	External interrupt 2 enable register 2
33_H	(R/W)	EIF2	External interrupt 2 flag register 2
34_H to $5F_H$	Vacancy		
60_H to $6B_H$	(R/W)	VRAM	Display data RAM
$6C_H$ to 71_H	Vacancy		
72_H	(R/W)	LCDR	LCD controller/driver control register 1
73_H to $7B_H$	Vacancy		
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$	Access prohibited	ITR	Interrupt test register

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	AV_{CC} must not exceed V_{CC} + 0.3 V.
	AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	AVR must not exceed AV_{CC} + 0.3 V.
LCD power supply voltage	V0 to V3	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	V0 to V3 on the product without booster must not exceed V_{CC}.
Input voltage	V_{I1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	V_{I1} must not exceed V_{SS} + 7.0 V. All pins except P20 to P27 without a pull-up resistor
	V_{I2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P20 to P27 without a pull-up resistor
Output voltage	V_{O1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	V_{O1} must not exceed V_{SS} + 7.0 V. All pins except P20 to P27, P32, P33, P40 to P47, and P60 to P67 without a pull-up resistor
	V_{O2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P20 to P27, P32, P33, P40 to P47, and P60 to P67 without a pull-up resistor
"L" level maximum output current	I_{OL1}	—	10	mA	All pins except P21, P26, and P27
	I_{OL2}	—	20	mA	P21, P26, and P27
"L" level average output current	I_{OLAV1}	—	4	mA	All pins except P21, P26, P27, and power supply pins Average value (operating current × operating rate)
	I_{OLAV2}	—	8	mA	P21, P26, and P27 Average value (operating current × operating rate)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	Peak value
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	I_{OH1}	—	–5	mA	All pins except P30, P31, and power supply pins
	I_{OH2}	—	–10	mA	P30 and P31

(Continued)

(Continued)

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
"H" level average output current	I_{OHAV1}	—	–2	mA	All pins except P30, P31, and power supply pins Average value (operating current × operating rate)
	I_{OHAV2}	—	–4	mA	P30 and P31 Average value (operating current × operating rate)
"H" level total maximum output current	ΣI_{OH}	—	–50	mA	Peak value
"H" level total average output current	ΣI_{OHAV}	—	–10	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

Precautions: Parmanent device damage may occur if the above "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*1	6.0*1	V	Normal operation assurance range*1
		2.2*1	4.0	V	Dual-clock mask ROM products
		2.7	6.0	V	Normal operation assurance range for MB89P165/A and MB89W165/A
		1.5	6.0	V	Retains the RAM state in stop mode
	AVR	2.0	AV_{CC}	V	Normal operation assurance range
LCD power supply voltage	V0 to V3	V_{SS}	V_{CC}	V	V0 to V3 pins on the products without a booster LCD power supply range (The optimum value dependent on the LCD element in use.)
EPROM program power supply voltage	V_{PP}	—	V_{SS} + 13.0	V	MOD1 pin of the MB89P165
Operating temperature	T_A	–40	+85	°C	

*1: The minimum operating power supply voltage varies with the execution time (instruction cycle time) setting for the operating frequency.
A/D converter assurance accuracy varies with the operating power supply voltage.

*2: P32 and P33 are applicable only for procucts of the MB89160 series (without "A" suffix).
P40 to P47 and P60 to P67 are applicable when selected as ports.

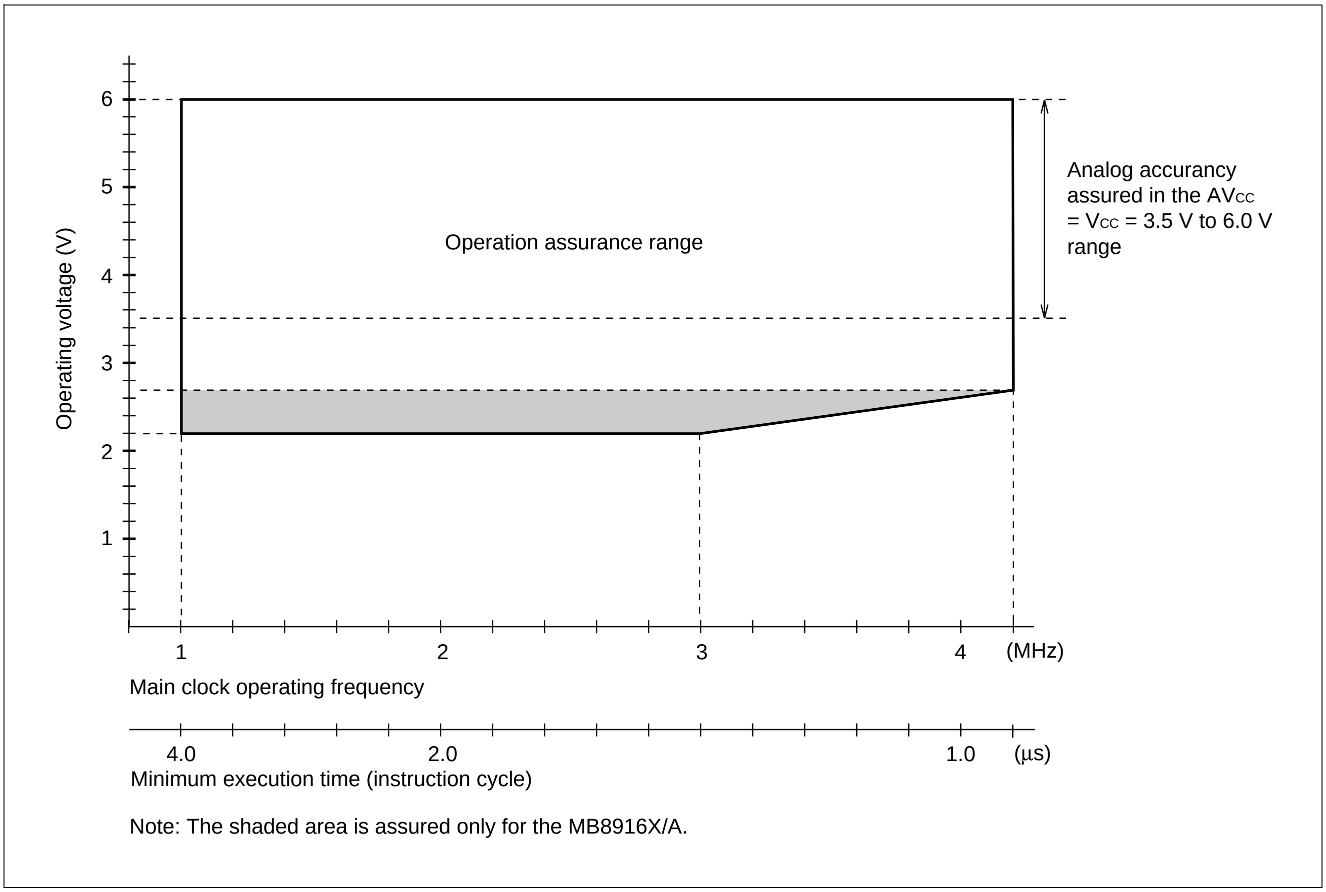


Figure 1 Operating Voltage vs. Main Clock Operating Frequency (Single-clock MB8916X/A and MB89P165/PV160)

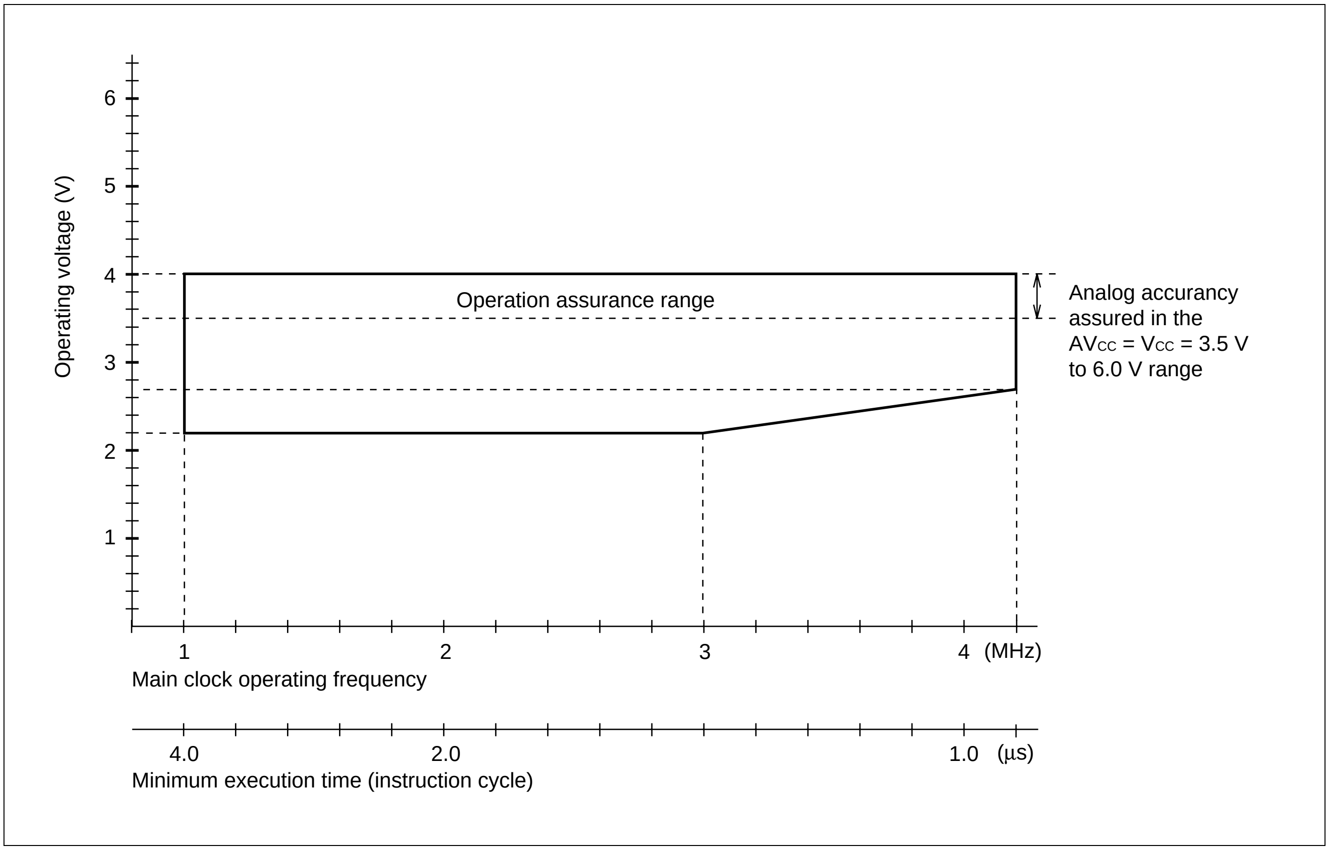


Figure 2 Operating Voltage vs. Main Clock Operating Frequency (Dual-clock MB8916X/A)

Figures 1 and 2 indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(1) Pin DC characteristics (V_{CC} = +5.0 V)

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, EC, SI, SCK, INT10 to INT13, INT20 to INT27	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
“L” level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, EC, SI, SCK, INT10 to INT13, INT20 to INT27	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_{D1}	P20 to P27, P33, P32, P40 to P47, P60 to P67	—	V_{SS} – 0.3	—	V_{SS} + 6.0*2	V	P20 to P27, P40 to P47, and P60 to P67 without pull-up resistor only
	V_{D2}	P50 to P57	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
“H” level output voltage	V_{OH1}	P00 to P07, P10 to P17	I_{OH} = –2.0 mA	2.4	—	—	V	
	V_{OH2}	P30, P31	I_{OH} = –6.0 mA	4.0	—	—	V	
“L” level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P71	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	P21, P26, P27	I_{OL} = 8.0 mA	—	—	0.4	V	
	V_{OL3}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.6	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, MOD0, MOD1, P30, P31	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor

(Continued)

(Continued)

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Open-drain output leakage current	I_{LO1}	P20 to P27, P32, P33, P40 to P47, P60 to P67, P70, P71	0.45 V < V_I < 6.0 V	—	—	±1	µA	Without pull-up resistor
	I_{LO2}	P50 to P57	0.45 V < V_I < V_{CC}	—	—	±1	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57, P60 to P67, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = +5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to SEG24		—	—	15	kΩ	
LCD divided resistance	R_{LCD}	—	Between V_{CC} and V0	300	500	750	kΩ	Products without a booster only
LCD controller/driver leakage current	I_{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG23	—	—	—	±1	µA	
Booster for LCD driving output voltage	V_{OV3}	V3	V1 = 1.5 V	4.3	4.5	4.7	V	Products with a booster only
	V_{OV2}	V2		2.9	3.0	3.1	V	
Reference output voltage for LCD driving	V_{OV1}	V1	I_{IN} = 0 µA	1.27	1.5	1.73	V	
Reference voltage input impedance	R_{RIN}	V1	—	600	1000	1400	kΩ	Procucts with a booster only
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}	f = 1 MHz	—	10	—	pF	

Note: For pins which serve as the segment (SEG8 to SEG24) and ports (P40 to P47, P50 to P57, and P60 to P67), see the port parameter when these pins are used as ports and the segment parameter when they are used as segments. P32 and P33 are applicable only for products of the MB89160 series (without “A” suffix). Applicable as external capacitor connection pins for products of the MB89160A series (with “A” suffix).

(2) Pin DC Characteristics (V_{CC} = +3.0 V)

(V_{CC} = 3.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17	I_{OH} = –1.0 mA	2.4	—	—	V	
	V_{OH2}	P30, P31	I_{OH} = –3.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70 to P71	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{\text{RST}}$	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL3}	P21, P26, P27	I_{OL} = 3.6 mA	—	—	0.4	V	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57, P60 to P67, $\overline{\text{RST}}$	V_I = 0.0 V	50	100	150	kΩ	With pull-up resistor

(3) Power Supply Current Characteristics (MB8916X)

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current[*1]	I_{CC1}	V_{CC}	F_{CH} = 4.2 MHz, V_{CC} = 5.0 V t_{inst}[*2] = 4/F_{CH} Main clock operation mode	—	5.0	10.0	mA	MB8916X/A, MB89PV160
				—	8.0	15.0	mA	MB89PV165
	I_{CC2}		F_{CH} = 4.2 MHz, V_{CC} = 3.0 V t_{inst}[*2] = 64/F_{CH} Main clock operation mode	—	1.5	2.0	mA	MB8916X/A, MB89PV160
				—	2.4	2.8	mA	MB89P165
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V t_{inst}[*2] = 2/F_{CL} Subclock operation mode	—	0.05	0.1	mA	MB8916X/A, MB89PV160
				—	1.0	3.0	mA	MB89PV165
	I_{CCS1}		F_{CH} = 4.2 MHz, V_{CC} = 5.0 V t_{inst}[*2] = 4/F_{CH} Main clock sleep mode	—	2.5	5.0	mA	MB8916X/A, MB89PV160, MB89PV165
	I_{CCS2}		F_{CH} = 4.2 MHz, V_{CC} = 3.0 V t_{inst}[*2] = 64/F_{CH} Main clock sleep mode	—	1.0	1.5	mA	
	I_{CCSL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V t_{inst}[*2] = 2/F_{CL} Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V Watch mode	—	10	15	µA	MB8916X, MB89P165-1XX, MB89PV160
	I_{CCT2}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V • Watch mode • During reference voltage generator and booster operation	—	250	400	µA	MB8916XA, MB89P165-2XX
	I_{CCH}		T_A = +25°C, V_{CC} = 5.0 V Stop mode	—	0.1	1.0	µA	MB8916X
				—	0.1	10	µA	MB89PV160, MB89P165-1XX
	I_A	AV_{CC}	F_{CH} = 4.2 MHz, V_{CC} = 5.0 V	—	1.0	3.0	mA	When A/D conversion is activated

*1: The power supply current is measured at the external clock, open output pins, and the external LCD dividing resistor (or external input for the reference voltage). In the case of the MB89PV160, the current consumed by the connected EPROM and ICE is not included.

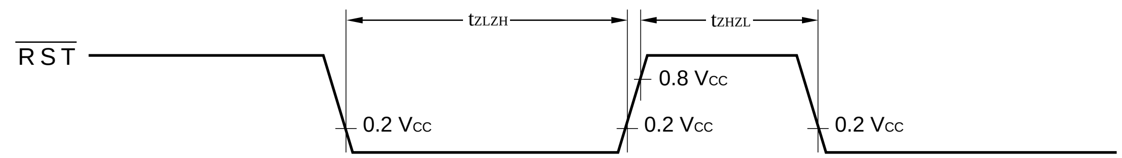
*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V ±10 %, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}	—	ns	
$\overline{RST}$ "H" pulse width	t_{ZHZL}		24 t_{XCYL}	—	ns	

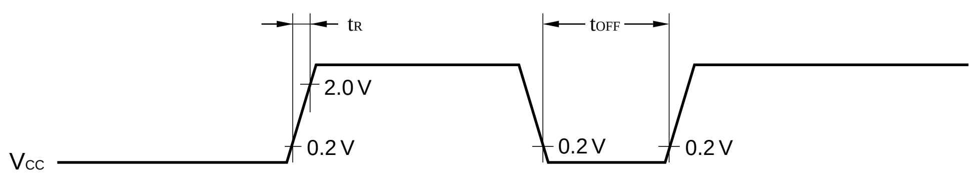


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}	—	1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

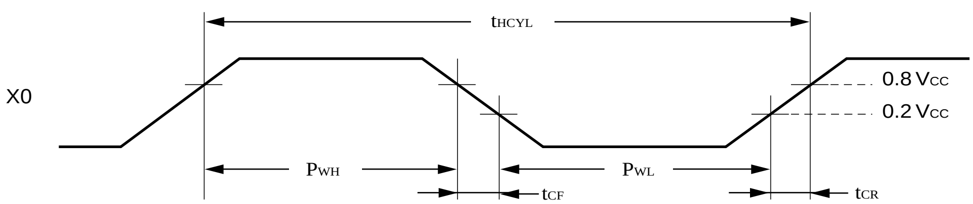


(3) Clock Timing

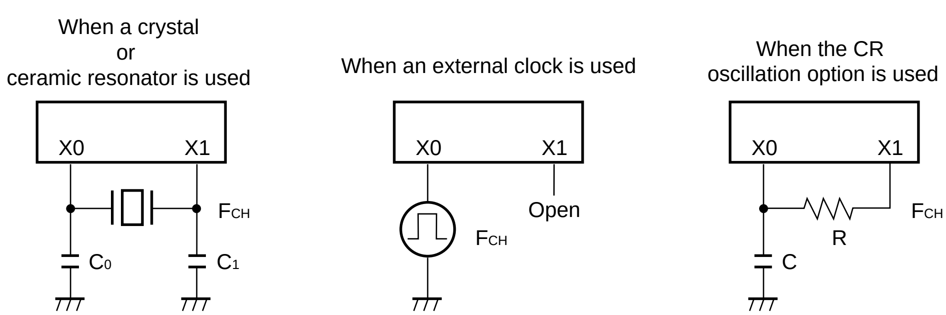
(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	4.2	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	238	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	24	ns	

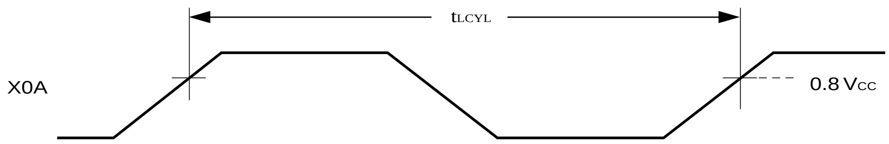
Main Clock Timing and Conditions



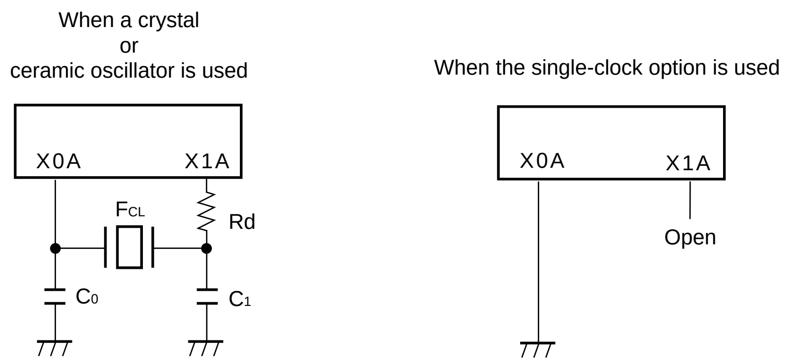
Main Clock Conditions



Subclock Timing and Conditions



Subclock Conditions



(4) Instruction Cycle

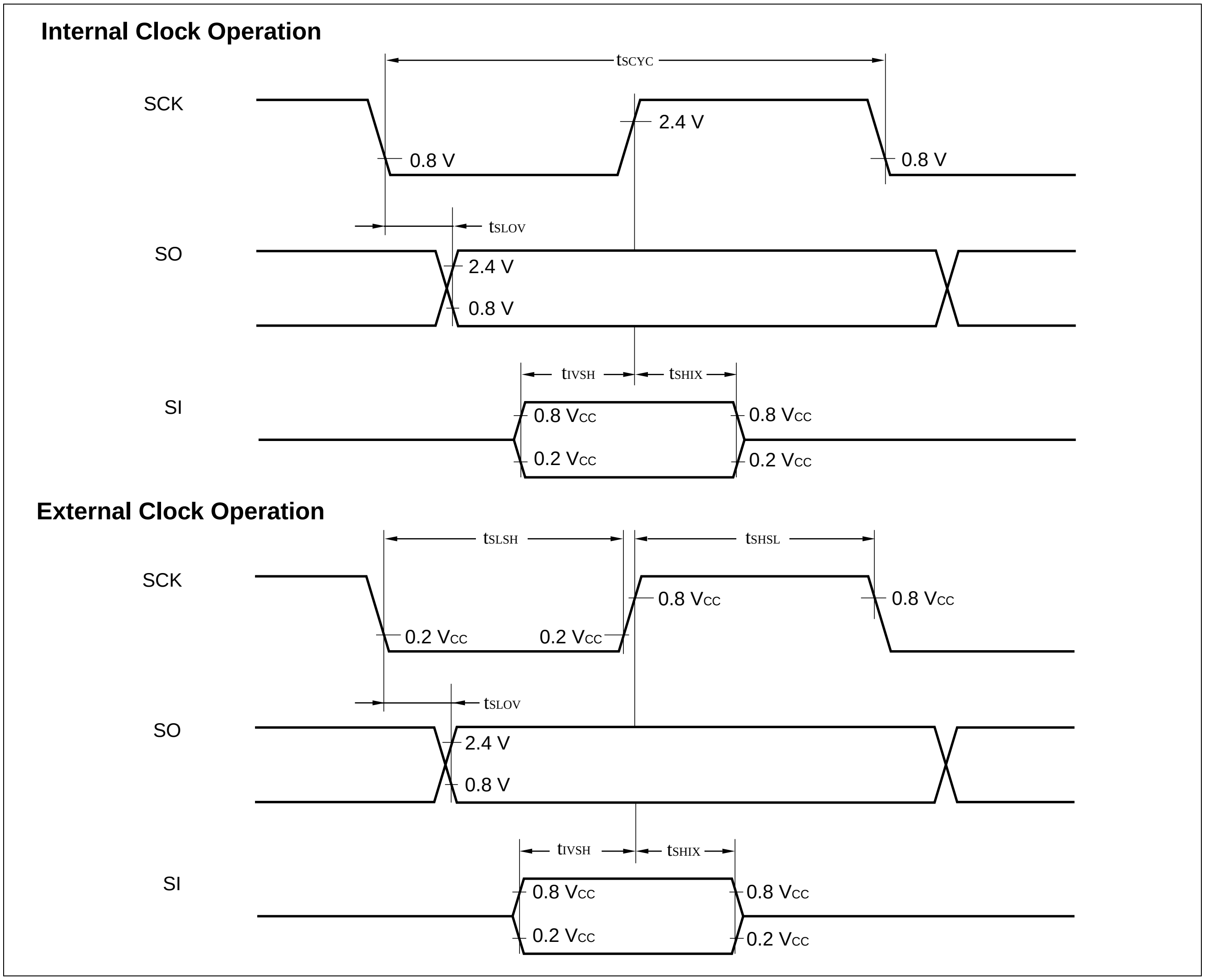
Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ t_{inst} = 1.0 µs at F_{CH} = 4 MHz
		$2/F_{CL}$	µs	t_{inst} = 62 µs at F_{CL} = 32.768 kHz

(5) Serial I/O Timing

(V_{CC} = +5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	
Serial clock "H" pulse width	t_{SHSL}	SCK	External clock operation	1 t_{inst}*	—	µs	
Serial clock "L" pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see "(4) Instruction Cycle."

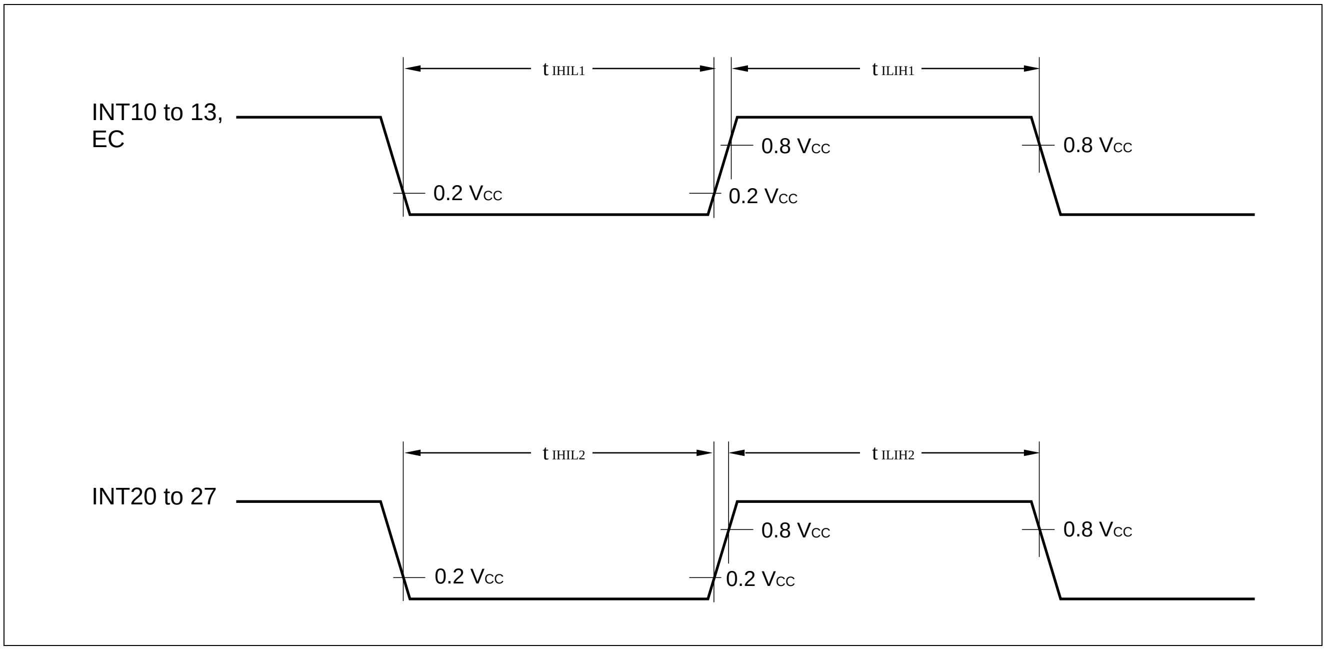


(6) Peripheral Input Timing

(V_{CC} = +5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT10 to INT13, EC	1 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		1 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	INT20 to INT27	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



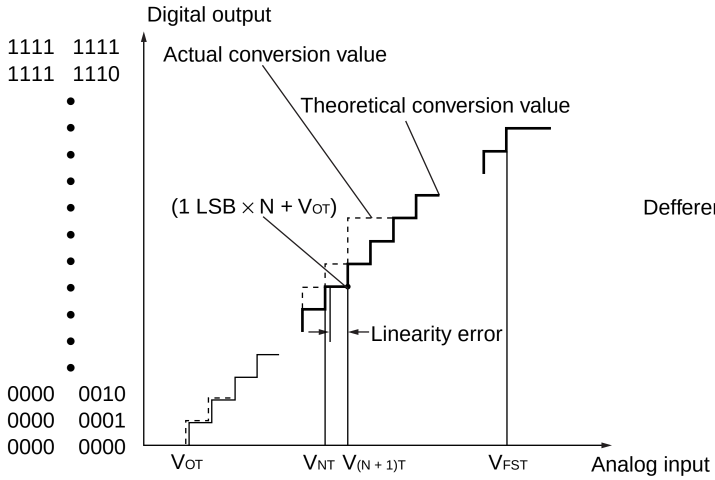
5. A/D Converter Electrical Characteristics

(3 MHz, $AV_{CC} = V_{CC} = +3.5$ V to +6.0 V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			AVR = AV_{CC}	—	—	±1.5	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.0 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.0 LSB	mV	
Full-scale transition voltage	V_{FST}			AVR – 3.0 LSB	AVR – 1.5 LSB	AVR	mV	
Interchannel disparity	—			—	—	0.5	LSB	
A/D mode conversion time			—	—	44 t_{inst}	—	µs	
Sense mode conversion time				—	12 t_{inst}	—	µs	
Analog port input current	I_{AI}	AN0 to AN7		—	—	10	µA	
Analog input voltage	—			0.0	—	AVR	V	
Reference voltage	—	AVR		2.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		AVR = 5.0 V, when A/D conversion is activated	—	100	—	µA	
	I_{RH}		AVR = 5.0 V, when A/D conversion is stopped	—	—	1	µA	

(1) A/D Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 8, analog voltage can be divided into 2^8=256.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



$$1\text{ LSB} = \frac{\text{AVR}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\text{ LSB} \times N + V_{OT})}{1\text{ LSB}}$$

$$\text{Defferential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\text{ LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\text{ LSB} \times N + 1\text{ LSB})}{1\text{ LSB}}$$

(2) Precautions

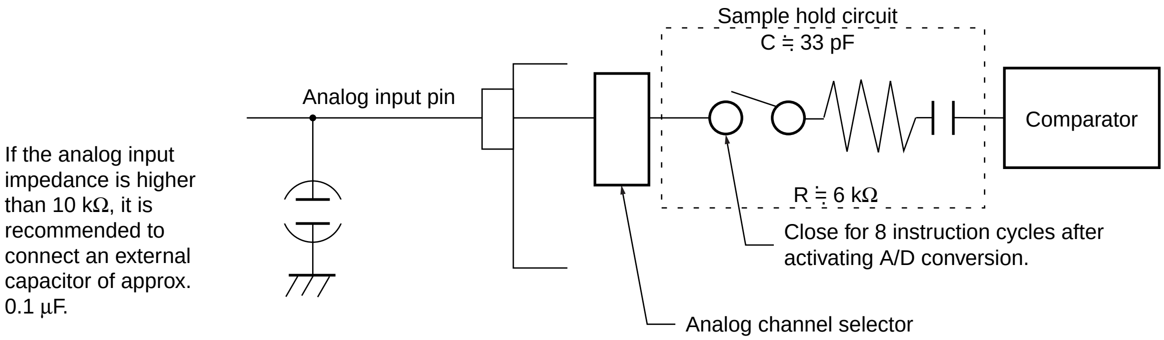
- **Input impedance of analog input pins**

The A/D converter contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.

Analog Input Equivalent Circuit

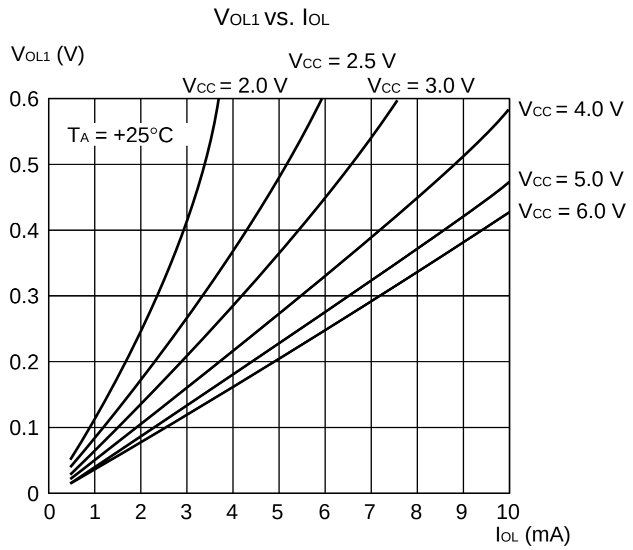


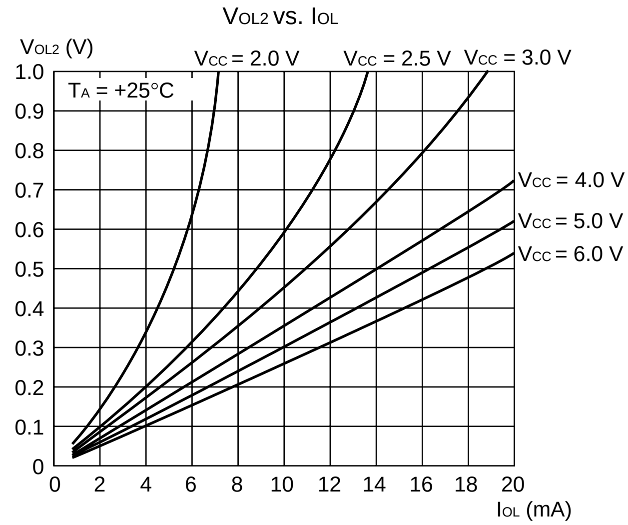
- **Error**

The smaller the |AVR – AV_{SS}|, the greater the error would become relatively.

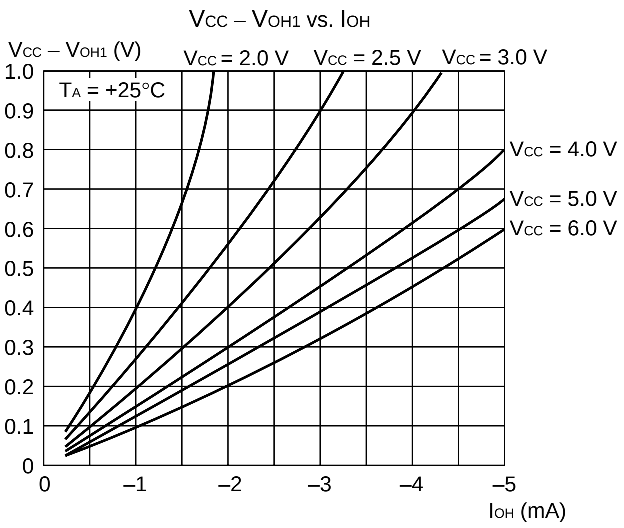
■ EXAMPLE CHARACTERISTICS

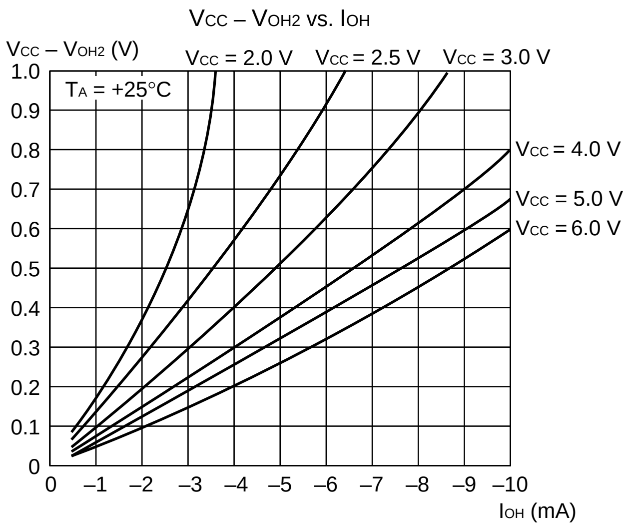
(1) "L" Level Output Voltage



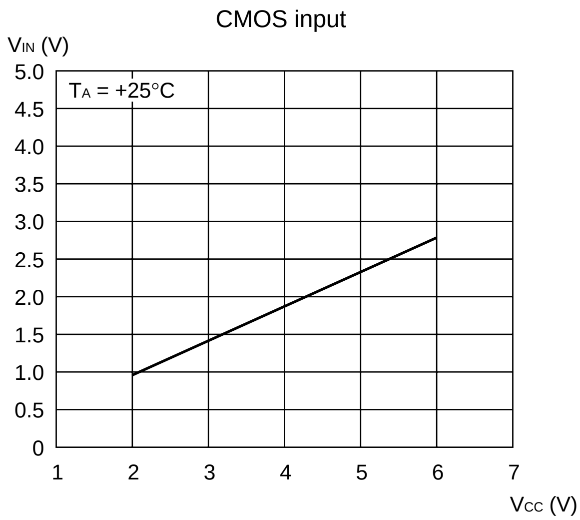


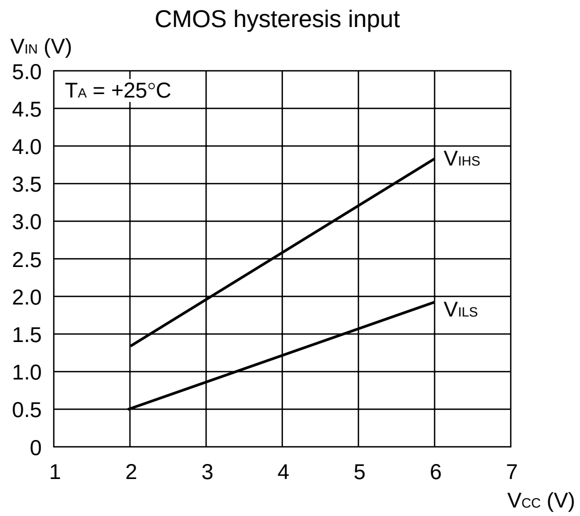
(2) "H" Level Output Voltage





(3) “H” Level Input Voltage/“L” level Input Voltage

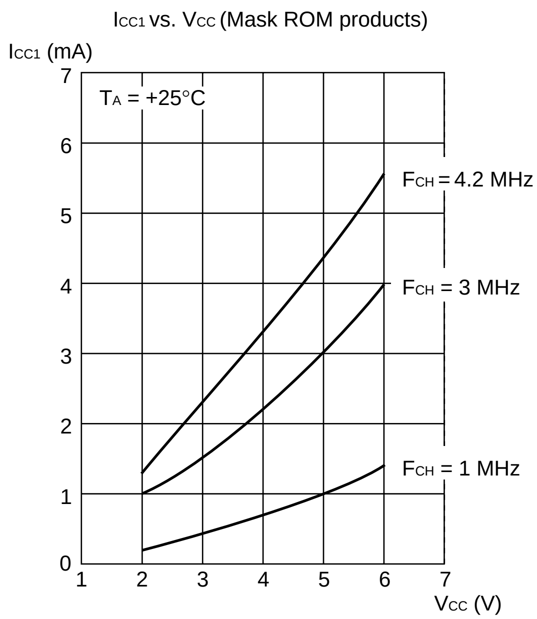


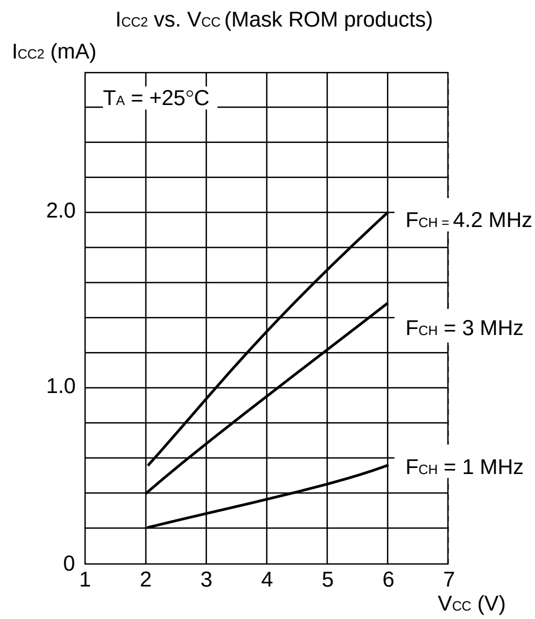


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(4) Power Supply Current (External Clock)





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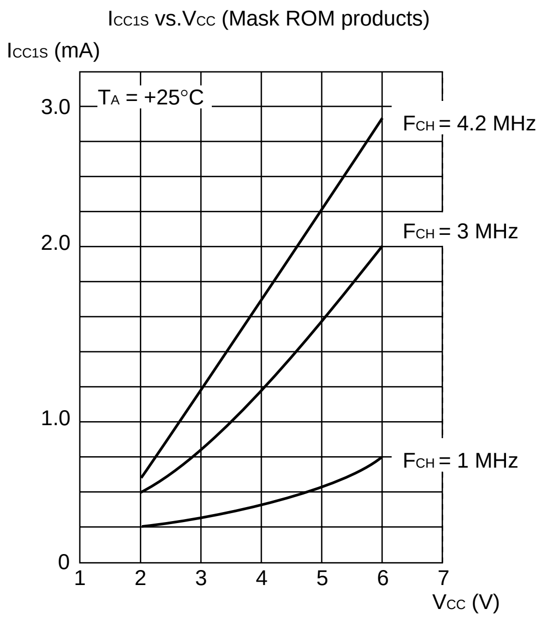
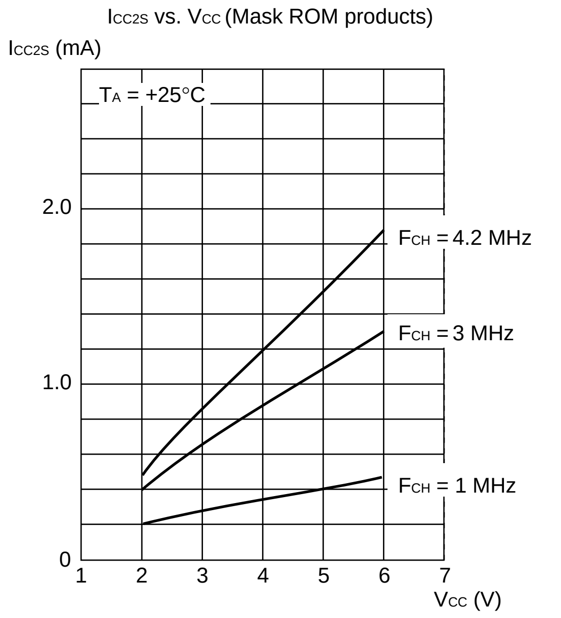
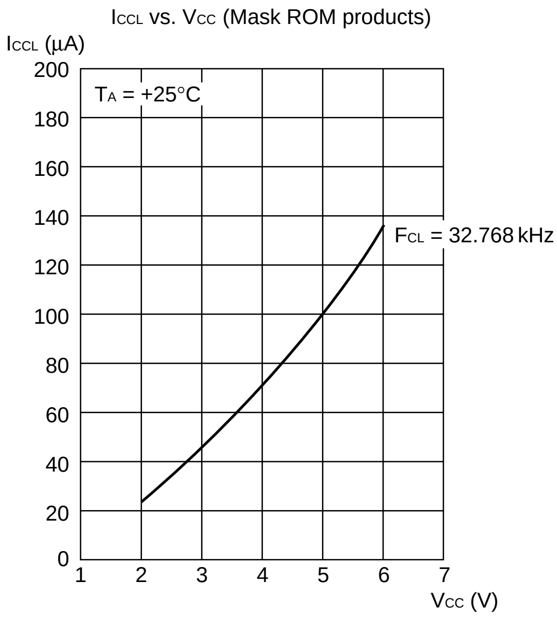
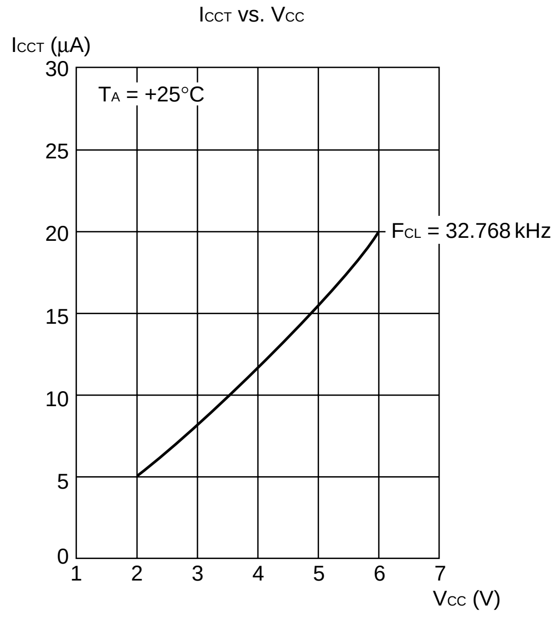

ICC1S vs.VCC (Mask ROM products)
ICC1S (mA)
TA = +25°C
FCH = 4.2 MHz
FCH = 3 MHz
FCH = 1 MHz
3.0
2.0
1.0
0
1
2
3
4
5
6
7
VCC (V)

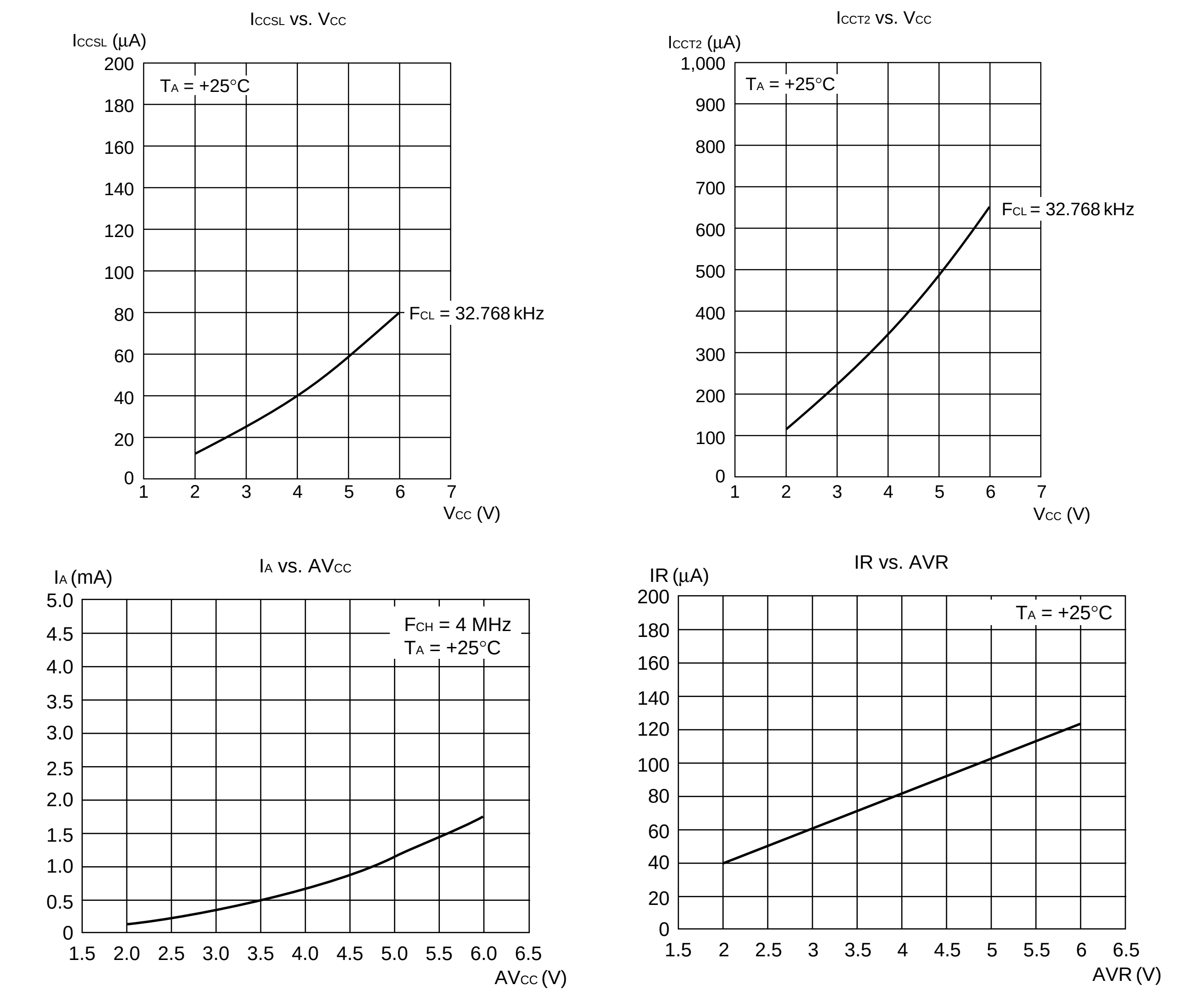

ICC2S vs. VCC (Mask ROM products)
ICC2S (mA)
TA = +25°C
FCH = 4.2 MHz
FCH = 3 MHz
FCH = 1 MHz
2.0
1.0
0
1
2
3
4
5
6
7
VCC (V)


ICCL vs. VCC (Mask ROM products)
ICCL (µA)
TA = +25°C
FCL = 32.768 kHz
200
180
160
140
120
100
80
60
40
20
0
1
2
3
4
5
6
7
VCC (V)

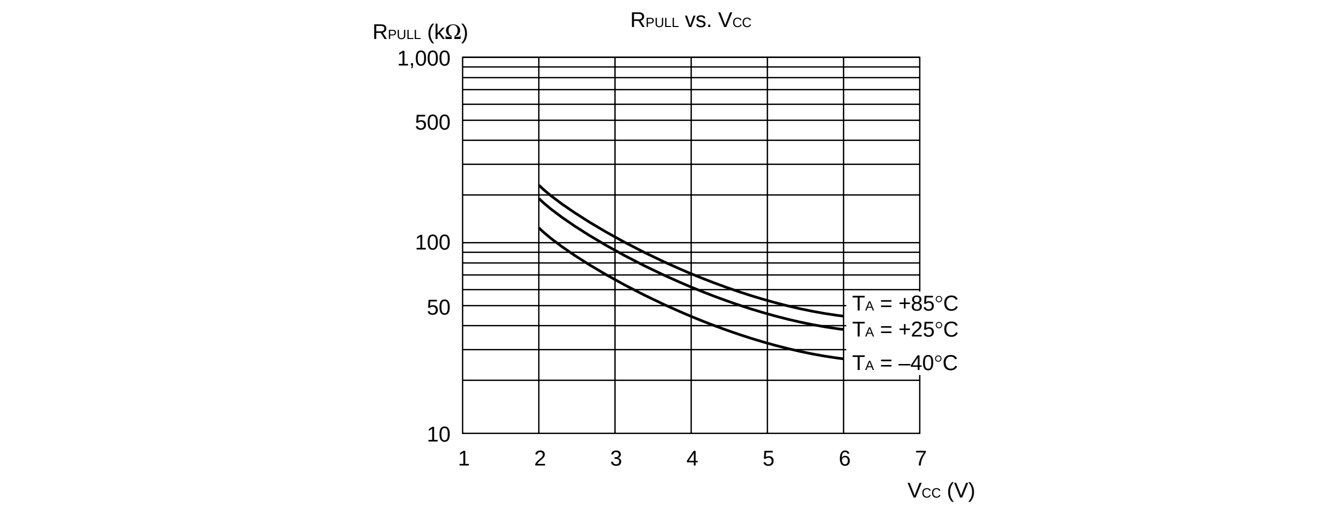

ICCT vs. VCC
ICCT (µA)
TA = +25°C
FCL = 32.768 kHz
30
25
20
15
10
5
0
1
2
3
4
5
6
7
VCC (V)

(Continued)

(Continued)



(5) Pull-up Resistance



■ MASK OPTIONS

Part number	MB89161/3/5	MB89P165	MB89PV160
Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
Pull-up resistors (SEG) P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57, P60 to P67	Slectable per pin (The pull-up resistors for P40 to P47 and P60 to P67 are only selectable when these pins are not set as segment outputs. When the A/D is used, P50 to P57 are must not selected.)	Can be set per pin (P20 to P27, P40 to P47, and P60 to P67 are available only for without a pull-up resistor.)	Fixed to without pull-up resistor
Power-on reset (POR) With power-on reset Without power-on reset	Selectable	Selectable	Fixed to with power-on reset
Selection of oscillation stabilization time (OSC) • The initial value of the oscillation stabilization time for the main clock can be set by selecting the values of the WTM1 and WTM0 bits on the right.	Selectable OSC 0 : $2^2/F_{CH}$ 1 : $2^{12}/F_{CH}$ 2 : $2^{16}/F_{CH}$ 3 : $2^{18}/F_{CH}$	Selectable WTM1 WTM0 0 0 : $2^2/F_{CH}$ 0 1 : $2^{12}/F_{CH}$ 1 0 : $2^{16}/F_{CH}$ 1 1 : $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{16}/F_{CH}$
Main clock oscillation type (XSL) Crystal or ceramic resonator CR	Selectable	Crystal or ceramic only	Fixed to crystal or ceramic
Reset pin output (RST) With reset output Without reset output	Selectable	Selectable	Fixed to with reset output
Clock mode selection (CLK) Dual-clock mode Single-clock mode	Selectable	Selectable	Fixed to dual-clock mode

- **Segment Options**

No.	Part number	MB89161/3/5	MB89P165	MB89PV160
	Specifying procedure	**Specify when ordering masking**	**Select by version number**	**Select by version number**
7	LCD output pin configuration choices	Specify by the option combinations listed below		
	SEG = 4: P40 to P47 segment output P60 to P67 segment output P70, P71 common output	Specify as SEG = 4	–101 : SEG 24 pins –201 COM 4 pins	–101 : SEG 24 pins COM 4 pins
	SEG = 3: P40 to P43 segment output P44 to P47 port output P60 to P67 segment output P70, P71 common output	Specify as SEG = 3	–102 : SEG 20 pins –202 COM 4 pins	–102 : SEG 20 pins COM 4 pins
	SEG = 2: P40 to P47 port output P60 to P67 segment output P70, P71 common output	Specify as SEG = 2	–103 : SEG 16 pins –203 COM 4 pins	–103 : SEG 16 pins COM 4 pins
	SEG = 1: P40 to P47 port output P60 to P63 segment output P64 to P67 port output P70, P71 port output	Specify as SEG = 1	–104 : SEG 12 pins COM 2 pins	–104 : SEG 12 pins COM 2 pins
	SEG = 0: P40 to P47 port output P60 to P67 port output P70, P71 port output	Specify as SEG = 0	–105 : SEG 8 pins COM 2 pins	–105 : SEG 8 pins COM 2 pins

■ VERSIONS

Version				Features	
Mass production product	**One-time PROM product**	**EPROM product**	**Piggyback/ evaluation product**	**Number of seg- ment pins**	**Booster**
MB89160A series	MB89P165-201 -202 -203	MB89W165-201 -202 -203	—	24 (4 commons) 20 (4 commons) 16 (4 commons)	Yes
MB89160 series	MB89P165-101 -102 -103 -104 -105	MB89W165-101 -102 -103 -104 -105	MB89PV160-101 -102 -103 -104 -105	24 (4 commons) 20 (4 commons) 16 (4 commons) 12 (2 commons) 8 (2 commons)	No

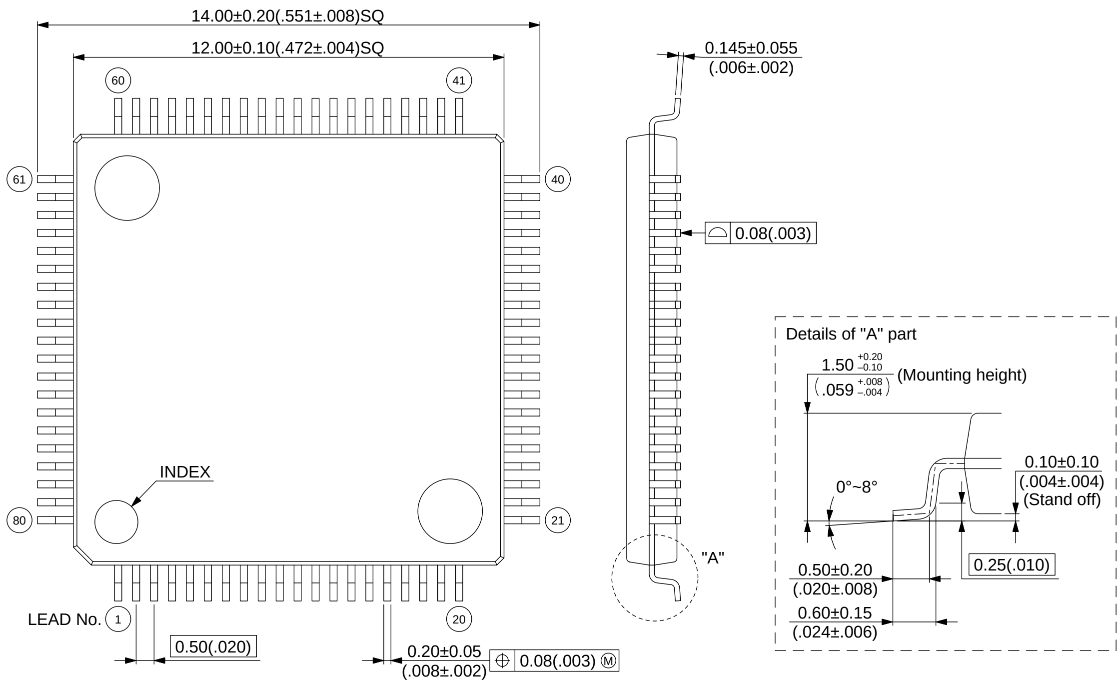
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89161-PFV MB89161A-PFV MB89163-PFV MB89163A-PFV MB89165-PFV MB89165A-PFV MB89P165-×××-PFV	80-pin Plastic LQFP (FPT-80P-M05)	
MB89161-PF MB89161A-PF MB89163-PF MB89163A-PF MB89165-PF MB89165A-PF MB89P165-×××-PF	80-pin Plastic QFP (FPT-80P-M06)	
MB89161-PFM MB89161A-PFM MB89163-PFM MB89163A-PFM MB89165-PFM MB89165A-PFM MB89P165-×××-PFM	80-pin Plastic LQFP (FPT-80P-M11)	
MB89W165-×××-PF	80-pin Ceramic QFP (FPT-80C-A02)	
MB89PV160-×××-PF	80-pin Ceramic MQFP (MQP-80C-P01)	

Note: For information on ×××, see section “■ Versions.”

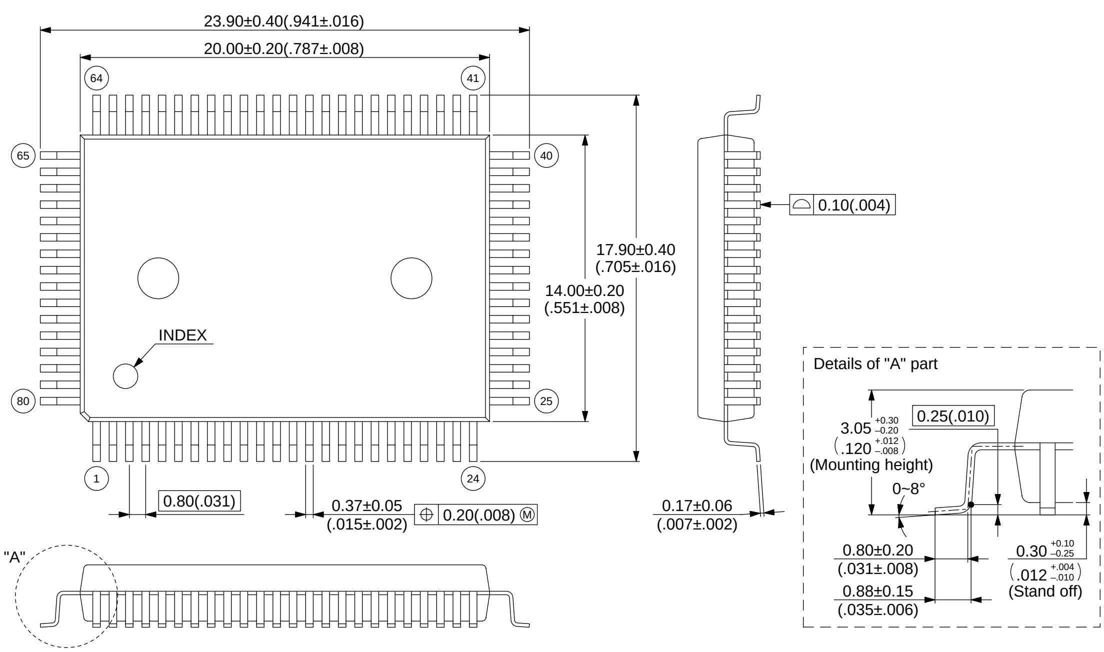
■ PACKAGE DIMENSIONS

80-pin plastic LQFP
(FPT-80P-M05)



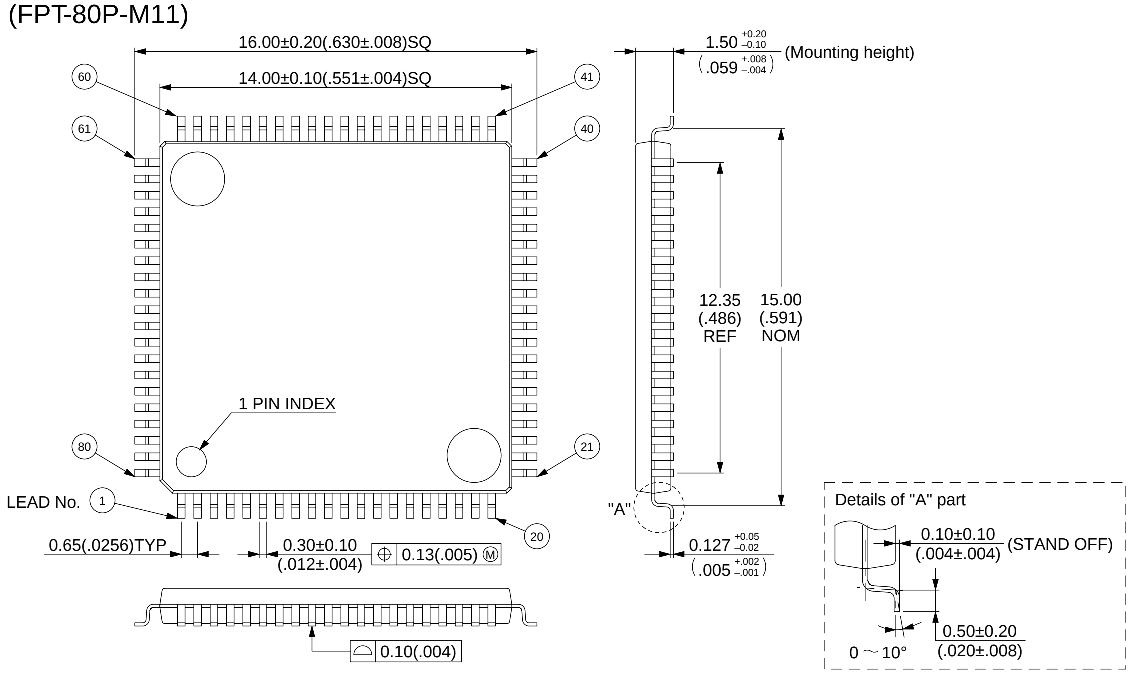
Dimensions in mm (inches).

80-pin plastic QFP
(FPT-80P-M06)



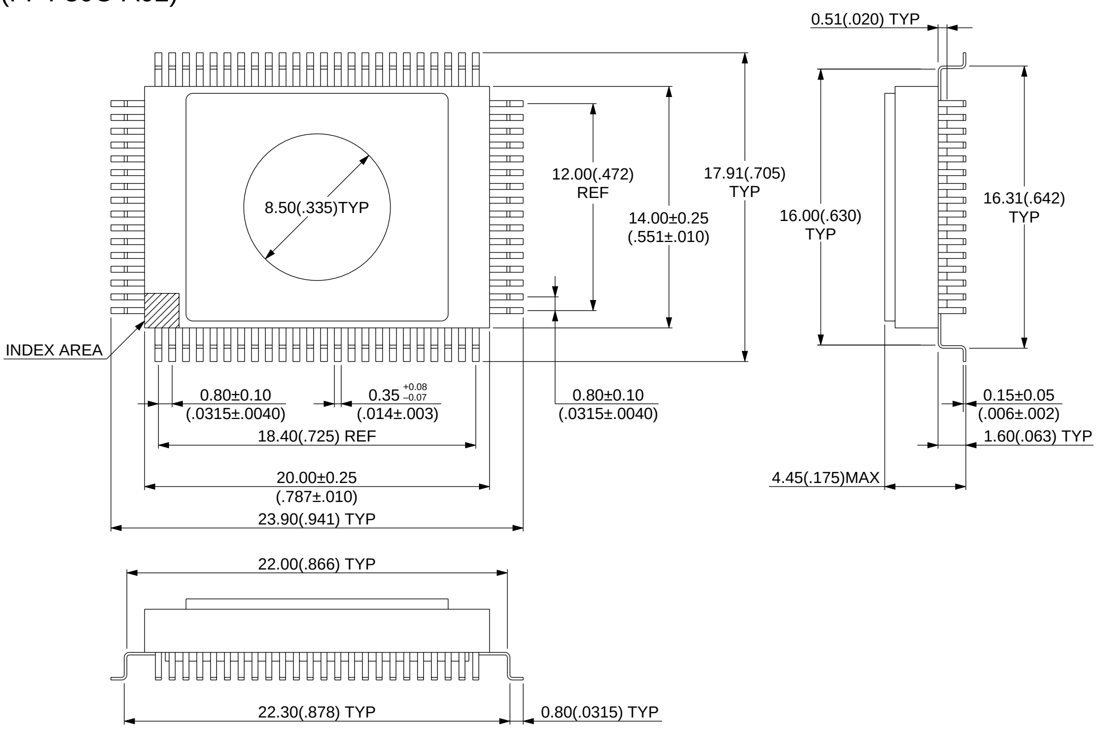
Dimensions in mm (inches).

80-pin plastic LQFP
(FPT-80P-M11)



Dimensions in mm (inches).

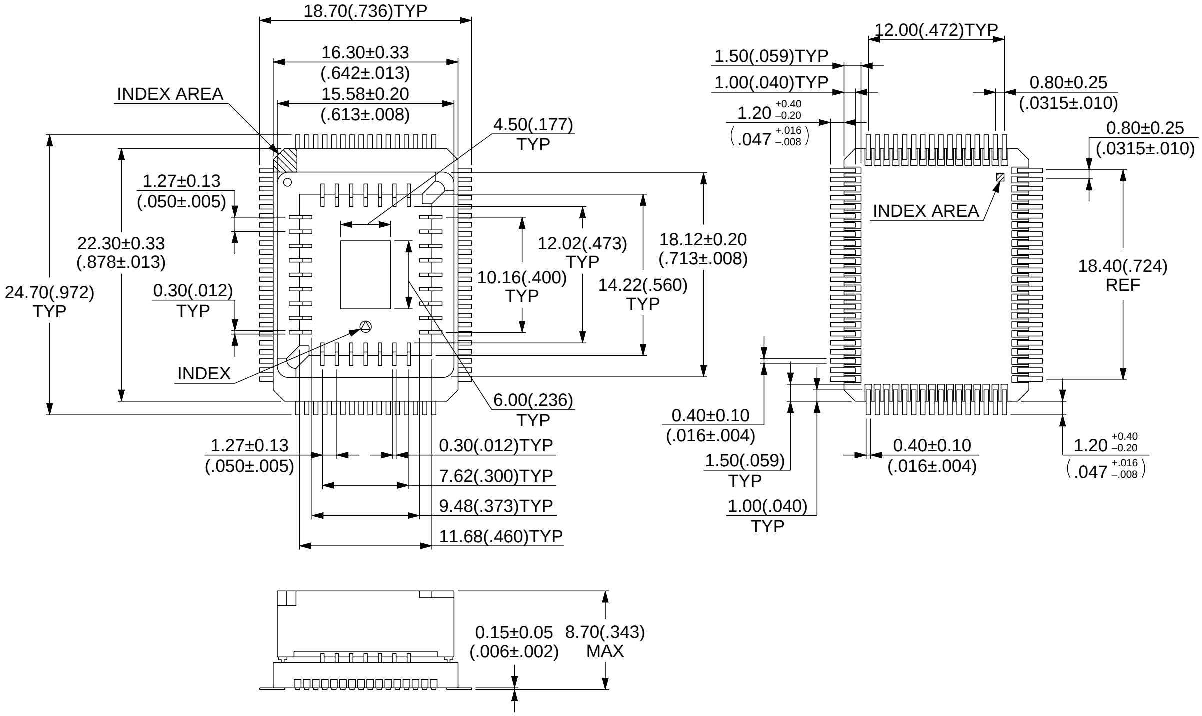
80-pin ceramic QFP
(FPT-80C-A02)



Dimensions in mm (inches).

(Continued)

80-pin ceramic MQFP
(MQP-80C-P01)



Dimensions in mm (inches).

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