FUJITSU

# TTL TWO-PHASE CLOCK GENERATOR AND DRIVER

# MB 8867
# MB 8867E

October 1982
Edition 2.0

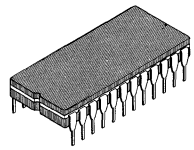
## TWO-PHASE MICROPROCESSOR CLOCK

The Fujitsu MB 8867 is an advanced Microprocessor Clock Generator/Driver LSI manufactured with Fujitsu's bipolar TTL process. The circuit generates non-overlapping two-phase clock signals for the Fujitsu MBL 6800 microprocessor unit or similiar single +5 volt MPU's. Additionally, two-phase TTL clock signals synchronized with the MPU clock are provided, as well as an MPU data strobe, reset/clock controls for the memory interrupt, and an automatic power-up reset. With the MB 8867, the entire MPU timing system can be designed with one chip and a minimum of external components.

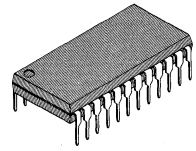
A built-in oscillator permits external timing control by a crystal; or RC network timing can be utilised for less critical applications. In the former, the internal frequency divider is rate selectable, so that the output frequency is either 1/4 or 1/16 of the source frequency.

Driver circuits are included on the MB 8867 which eliminates the need for external buffer gates and reduces system package count. Output drivers are short-circuit protected.

- Single chip two-phase clock generator with on-chip drivers
- Short-circuit protected outputs
- Complete MPU system timing network including dynamic memory refresh
- Single +5V power supply
- Low power consumption: 450 mW typ.
- Reliable TTL process
- Two-phase TTL clock signals
- Data strobe for memory control synchronization
- Automatic power-up and manual reset
- Clock controls for memory interrupt
- Crystal or RC network frequency source
- Selectable source frequency options
- Works with high speed microprocessors
- Standard 24 pin package
- Minimum external components required

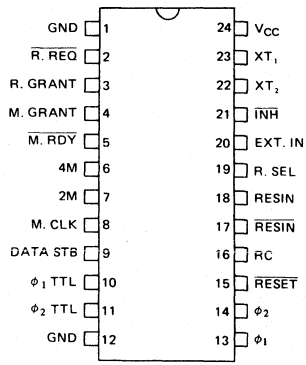


**CERAMIC PACKAGE**
**DIP-24C-C01**



**PLASTIC PACKAGE**
**DIP-24P-M01**

**PIN ASSIGNMENT**




**ABSOLUTE MAXIMUM RATINGS (See NOTE)**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| $V_{CC}$ Pin Potential to GND Pin | $V_{CC}$ | +7 Max. | V |
| Input Voltage | $V_{IN}$ | -0.5 to +5.5 | V |
| Output Voltage | $V_O$ | -0.5 to +5.5 | V |
| Operating Temperature | $T_{OP}$ | -25 to +125 | °C |
| Storage Temperature | $T_{stg}$ | -55 to +150 | °C |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

## INTRODUCTION

The MB 8867 provides the two-phase clock signal input for the MBL 6800 microprocessor or any similiar timing signal required in a microcomputer system. The IC incorporates the necessary logic to ensure that these clock signals ($\phi_1$ and $\phi_2$) are non-overlapping; and, additionally, the MB 8867 is designed to accomodate direct connection to high capacitive loads (typically 170 pF) without additional buffering.

Most high speed microprocessor controlled systems utilize dynamic random access memories in order to minimize system cost and power consumption. A major design problem in such systems is to provide dynamic RAM refresh timing signals synchronized with the operation of the MPU. The MB 8867 solves this problem with its refresh control pins, $\overline{\text{R. REQ}}$ and R. GRANT (Refresh Request and Refresh Grant).

In the pin description below, all TTL compatible inputs and outputs are indicated by "TTL input" or "TTL output" and later refered to in the characteristic tables by these terms.

## DESCRIPTION OF PINS

**$XT_1$, $XT_2$**
Two pins are provided for the connection of an external crystal. The crystal selected should be either four or sixteen times the desired output clock frequency. Small picofarad capacitors are provided internally in the oscillator circuitry. However, for fine oscillation control, an additional small capacitor (3 pf to 10 pf) in series with the crystal may be used.

**EXT. IN** (TTL input)
This input is used for an external RC network to provide timing control when a crystal is not utilized. Note that, like the crystal source, the input frequency will be either four or sixteen times the desired output clock frequency. See the APPLICATIONS INFORMATION section of this data sheet for proper external component connection.

**M. CLK** (TTL output)
Provides a reference clock driver for external memory synchronous with $\phi_2$. The frequency is identical to the output clock frequency ($\phi_1$, $\phi_2$), but is not affected by switching $\overline{\text{R. REQ}}$ (refresh cycle).

**2M, 4M** (TTL outputs)
2M and 4M are pulse train drivers with frequencies of two times and four times the output clock ($\phi_1$, $\phi_2$) frequency, respectively. When R. SEL is low, EXT. IN and 4M are in opposite phase. Therefore, ring oscillation can be generated without an external crystal by inserting an appropriate RC network between 4M and EXT. IN. See the APPLICATIONS INFORMATION section of this data sheet for circuit information.

**RC**
Provides automatic power-up reset function by utilizing an external RC network. $\overline{\text{RESET}}$ goes low with the rising edge of $\phi_1$ when RC is less than 0.8V; $\overline{\text{RESET}}$ goes high when RC is greater than 2/3 $V_{CC}$. Therefore, automatic power-up reset is obtained by providing a delay slower than the rise time of $V_{CC}$.

**$\overline{\text{INH}}$** (TTL input)
Used to control internal oscillation. The oscillator is operational when $\overline{\text{INH}}$ is brought high (open); the oscillator is inhibited when $\overline{\text{INH}}$ is brought low.

**R. SEL** (TTL input)
When R. SEL is high (open), the one-by-four frequency divider is operational; when R. SEL is low, the divider is bypassed. As an example, a 16MHz external time source will generate a 1MHz output clock frequency if R. SEL is high.

**$\phi_1$, $\phi_2$**
MPU output clock drivers. $\phi_1$ and $\phi_2$ have non-overlapping control.

**$\phi_1$ TTL, $\phi_2$ TTL** (TTL outputs)
TTL level output clock drivers synchronized with $\phi_1$ and $\phi_2$, respectively.

**DATA STB** (TTL output)
Data strobe signal for memory read and write operations. DATA STB goes high one cycle of the 4M output frequency after $\phi_2$ goes high; DATA STB goes low just before $\phi_2$ goes low. If $\overline{\text{M. RDY}}$ is not interrupted, DATA STB will maintain its high state during the last quarter cycle of $\phi_2$.

**RESIN, $\overline{\text{RESIN}}$** (TTL outputs)
Provides manual input reset. After reset, RESIN is brought low and $\overline{\text{RESIN}}$ is open. Manual reset occurs when these states are reversed. An internal flip-flop prevents switch-on chattering.

**$\overline{\text{RESET}}$** (TTL output open-collector)
Open-collector output pin to provide the reset function.

**$\overline{\text{R. REQ}}$,** (TTL input) **R. GRANT** (TTL output)
These pins provide memory refresh control. $\overline{\text{R. REQ}}$ is usually kept high. To start the refresh cycle, $\overline{\text{R. REQ}}$ is brought low, and then R. GRANT goes high at the next falling edge of the memory clock. Then $\overline{\text{R. REQ}}$ is brought high, and R. GRANT will go low at the next falling edge of the memory clock. $\phi_1$ will stay high and $\phi_2$ will stay low during refresh. R. GRANT may be connected to the three state control of the MPU system to provide refresh for dynamic memories and DMA (Direct Memory Access) in the "cycle steal" mode.

**$\overline{\text{M. RDY}}$,** (TTL input) **M. GRANT** (TTL output)
Provided for low speed memory control. $\overline{\text{M. RDY}}$ is usually kept high. When $\overline{\text{M. RDY}}$ is brought low, M. GRANT goes low on the next falling edge of 4M. The high state of $\phi_2$ is extended for the period that M. GRANT is low. At the same

time, the high state of M.CLK and DATA STB are maintained. This permits a long time period for memory read operations.

### $V_{CC}$

Connected to the +5V supply. By-pass capacitors are recommended if the supply rail is long in order to reduce supply impedance.

### GND 1, GND 2

Two ground terminals are provided in order to reduce internal impedance paths.

**Fig. 1—MB 8867 BLOCK DIAGRAM**

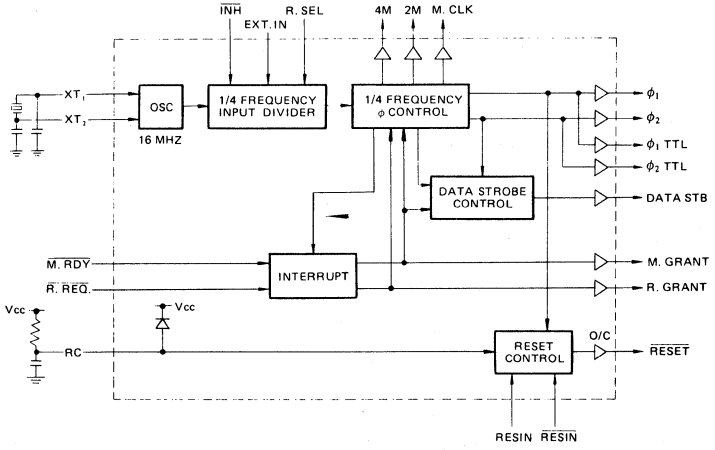
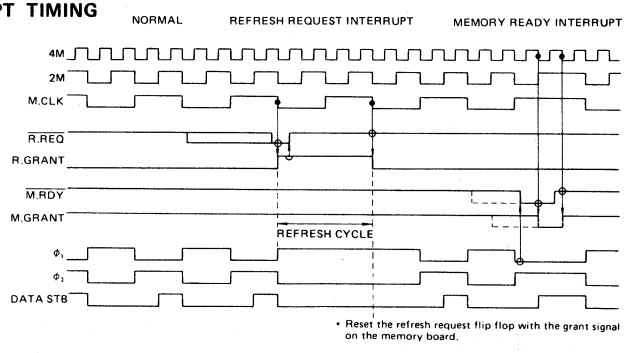


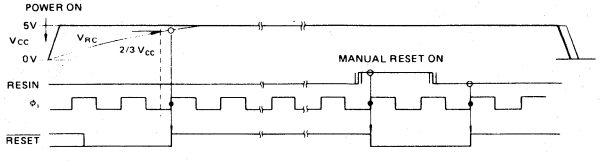

**Fig. 2—SYSTEM TIMING DIAGRAM**

● **MEMORY INTERRUPT TIMING**




* Reset the refresh request flip flop with the grant signal on the memory board.

● **POWER-UP RESET TIMING**



## GUARANTEED OPERATING CONDITIONS
(Referenced to GND)

| Parameter | Symbol | Value | | | Unit | Operating Temperature |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V | 0°C to +70°C |
| Input High Voltage (TTL inputs) | $V_{IHT}$ | 2 | | | V | |
| Input High Voltage (RC) | $V_{IHR}$ | 4.5 | | | V | |

## DC CHARACTERISTICS *
(Full Guaranteed Operating Ranges unless otherwise noted.)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Output High Voltage | | | | | |
| $\phi_1, \phi_2$ ($I_{OH}$=-0.2mA, $V_{CC}$=5.25V) | $V_{OH}$ | 4.95 | | | V |
| TTL outputs except $\overline{RESET}$ ($I_{OH}$=-0.4mA, $V_{CC}$=4.75V) | | 2.4 | | | V |
| Output Low Voltage | | | | | |
| $\phi_1, \phi_2$ ($I_{OL}$=1.8mA, $V_{CC}$=4.75V) | $V_{OL}$ | | | 0.3 | V |
| TTL inputs ($I_{OL}$=16mA, $V_{CC}$=4.75V) | | | | 0.4 | V |
| Input Clamp Diode Voltage | | | | | |
| TTL inputs ($I_{IC}$=-12mA, $V_{CC}$=4.75V) | $V_{IC}$ | | | 1.5 | V |
| Input High Current | | | | | |
| EXT IN ($V_{CC}$=5.25V, $V_{IN}$=2.4V) | $I_{IH}$ | | | 40 | μA |
| $\overline{R.REQ}$, $\overline{M.RDY}$, RESIN, $\overline{RESIN}$, R.SEL, $\overline{INH}$ ($V_{CC}$=4.75V, $V_{IN}$=2.4V) | | -100 | | | μA |
| RC ($V_{CC}$=5.25V, $V_{IN}$=5.25V) | | | | 10 | μA |
| Input Low Current | | | | | |
| EXT IN ($V_{CC}$=5.25V, $V_{IN}$=0.4V) | $I_{IL}$ | | | -1.6 | mA |
| $\overline{R.REQ}$, $\overline{M.RDY}$, RESIN, $\overline{RESIN}$ ($V_{CC}$=5.25V, $V_{IN}$=0.4V) | | | | -3.2 | mA |
| R.SEL, $\overline{INH}$ ($V_{CC}$=5.25V, $V_{IN}$=0.4V) | | | | -4.8 | mA |
| Power Supply Current | | | | | |
| ($V_{CC}$=4.75V, $XT_2$=0V) | $I_{CC}$ | 60 | | | mA |
| ($V_{CC}$=5.25V, $XT_2$=0V) | | | | 160 | mA |
| Output High Current | | | | | |
| $\overline{RESET}$ ($V_{CC}$=4.5V, $V_{OH}$=5.5V) | $I_{OH}$ | | | 250 | μA |
| Output Short Circuit Current | | | | | |
| $\phi_1, \phi_2$ ($V_{OL}$=0V, $V_{CC}$=5.25V) | $I_{OS}$ | -33 | | -100 | mA |
| TTL inputs except $\overline{RESET}$ ($V_{OL}$=0V, $V_{CC}$=5.25V) | | -18 | | -55 | mA |

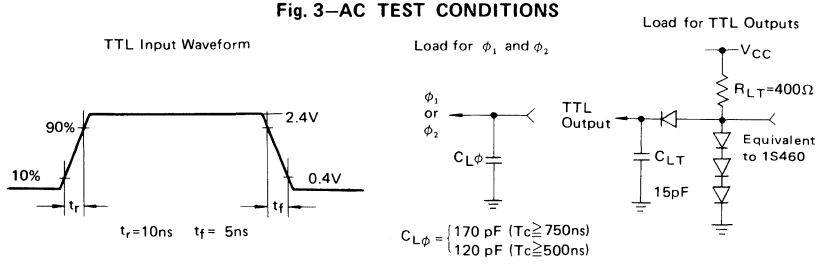
* Unused terminals are left open.

## AC CHARACTERISTICS

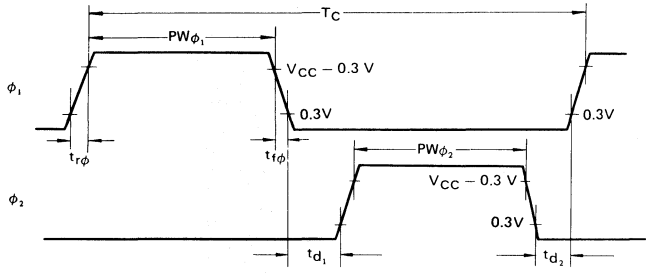
**(Full Guaranteed Operating Ranges unless otherwise noted.)**

| Parameter | | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Cycle Time | MB 8867 | $T_C$ | 0.5 | | 10 | μs | Fig. 3 |
| | MB 8867E | | 0.666 | | | | Fig. 4 |
| $\phi_1$ Pulse Width ($\phi_1$) | MB 8867 | $PW_{\phi_1}$ | $\frac{Tc}{2}-70$ | | | ns | Fig. 3 |
| | MB 8867E | | $\frac{Tc}{2}-100$ | | | | |
| $\phi_2$ Pulse Width ($\phi_2$) | MB 8867 | $PW_{\phi_2}$ | $\frac{Tc}{2}-50$ | | | ns | Fig. 4 |
| | MB 8867E | | $\frac{Tc}{2}-100$ | | | | |
| Rise Time ($\phi_1$, $\phi_2$) | | $t_{r\phi}$ | | 20 | 40 | ns | Fig. 3 |
| Fall Time ($\phi_1$, $\phi_2$) | | $t_{f\phi}$ | | 15 | 30 | ns | Fig. 4 |
| $\phi_1$ to $\phi_2$ Delay Time ($\phi_1$, $\phi_2$) | | $t_{d_1}$ | 5 | 20 | 30 | ns | Fig. 3 |
| $\phi_2$ to $\phi_1$ Delay Time ($\phi_1$, $\phi_2$) | | $t_{d_2}$ | 5 | 20 | 30 | ns | Fig. 4 |
| Pulse Width (4M) (M.RDY=INH=R.SEL=HIGH) | | $PW_4$ | $\frac{Tc}{8}-30$ | $\frac{Tc}{8}$ | | ns | Fig. 3 |
| | (2M) | $PW_2$ | $\frac{Tc}{4}-30$ | $\frac{Tc}{4}$ | | ns | Fig. 5 |
| | (M.CLK) | $PW_M$ | $\frac{Tc}{2}-30$ | $\frac{Tc}{2}$ | | ns | Fig. 3 |
| | (DATA STB) | $PW_D$ | $\frac{Tc}{4}-30$ | $\frac{Tc}{4}$ | | ns | Fig. 6 |
| 4M to M.GRANT Delay Time | | $t_{4G}$ | | | 50 | ns | Fig. 3 |
| 4M to M.CLK Delay Time | | $t_{4MC}$ | | 15 | 30 | ns | Fig. 5 |
| M.CLK to $\phi_1$ Delay Time | | $t_{M_1}$ | 5 | 20 | 60 | ns | Fig. 3 |
| M.CLK to $\phi_2$ Delay Time | | $t_{M_2}$ | 15 | 40 | 80 | ns | |
| M.CLK to DATA STB Delay Time | | $t_{MD}$ | $\frac{Tc}{4}-30$ | | $\frac{Tc}{4}+15$ | ns | Fig. 6 |
| $\overline{\text{M.CLK}}$ to R.GRANT Delay Time | | $t_{MG}$ | | | 50 | ns | |
| $\overline{\text{M.RDY}}$ Enable Time | | $t_{EM}$ | 50 | | | ns | Fig. 3 |
| $\overline{\text{M.RDY}}$ Disable Time | | $t_{DM}$ | 50 | | | ns | Fig. 5 |
| $\overline{\text{R.REQ}}$ Enable Time | | $t_{ER}$ | 50 | | | ns | Fig. 3 |
| $\overline{\text{R.REQ}}$ Disable Time | | $t_{DR}$ | 50 | | | ns | Fig. 6 |

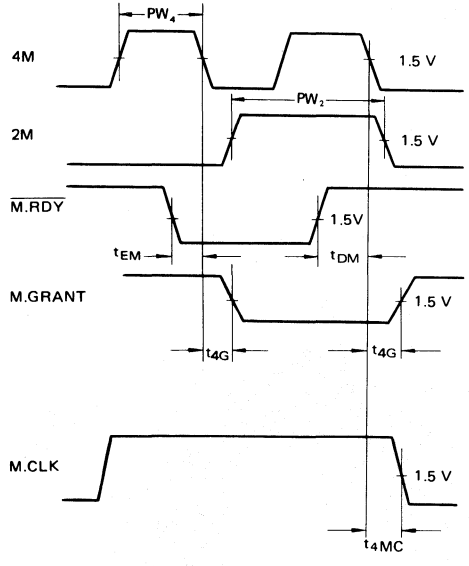
## Fig. 3—AC TEST CONDITIONS



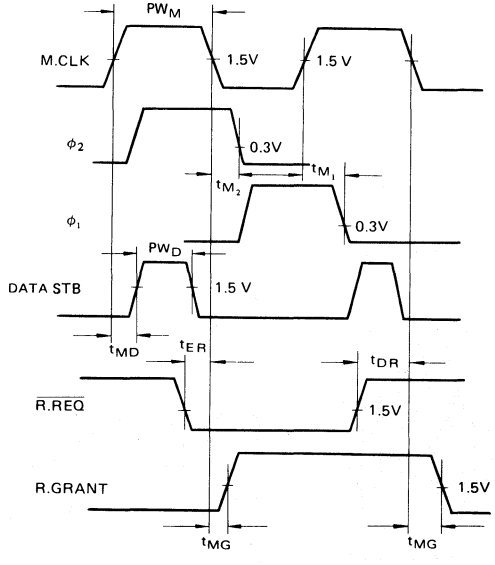

## Fig. 4—TIMING DIAGRAM (1)




## Fig. 5—TIMING DIAGRAM (2)




## Fig. 6—TIMING DIAGRAM (3)

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## TYPICAL CHARACTERISTICS CURVES

Fig. 7 – $I_{CC}$ SUPPLY CURRENT vs $V_{CC}$ SUPPLY VOLTAGE

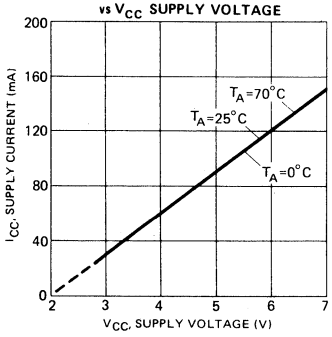



Fig. 8 – $I_{IN}$ INPUT CURRENT vs $V_{IN}$ INPUT VOLTAGE *

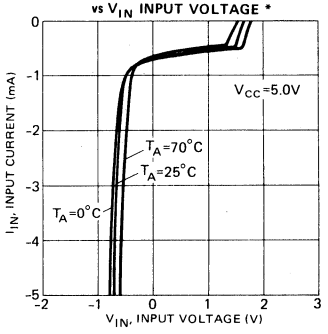
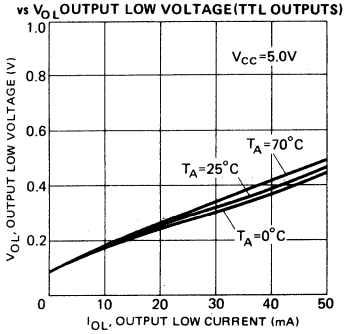



Fig. 9 – $I_{OL}$ OUTPUT LOW CURRENT vs $V_{OL}$ OUTPUT LOW VOLTAGE (TTL OUTPUTS)




* except inputs with pull-up resistor

Fig. 10 – $I_{OH}$ OUTPUT HIGH CURRENT vs $V_{OH}$ OUTPUT HIGH VOLTAGE (TTL OUTPUTS)

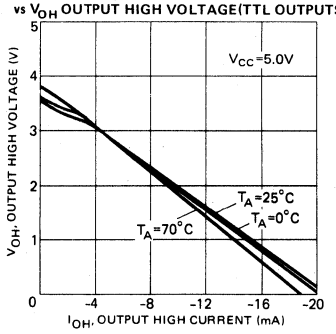



Fig. 11 – $I_{OL}$ OUTPUT LOW CURRENT vs $V_{OL}$ OUTPUT LOW VOLTAGE ($\phi$ OUTPUTS)

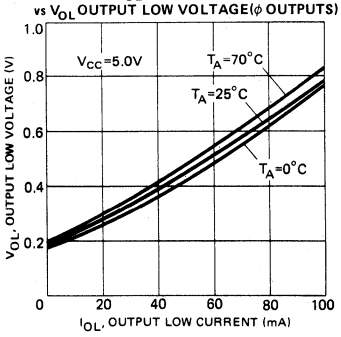



Fig. 12 – $\phi_1$, $\phi_2$ CLOCK PULSE WIDTH vs $T_C$ CYCLE TIME

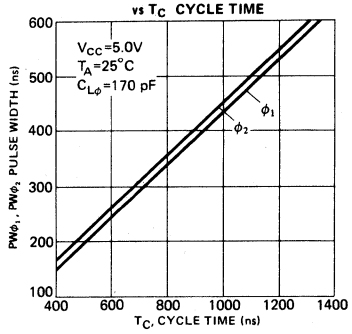



Fig. 13 – $I_{OH}$ OUTPUT HIGH CURRENT vs $V_{OH}$ OUTPUT HIGH VOLTAGE ($\phi$ OUTPUTS)

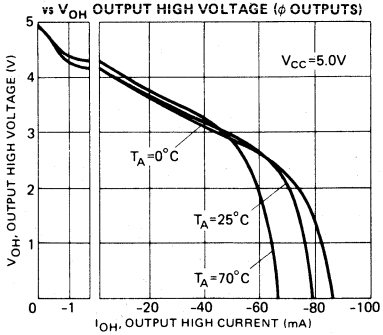
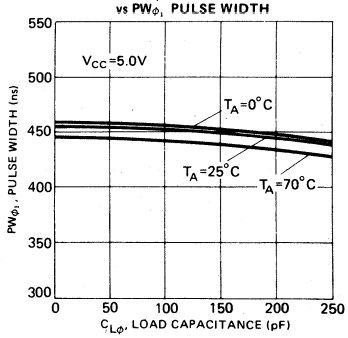



Fig. 14 – $C_{L\phi}$ LOAD CAPACITANCE vs $PW_{\phi_1}$ PULSE WIDTH



## APPLICATIONS INFORMATION

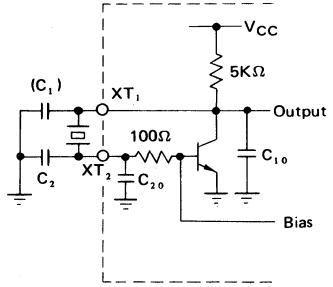
**1. Crystal Oscillator:**

The crystal oscillator circuitry is shown in Fig. 15. Oscillations between the serial ($f_0$) and parallel ($f_\infty$) resonant frequency of the crystal can be generated. Pico farad capacitors ($C_{10}$, $C_{20}$) are diffused on-chip. Therefore, oscillation can be generated by simply connecting an external capacitor ($C_2 \sim 50_pF$) from $XT_2$ to ground. Normally, a crystal with a resonant frequency of four or sixteen times the desired output clock driver frequency is used. The selection depends on whether the R. SEL pin is high (16X) or low (4X).

External crystal specifications:

| | |
|---|---|
| Oscillator Frequency | 22 MHz max. |
| Load Capacitance | 10 ~ 30 pF |
| Equivalent Resistance | 75 ohms max. |
| Resonant Power | 4 mW max. |

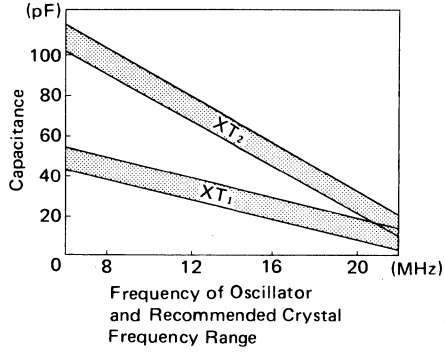
**Fig. 15—Oscillation Circuitry**




**Typical Frequency of Crystal Oscillator**

| Clock Frequency (MHz) | Cycle Time (ns) | Inherent Frequency of Crystal Oscillator (MHz) | |
|---|---|---|---|
| | | R.SEL=H | R.SEL=L |
| 1.00 | 1000 | 16.00 | – |
| 1.33 | 750 | 21.33 | – |
| 2.00 | 500 | – | 8.00 |

**Fig. 16—Standard Capacitance for Crystal Oscillator**

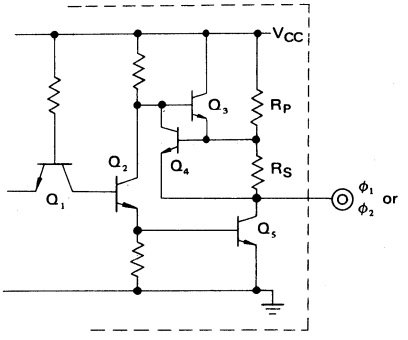



**2. $\phi_1$, $\phi_2$ Clock Driver Circuit**

The output clock driver circuit is shown in Fig. 17.

These circuits are designed to drive capacitive loads with a high amplitude pulse train. The pull-up resistor $R_p$ has a nominal value of 500 ohms, and is on-chip in order to swing $\phi_1$, $\phi_2$ up to $V_{CC}$. When $\phi_1$, $\phi_2$ are grounded, $R_s$ (10 ohms) and $Q_4$ protect the output driver $Q_3$.

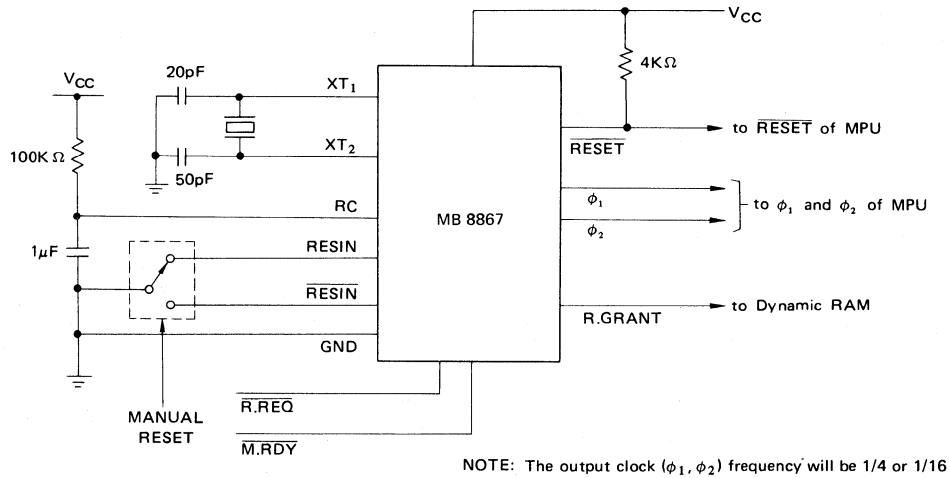
**Fig. 17—Clock Driver Circuitry**




**3. Input Controls**

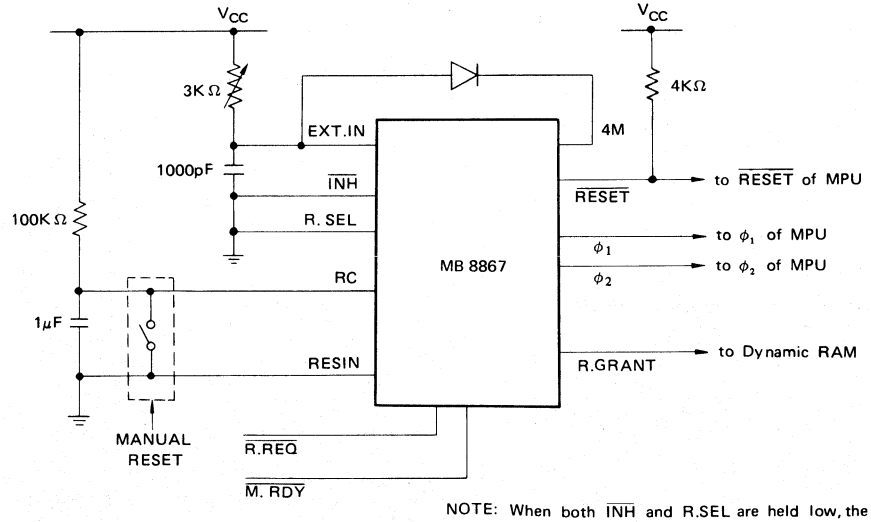
All input controls ($\overline{INH}$, R. SEL, $\overline{R.\ REQ}$, $\overline{M.\ RDY}$, RESIN, $\overline{RESIN}$) are TTL compatible. To simplify system packaging, all these pins have internal pull-up resistors so that they may be left open (unconnected) if desired.

Fig. 18–CLOCK GENERATION USING CRYSTAL




NOTE: The output clock ($\phi_1$, $\phi_2$) frequency will be 1/4 or 1/16 of the crystal frequency depending upon whether R.SEL is high or low.

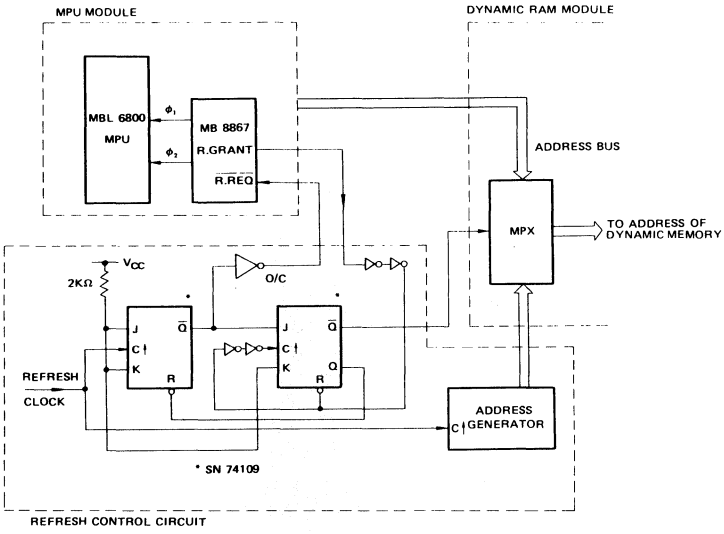
Fig. 19–CLOCK GENERATION USING EXTERNAL "RC" NETWORK



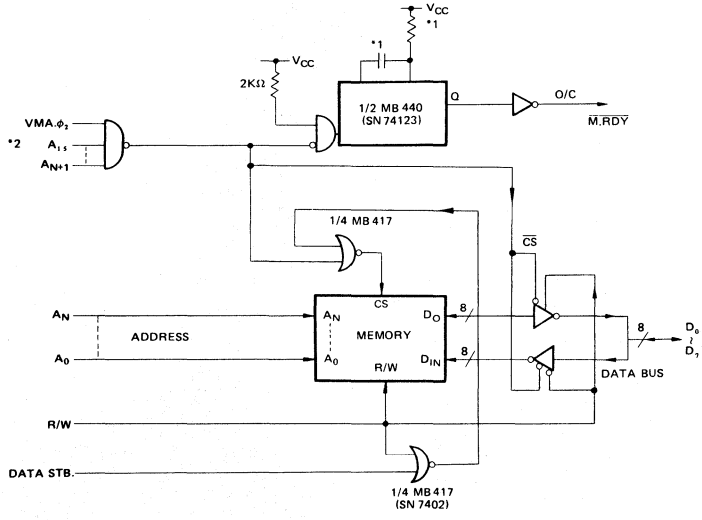

NOTE: When both $\overline{INH}$ and R.SEL are held low, the circuit between EXT. IN and 4M forms a five stage serial invertor. The osillation frequency of this ring oscillator is controlled by the external 3K ohm resistor.

## APPLICATIONS INFORMATION (cont'd)

### Fig. 20—REFRESH CONTROL APPLICATION




### Fig. 21—LOW SPEED MEMORY APPLICATION




NOTE: *1. Values depend upon memory speed. For 1 μs cycle time, use 100 pF and 25KΩ.
*2. Inverter for address selection may be used.

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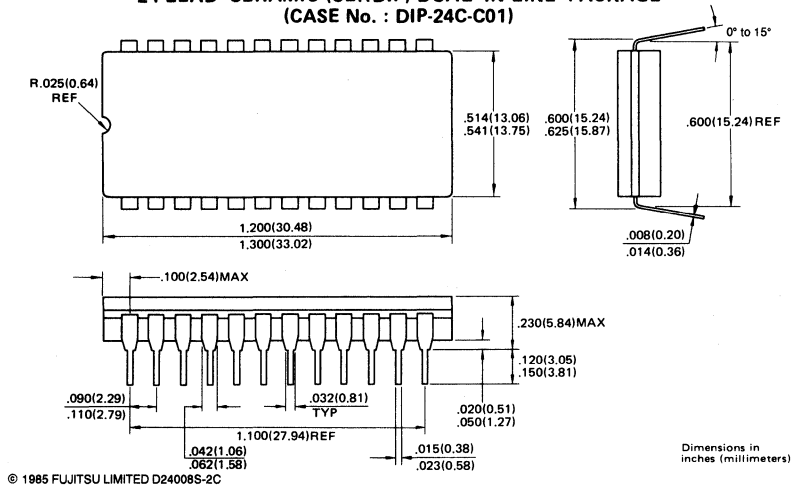
## PACKAGE DIMENSIONS

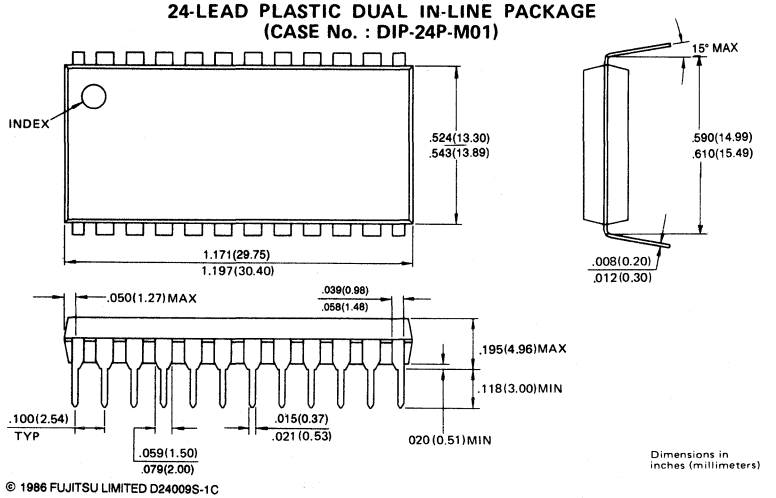
### 24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
### (CASE No. : DIP-24C-C01)




Dimensions in inches (millimeters)



### 24-LEAD PLASTIC DUAL IN-LINE PACKAGE
### (CASE No. : DIP-24P-M01)




Dimensions in inches (millimeters)

## SELECTOR GUIDE

### ANALOG-TO-DIGITAL CONVERTERS

| Device Number | Description | Resolution (bits) | Linearity (%) | Analog Input Voltage Range (V) | Conversion Speed | Supply Voltage (V) | Max. Supply Current (mA) | I/O Level | Package | Alternate Source |
|---|---|---|---|---|---|---|---|---|---|---|
| MB4052[1] | Bipolar 4-ch. 8-bit A/D Converter: Successive approximation technique, Serial output | 8 | ±0.19 | 3 Modes: 0 to 0.625, 0 to 2.5, 0 to 10 | 100 µs/ch Max | 3.5–6.0 or 8.0–18 | 30 at $V_{CC}$ = 6V | TTL/CMOS, Open Collector | DIP-16C-C02 DIP-16P-M02 | – |
| MB4053[2] | Bipolar 6-ch. A/D Converter Subsystem: Single slope method, Pulse width output, scale correction | – | ±0.2 | 0 to ($V_{CC}$ −2), 5.25 Max | 350 µ/ch Max | 4.75 to 15 | 10 | TTL | DIP-16C-C02 DIP-16P-M01 FPT-16P-M01 | µA 9708 |
| MB4056[3] | Bipolar 8-channel, successive approximation technique, Serial output | 6 | 0.19 | 0 to 1.25; 0 to 5 | 100 µ/channel max | 4.75 to 18 | 40 | TTL | DIP-20P-M01 | – |
| MB4063[2] | MB4053 with on-chip voltage divider | – | ±0.2 | 0 to ($V_{CC}$ −2), 5.25 Max | 350 µs/ch Max | – | – | TTL | DIP-16C-C02 DIP-16P-M01 FPT-16P-M01 | – |
| MB40547-7[3] -8[3] | Bipolar High Speed 1-ch. 8-bit A/D Converter: Fully-parallel comparison method | 8 8 | ±0.4 ±0.2 | $V_{CC}$ to ($V_{CC}$ −2) | 20 MSPS | −5.2 ±5% | −280 | 10K ECL | DIP-24C-A01 | – |
| MB40576[3] | Bipolar High Speed 1-ch. 6-bit A/D Converter: Fully-parallel comparison method | 6 | ±0.8 | $V_{CC}$ to ($V_{CC}$ −2) 1V Width | 20 MSPS | +5.0 ±5% | 80 | TTL | DIP-16P-M04 | – |

### DIGITAL-TO-ANALOG CONVERTERS

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| MB4072[2] | 8-bit High Speed Multiplying D/A Converter: High-Z open-collector outputs | 8 | ±0.2 | −10 to +18 ($V_S$ = ±15V) | 150 ns | ±4.5 to ±18 | 3.8 for $V_S^+$ = 15V −7.8 for $V_S^-$ = −15V | Any | DIP-16C-C02 DIP-16P-M02 FPT-16P-M02 | DAC-08 |
| MB40748-8[3] -9[3] | 10-bit High Speed D/A Converter | 10 | ±0.2 ±0.1 | 0 to −1 | 30 MSPS | −5.2 ±5% | −90 | 10K ECL | DIP-24C-A01 | – |
| MB40776[3] | 6-bit High Speed D/A Converter: Suitable for digital TV | 6 | ±0.8 | $V_{CC}$ to ($V_{CC}$ −1) | 20 MSPS | +5 ±5% | 65 | TTL | DIP-16P-M04 | – |
| MB40778[3] | 8-bit High Speed D/A Converter: Suitable for digital TV | 8 | ±0.2 | $V_{CC}$ to ($V_{CC}$ −1) | 30 MSPS | +5 ±5% | 75 | TTL | DIP-18P-M01 | – |
| MB40788[3] | 10-bit Ultra High Speed D/A Converter: Pin compatible with MB40748 | 10 | ±0.2 | 0 to −1 | 125 MSPS | −5.2 ±5% | −135 | 10K ECL | DIP-24C-A01 | – |

**Notes:**

1. $T_A$ = −30°C to +85°C
2. $T_A$ = −40°C to +85°C
3. $T_A$ = 0°C to +70°C

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