FUJITSU

MB88306 MB88307 MB88308 MB88309

October 1986

CMOS Output Expander

DESCRIPTION

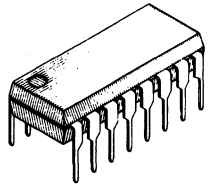
Each of the four expanders provides a serial I/O port and an 8-bit parallel output port. Data is serially loaded via the input port, converted to an 8-bit parallel format, and latched. The latched data is then transferred to the parallel output port for distribution. The 8-bit output port can directly drive a Light Emitting Diode (LED) display; the LED display can be expanded in byte-size increments to make any desired configuration. In terms of output drive and shift clock triggers, each expander is unique—see description that follows.

Expander	Output	Shift Clock Trigger
MB88306	CMOS 3-State	Rising Edge
MB88307	NMOS Open Drain	Rising Edge
MB88308	CMOS 3-State	Falling Edge
MB88309	NMOS Open Drain	Falling Edge

MB88306/7/8/9 are fabricated by a silicon-gate CMOS process and are packaged in a standard 16-pin plastic DIP or SOP. All four expanders operate with a single +5V power source and a 2 MHz shift clock over an ambient temperature range of −40°C to +85°C.

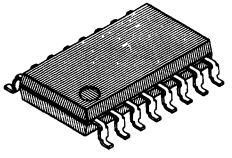
FEATURES

- 8-bit parallel output
- Serial input/output
- Expandable in 8-bit increments
- LED direct drive capability: 15 mA max at 1.2V
- Two output port types:
  —CMOS 3-state output (MB88306/8)
  —NMOS open-drain output (MB88307/9)
- Two shift clock polarities:
  —Rising-edge-triggering (MB88306/7)
  —Falling-edge-triggering (MB88308/9)
- Simple interface to Fujitsu 4-bit microcomputers
- TTL compatible outputs
- Single +5V power supply
- Silicon-gate CMOS process
- Two package options:
  —16-pin plastic DIP (Suffix -P)
  —16-pin plastic SOP (Suffix -PF)



8306-1

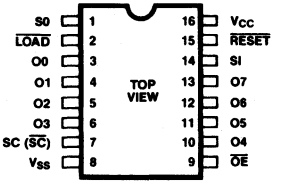
Plastic DIP (Suffix -P)
DIP-16P-M02



8306-2

Plastic SOP (Suffix -PF)
FPT-16P-M02

Pin Assignments



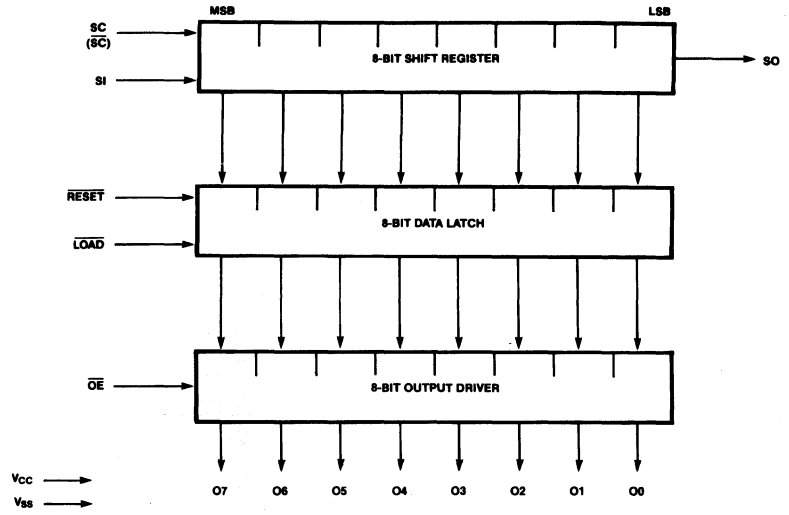
8306-3

Note:
SC is applicable to MB88306 and MB88307
$\overline{SC}$ is applicable to MB88308 and MB88309

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

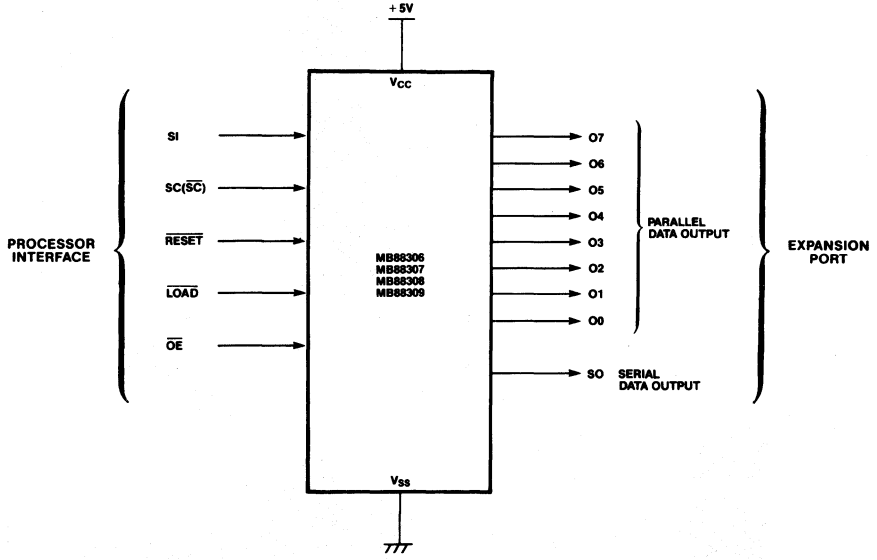
B38306

Figure 1. Block Diagram



8306-4

Figure 2. System Interface



8306-5

Note:
SC for MB88306/7; $\overline{SC}$ for MB88308/9

2

PIN DESCRIPTION

Figures 1 and 2 show the pin assignment and logic symbol of the MB88306/7/8/9. Table 1 shows the pin description. The MB88306/7/8/9 have two interfaces: one is the processor interface; SI, SC ($\overline{SC}$), $\overline{RESET}$, $\overline{LOAD}$, and $\overline{OE}$ inputs; the other is the expansion output port; O7-O0, and SO outputs.

Table 1: Pin Description

Symbol	Number	Type	Name & Function
• Power Supply			
V_{CC}	16	—	+5V dc power supply pin.
V_{SS}	8	—	Power supply ground pin.
• Processor Interface			
SI	14	I	Serial data input to the internal shift register: A data bit on the SI pin is shifted into the MSB of the shift register at the rising edge (MB88306/7) of the shift clock SC or the falling edge (MB88308/9) of the shift clock for $\overline{SC}$. The data bits are transferred from the processor or from the SO pin of the cascaded devices.
SC ($\overline{SC}$)	4	I	Shift clock input for the internal shift register: The rising edge of SC (MB88306/7) or falling edge of $\overline{SC}$ (MB88308/9) shifts a data bit on the SI pin into the MSB of the shift register, each bit of the shift register is shifted right, and the LSB of the shift register appears directly on the SO pin. A high level and low level and the falling edge (MB88306/7) or the rising edge (MB88308/9) keep contents of the shift register. *This is a hysteresis input.*
$\overline{RESET}$	15	I	Preset input for the internal data latch: A low level on the $\overline{RESET}$ pin initializes the data latch in high state, and also inhibits the $\overline{LOAD}$ input. *This is a hysteresis input.* The $\overline{RESET}$ input does not affect the shift register and the output drain.
$\overline{LOAD}$	2	I	Load enable input for the internal data latch: A low level on the $\overline{LOAD}$ pin transfers 8-bit parallel data of the shift register into the data latch. A high level inhibits data transmission from the shift register to the data latch, to hold contents of the data latch. This input is automatically inhibited when the $\overline{RESET}$ input is activated (low). *This is a hysteresis input.*
$\overline{OE}$	9	I	Output enable input of the output driver: A low level on the $\overline{OE}$ pin outputs 8-bit data of the data latch on the data output pins O7–O0. A high level places the O7–O0 pins in high impedance state. The $\overline{OE}$ pin does not control the SO output.
• Expansion Port			
O7–O0	13–10, 6–3	O	Parallel data output: This is an 8-bit 3-state data output port. This port outputs 8-bit data in the data latch when the $\overline{OE}$ pin is activated (low), and is placed in high impedance state when the $\overline{OE}$ pin is inactive (high). This port is CMOS 3-state output (MB88306/8) or NMOS open-drain output (MB88307/9). Both output drivers can directly drive LEDs. The MSB and LSB of the shift register are output onto the O7 and O0 pins, respectively. These pins are TTL compatible.
SO	1	O	Serial data output of the internal shift register: The LSB of the shift register appears directly onto the SO pin with some delay time because the SO output has no output latch. This pin is used to cascade devices to expand the data output port in 8-bit units. This pin is TTL compatible but is not 3-state output controlled by the $\overline{OE}$ pin.

FUNCTIONAL DESCRIPTION

BLOCK FUNCTIONS

The MB88306/7/8/9 consist of a shift register, a data latch, and an output driver. Figure 1.

Shift Register

This is an 8-bit serial-in/parallel-out static shift register, that converts serial data loaded by the processor into 8-bit parallel data. The rising edge (MB88306/7) or falling edge (MB88308/9) of the shift clock (SC or $\overline{SC}$) shifts a data bit on the SI pin into the MSB of the shift register. Each bit of the shift register is shifted right (MSB → LSB), and the LSB of the shift register is shifted out onto the SO pin. Eight parallel output lines of the shift register are internally connected to the data latch inputs. The Shift register has no clear input and, after power-up, the register contents are undefined. The $\overline{RESET}$ input does not affect the shift register.

Data Latch

This is an 8-bit D-type transparent latch that holds 8-bit parallel data transferred from the shift register. The latch has two control inputs, $\overline{LOAD}$ and $\overline{RESET}$: The $\overline{LOAD}$ pin is a data enable input and a low level on this pin transfers contents of the shift register into the data latch. The $\overline{RESET}$ pin is a preset input and a low level on this pin initializes the data latch in the high state. When the $\overline{RESET}$ input is active, the $\overline{LOAD}$ input is automatically inhibited.

Output Driver

This is an 8-bit 3-state output driver that is driven by 8 bits of data from the data latch. The MB88306/8 have a CMOS 3-state output driver and the MB88307/9 have an NMOS open-drain output driver. Both drivers are controlled by the $\overline{OE}$ input and can directly drive LEDs (V_{OL} = 1.2V max at I_{OL} = 20 mA). A low level on the $\overline{OE}$ pin enables 8-bit data in the data latch onto output pins O7–O0. A high level forces the output pins to a high impedance state. The $\overline{RESET}$ input does not affect the output driver.

SYSTEM INTERFACE

The processor and expansion-port interface for the four expanders is shown in Figure 2. As previously indicated, internal operations of the MB88306 and MB88307 are initiated on the rising edge of Shift Clock (SC) whereas, the same operations in the MB88308 and MB88309 occur on the falling edge of $\overline{SC}$. The Serial Output (SO) pin can be used to cascade two or more expanders; an example is shown later in this data sheet.

Table 2. Expander Functions

Mode	Control Inputs				Internal State		Data Outputs
	SC ($\overline{SC}$)	$\overline{LOAD}$	$\overline{RESET}$	$\overline{OE}$	Shift Register	Data Latch	O7–O0
Shift	↑ (↓)	H	X	X	X	X	X
Hold	H/L, ↓ (↑)	X	X	H	X	X	Z
				L			X
Load	X (X)	L	H	H	X	X	Z
				L	H/L	H/L	H/L
Reset	X (X)	X	L	H	X	H	Z
				L			X

Legend:
H = High level, L = Low level, Z = High impedance, X = Don't care, ↑ = Rising edge, ↓ = Falling edge

FUNCTIONAL DESCRIPTION (Continued)

OPERATING MODES

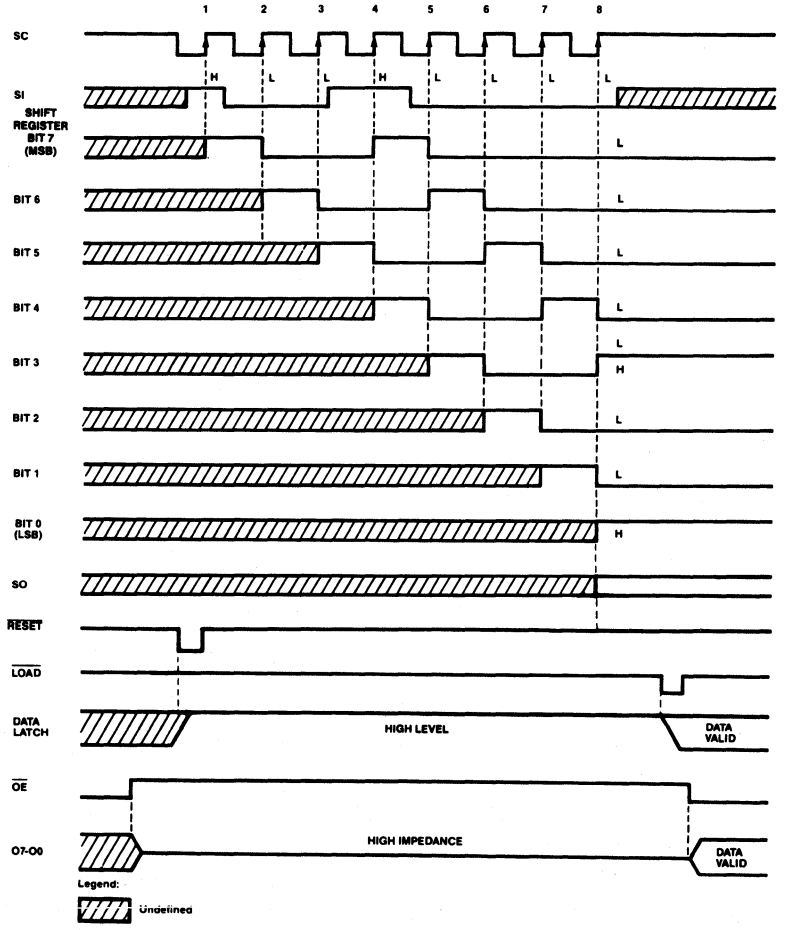
Initialization (Reset Mode)

After power on, contents of the shift register and data latch are undefined. The shift register can not be initialized by hardware because it has no preset input. The data latch can be preset to a high state by a low level on the $\overline{\text{RESET}}$ pin.

Data Input (Shift & Hold Modes)

Data serially loaded by the processor through the SI pin synchronously with the shift clock, SC (MB88306/7) or $\overline{\text{SC}}$ (MB88308/9). At the rising edge of SC or the falling edge of $\overline{\text{SC}}$, serial data on the SI pin is shifted into the MSB of the shift register. Each bit of the shift register is shifted right, and the LSB of the shift register underflows onto the SO pin. During high and low levels of SC ($\overline{\text{SC}}$), contents of the shift register are held.

Figure 3. Input/Output Timing Based on the Rising Edge of SC (I/O timing for $\overline{\text{SC}}$ is identical, except for pulse-width offset.)



FUNCTIONAL DESCRIPTION (Continued)

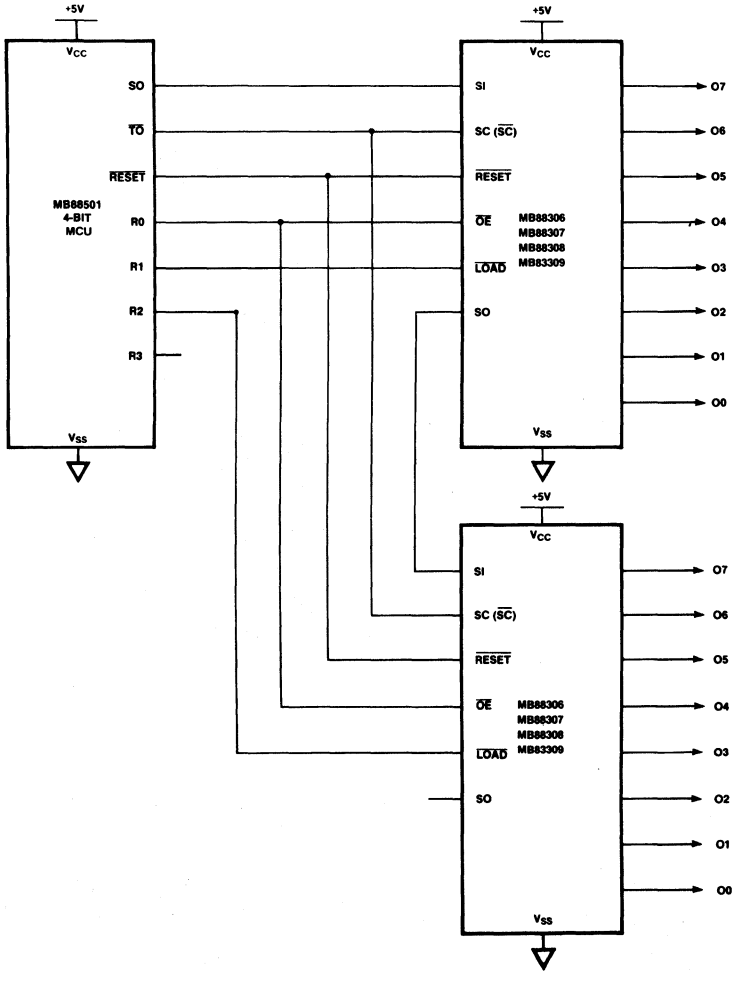
Data Output (Load Mode)

A low level on the $\overline{LOAD}$ pin transfers 8 bits of data from the shift register in parallel into the data latch. A low level on the $\overline{OE}$ pin enables the 8-bit data in the data latch onto the output port pins O7–O0. When the $\overline{LOAD}$ pin is high, the shift register and the data latch are isolated to hold contents of the data latch. (When the $\overline{RESET}$ pin is activated, the load input is automatically inhibited.) Also, when the $\overline{OE}$ pin is inactive, the O7–O0 pins are forced to a high impedance state. (The data output pins of the MB88307/9 float when 1s are output because they have NMOS open-drain drivers.)

APPLICATION

Figure 4 shows an example of an expanded output port configuration.

Figure 4. Expanded Output Port Configuration



2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Supply Voltage	V_{CC}	$V_{SS}-0.3$	$V_{SS}+7.0$	V	
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Output Voltage	V_{OUT}	$V_{SS}-0.3$	$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Output Low Current	I_{OL}		20	mA	
Total Output Low Current	ΣI_{OL}		60	mA	
Power Dissipation	P_D		200	mW	
Operating Ambient Temperature	T_A	−40	+85	°C	
Storage Temperature	T_{STG}	−55	+150	°C	

Note:

Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply Voltage	V_{CC}	4.5	5.5	V	Guaranteed range
	V_{SS}	0	0	V	
Input High Voltage	V_{IH}	$0.7V_{CC}$	$V_{CC}+0.3$	V	Non-hysteresis inputs: SI, $\overline{OE}$
	V_{IHS}	$0.8V_{CC}$	$V_{CC}+0.3$	V	Hysteresis inputs: $\overline{RESET}$, $\overline{LOAD}$, SC ($\overline{SC}$)
Input Low Voltage	V_{IL}	$V_{SS}-0.3$	$0.3V_{CC}$	V	Non-hysteresis inputs: SI, $\overline{OE}$
	V_{ILS}	$V_{SS}-0.3$	$0.2V_{CC}$	V	Hysteresis inputs: $\overline{RESET}$, $\overline{LOAD}$, SC ($\overline{SC}$)
Operating Ambient Temperature	T_A	−40	+85	°C	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Output High Voltage	V_{OH}	O7–O0[1], SO	V_{CC} = 4.5V, I_{OH} = −200 μA	2.4			V
			V_{CC} = 4.5V, I_{OH} = −10 μA	4.0			V
Output Low Voltage	V_{OL}	O7–O0, SO	V_{CC} = 4.5V, I_{OL} = 1.8 mA			0.4	V
			V_{CC} = 4.5V, I_{OL} = 5.0 mA			0.6	V
			V_{CC} = 4.5V, I_{OL} = 15 mA			1.2	V
Input Leakage Current	I_{IL}	SI, SC, ($\overline{SC}$) $\overline{RESET}$, $\overline{LOAD}$, $\overline{OE}$	V_{CC} = 5.5V, V_{IN} = 0.4V			−10	μA
High-Impedance Output Leakage Current	I_{OZ}	O7–O0[1]	V_{CC} = 5.5V, V_{IN} = 0V to 5.5V, Off State			±10	μA
Open-Drain Output Leakage Current	I_{leak}	O7–O0[2], SO	V_{CC} = 5.5V, V_{IN} = 5.5V, Off State			10	μA
Supply Current	I_{CC}	V_{CC}	V_{CC} = 5.0V (Typ), 5.5V (Max), f_C = 2 MHz, All Outputs Open and All Inputs Pulled Up/Down to V_{CC}/V_{SS}		'100	200	μA

Notes:

1. This parameter is specified for MB88307/MB88309 (CMOS 3-state output).
2. This parameter is specified for MB88306/MB88308 (NMOS open-drain output).

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Input Timing Requirements

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Shift Clock Frequency	f_C	SC ($\overline{SC}$)				2	MHz
Shift Clock Cycle Time	t_{CYC}	SC ($\overline{SC}$)	Fig. 5 (Fig. 6)	0.5			μs
Shift Clock Pulse Width	t_{WCH} / t_{WCL}	SC ($\overline{SC}$)	Fig. 5 (Fig. 6)	200			ns
Shift Clock Rise/Fall Times	t_{cr} / t_{cf}	SC ($\overline{SC}$)	Fig. 5 (Fig. 6)	10		100	ns
Input Data Setup Time	t_S	SI	Fig. 5 (Fig. 6)	100			ns
Input Data Hold Time	t_H	SI	Fig. 5 (Fig. 6)	50			ns
Reset Pulse Width	t_{W1}	$\overline{RESET}$	Fig. 7	100			ns
Load Pulse Width	t_{W2}	$\overline{LOAD}$	Fig. 7	200			ns

AC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted) (Continued)

Figure 5. Input Timing for MB88306 and MB88307

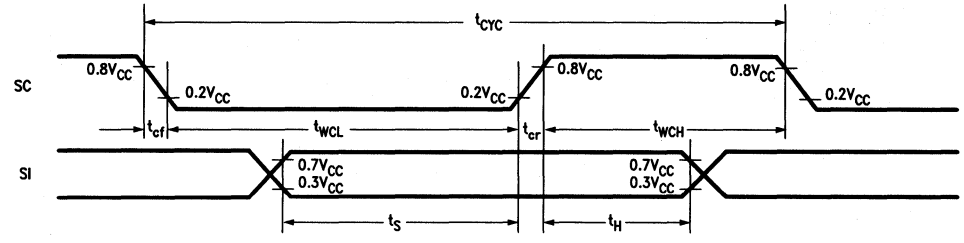


Figure 6. Input Timing for MB88308 and MB88309

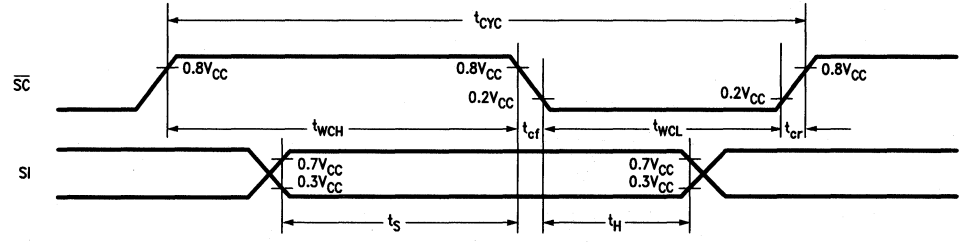
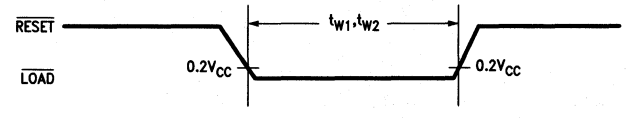


Figure 7. Input Timing for All Expanders



AC CHARACTERISTICS

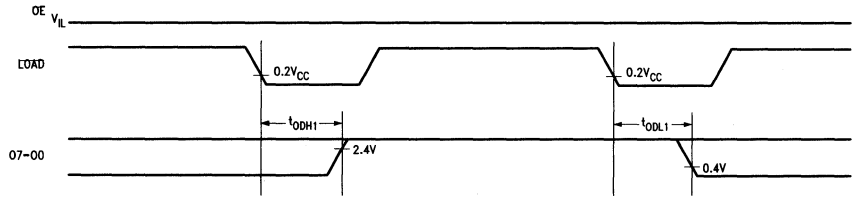
(Recommended operating conditions unless otherwise noted) (Continued)

Output Timing Responses

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Parallel Data Output Delay Time	t_{ODH1}	O7–O0	Output Load: 50 pF + 1.2 kΩ See Fig. 8			500	ns
	t_{ODL1}					200	ns
	t_{DOH2}					500	ns
	t_{DOL2}					200	ns
Serial Data Output Delay Time	t_{SDH}	SO				500	ns
	t_{SDL}					200	ns

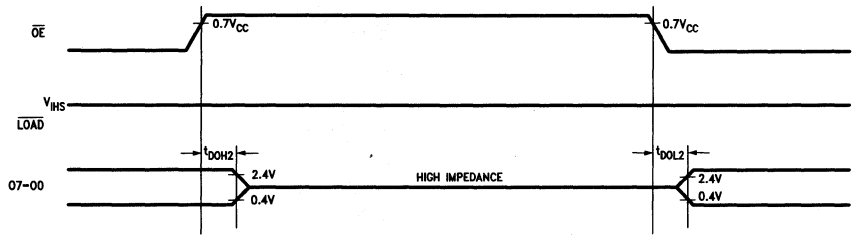
Figure 8. Output Timing for All Expanders

Parallel Data Output (1)—$\overline{LOAD}$ Controlled



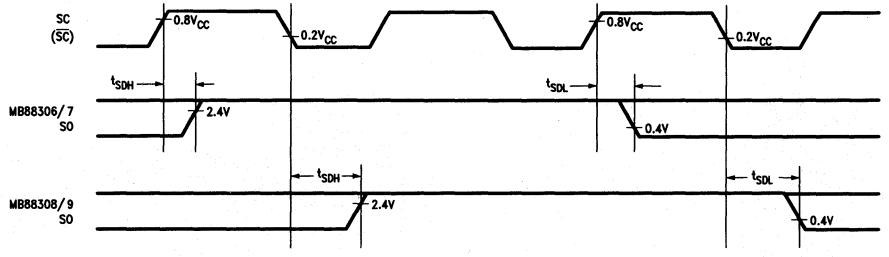
8306-11

Parallel Data Output (2)—$\overline{OE}$ Controlled



8306-13

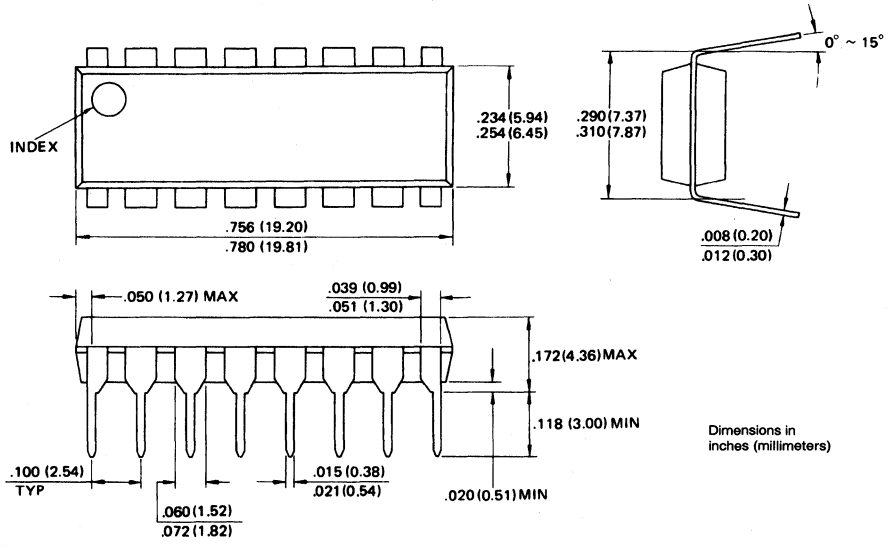
Serial Data Output



8306-12

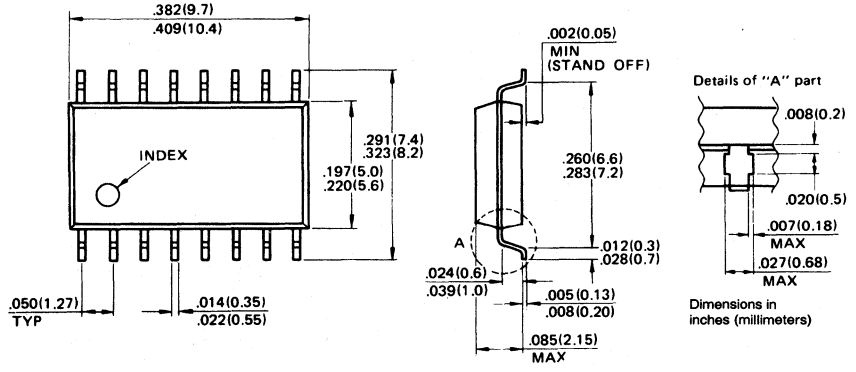
PACKAGE DIMENSIONS

16-LEAD PLASTIC
DUAL IN-LINE PACKAGE
(DIP-16P-M02)



8306-14

16-LEAD PLASTIC
FLAT PACKAGE
(FPT-16P-M02)



8306-15