Preliminary

Advanced Products FUJITSU

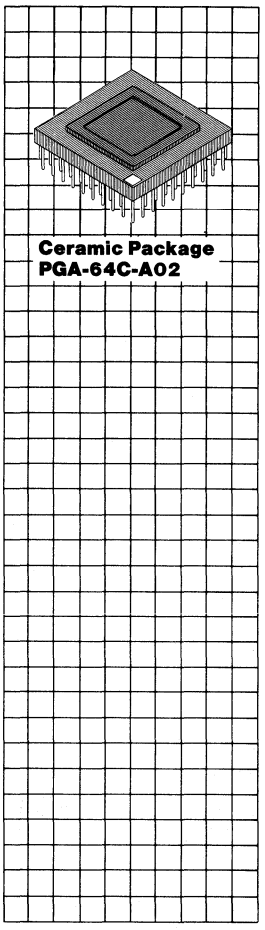
MB8795B
Ethernet Data Link Controller

Description

The Fujitsu MB8795B Ethernet Data Link Controller (EDLC) manufactured with Fujitsu's Advanced CMOS Technology, is designed for Ethernet* Local Area Network Systems and to be used with Fujitsu's MB502A Ethernet Encoder/Decoder (EED).

The MB8795B EDLC provides the user with a low power implementation of the Data Link Layer of the Ethernet Blue Book Specification. High throughput is possible via the separate data ports, while low cost implementations are also possible by tying the ports together.

The host system communicates with the MB8795B EDLC using the command and status registers accessed through the control port. Functions provided include complete transmit and receive control, and interrupt masking.



Ceramic Package
PGA-64C-A02

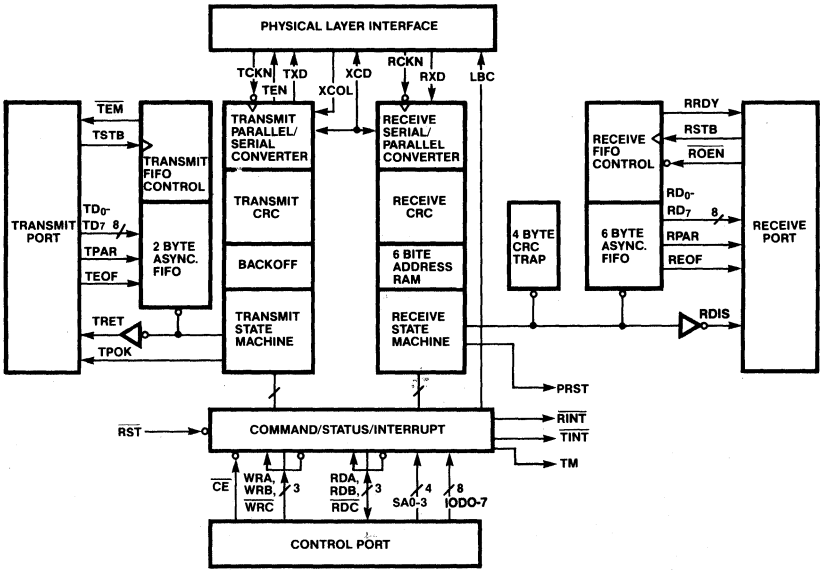
Features

- **Implementing Ethernet Blue Book Specification**
- **Function to generate and remove preamble and CRC**
- **Conversion between serial and parallel Data**
- **Four modes of address recognition**

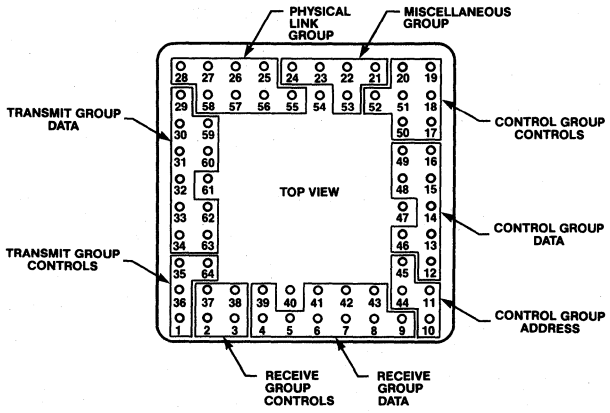
  Accept no packet, Physical Address/Multicast-group Address/Broadcast Address, Physical Address/Multicast Address, Accept all packets
- **Random exponential backoff to recover from collisions**
- **Three separate data ports providing flexible interface; Transmit, Receive, Control Ports**
- **Optional parity check on transmit byte stream**
- **Odd parity generated for receive byte stream**
- **Low power, advanced silicon gate CMOS technology**
- **Space saving 64-pin pin grid array package**

Note: *Ethernet is a trademark of Xerox Corp.

Block Diagram



Pin Assignment



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Pin Assignment
(Continued)

PIN No.	I/O	Pin Name	PIN No.	I/O	Pin Name	PIN No.	I/O	Pin Name	PIN No.	I/O	Pin Name
1	O	$\overline{TEM}$	17	I	$\overline{WRC}$	33	I	TD2	49	I/O	IOD6
2	O	RRDY	18	I	$\overline{WRB}$	34	I	TD0	50	I	RDA
3	I	$\overline{RSTB}$	19	I	$\overline{CE}$	35	O	TPOK	51	I	$\overline{RDB}$
4	O	RD0	20	I	$\overline{WRA}$	36	I	TSTB	52	I	$\overline{RDC}$
5	O	RD2	21	O	$\overline{TINT}$	37	O	RDIS	53	I	$\overline{RST}$
6	O	RD3	22	O	$\overline{RINT}$	38	I	$\overline{ROEN}$	54	V_{SS}	GND
7	O	RD5	23	O	PRST	39	O	RD1	55	I	RCKN
8	O	RD7	24	O	TM	40	V_{SS}	GND	56	I	XCOL
9	O	RPAR	25	I	RXD	41	O	RD4	57	I	XCD
10	I	SA1	26	I	TCKN	42	O	RD6	58	O	LBC
11	I	SA3	27	O	TXD	43	O	REOF	59	I	TEOF
12	I/O	IOD0	28	O	TEN	44	I	SA0	60	I	TD6
13	I/O	IOD2	29	I	TPAR	45	I	SA2	61	V_{DD}	V_{CC}
14	I/O	IOD3	30	I	TD7	46	I/O	IOD1	62	I	TD3
15	I/O	IOD5	31	I	TD5	47	V_{DD}	V_{CC}	63	I	TD1
16	I/O	IOD7	32	I	TD4	48	I/O	IOD4	64	O	TRET

Absolute Maximum Ratings

Rating	Symbol	Value Min.	Value Max.	Unit
Supply Voltage	V_{CC}	GND - 0.3*	7.0	V
Input and Output Voltage	V_I, V_{OUT}	GND - 0.3*	V_{CC} + 0.3*	V
Storage Temperature	T_{STG}	-55	150	°C
Operating Temperature	T_{OP}	0	70	°C

Note: *0.3 V is for stable state. For transit state, 0.5 V is allowed. (20 to 30 nsec.)

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Capacitance
(T_A = 25°C, V_{CC} = V_I = GND = 0V, f = 1 MHZ

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Unit
Input Capacitance	C_{IN}			8	pF
Output Capacitance	C_{OUT}			8	pF
Bus Capacitance	$C_{I/O}$			12	pF

Recommended Operating Conditions

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_{OP}	0		70	°C

DC Characteristics

Parameter	Symbol	Value Min.	Typ.	Max.	Unit
Power Supply Current (For Stable State; $V_{IH} = V_{CC}$, V_{IL} = GND)	I_{CC}	0		0.1	mA
Output High Voltage (I_{OH} = -0.4mA)	V_{OH}	4.0		V_{CC}	V
Output Low Voltage (I_{OL} = 2mA)	V_{OL}	GND		0.4	V
Input High Voltage	V_{IH}	2.2			V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage Current (V_I = 0V to V_{CC})	I_{LI}	-10		10	μA
Input Leakage Current for Bus Pins (V_I = 0V to V_{CC})	I_{LZ}	-40		40	μA

AC Characteristics

Control Register Read Timing

Parameter	Symbol	Value Min.	Typ.	Max.	Unit
Read Pulse Width	t_{RW}	35			ns
Read Address Pulse Width	t_{RAW}	35			ns
Read Access Time (C_L = 80 pF)	t_{RA}			110	ns
Read Address Access Time (C_L = 80 pF)	t_{RAA}			150	ns
Read Turn-off Delay Time (C_L = 80 pF)	t_{RZ}	10			ns
Read Address Turn-off Delay Time (C_L = 80 pF)	t_{RAZ}	20			ns
Address Register Read Access Time (C_L = 80 pF)	t_{ARRA}			300	ns
Address Register Read Address Turn-off Delay Time (C_L = 80 pF)	t_{ARRAZ}	20			ns
Address Register Read Address Setup Time	t_{ARRAS}	15			ns
Address Register Read Address Hold Time	t_{ARRAH}	90			ns

Control Register Write Timing

Parameter	Symbol	Value Min.	Typ.	Max.	Unit
Write Pulse Width	t_{WW}	35			ns
Write Address Set-up Time	t_{WAS}	30			ns
Write Data Set-up Time	t_{WDS}	15			ns
Write Address Hold Time	t_{WAH}	40			ns
Write Data Hold Time	t_{WDH}	80			ns
Test Pin Delay Time (C_L = 50 pF)	t_T			150	ns
Transmit Status Register Reset Delay Time (C_L = 50 pF)	t_{TS}			150	ns
Receive Status Register Reset Delay Time (C_L = 50 pF)	t_{RS}			150	ns
Reset Register Reset Delay Time (C_L = 50 pF)	t_R			220	ns

AC Characteristics
(Continued)

Transmit Timing

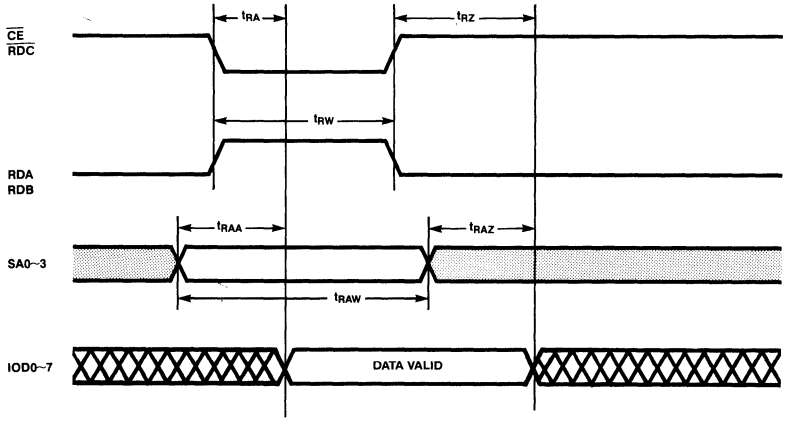
Parameter	Symbol	Value Min.	Typ.	Max.	Unit
TSTB Pulse Width	t_{TSTBW}	35			ns
TCKN Pulse Width	t_{TCKNW}	35			ns
TCKN Frequency	f_{TCKN}			10.2	MHz
Transmit Data Set-up Time	t_{TDS}	20			ns
Transmit Data Hold Time	t_{TDH}	25			ns
$\overline{TEM}$ Delay Time High (C_L = 50 pF)	t_{TEMH}			100	ns
$\overline{TEM}$ Delay Time Low (C_L = 50 pF)	t_{TEML}			150	ns
TEM Delay Time Low (Sync.) (C_L = 50 pF)	t_{TEMLS}			170	ns
TEN Delay Time (C_L = 50 pF)	t_{TEN}			55	ns
TXD Delay Time (C_L = 50 pF)	t_{TXD}			70	ns
TPOK Delay Time (C_L = 50 pF)	t_{TPOK}			150	ns
$\overline{TRET}$ Delay Time (C_L = 50 pF)	t_{TRET}			140	ns
TINT Delay Time (Transmit) (C_L = 50 pF)	t_{TINTT}			160	ns

Receive Timing

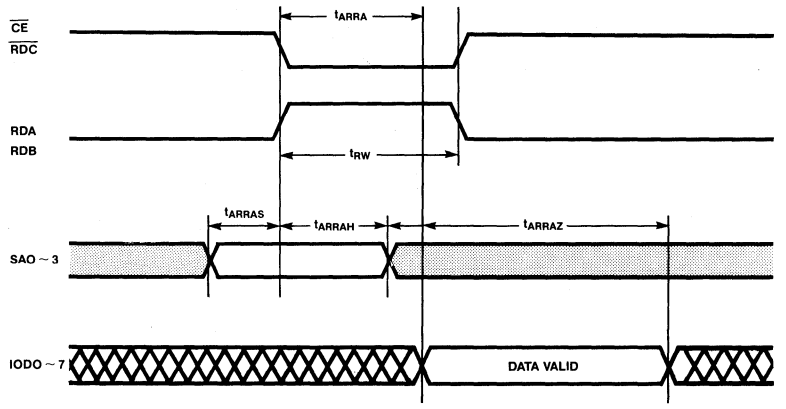
Parameter	Symbol	Value Min.	Typ.	Max.	Unit
RCKN Pulse Width	t_{RCKNW}	35			ns
RCKN Frequency	f_{RCKN}			10.2	MHz
$\overline{RSTB}$ Pulse Width	t_{RSTBW}	35			ns
ROEN Pulse Width	t_{ROENW}	35			ns
Receive Data Set-up Time	t_{RDS}	20			ns
Receive Data Hold Time	t_{RDH}	10			ns
RRDY Delay Time High (Sync.) (C_L = 50 pF)	t_{RRDYHS}			650	ns
Receive Data Delay Time (Sync.) (C_L = 50 pF)	t_{RDDS}			650	ns
RRDY Delay Time High (C_L = 50 pF)	t_{RRDYH}			100	ns
RRDY Delay Time Low (C_L = 50 pF)	t_{RRDYL}			65	ns
$\overline{Receive}$ Data Delay Time (C_L = 50 pF)	t_{RD}	10		100	ns
$\overline{ROEN}$ Access Time (C_L = 50 pF)	t_{ROENA}			80	ns
ROEN Turn-off Delay Time (C_L = 50 pF)	t_{ROENZ}	10			ns
RDIS Delay Time (C_L = 50 pF)	t_{RDIS}			120	ns
$\overline{PRST}$ Delay Time (C_L = 50 pF)	t_{PRST}			120	ns
$\overline{RINT}$ Delay Time (C_L = 50 pF)	t_{RINT}			160	ns
TINT Delay Time (Rcv) (C_L = 50 pF)	t_{TINTR}			190	ns

Timing Diagram

Control Register Read
Registers 0~7, F



Address Registers 8~D



WHEN RESET OR WHEN IN LOOPBACK AND ACCEPT NO PACKET MODE.

DON'T CARE

DATA UNDEFINED

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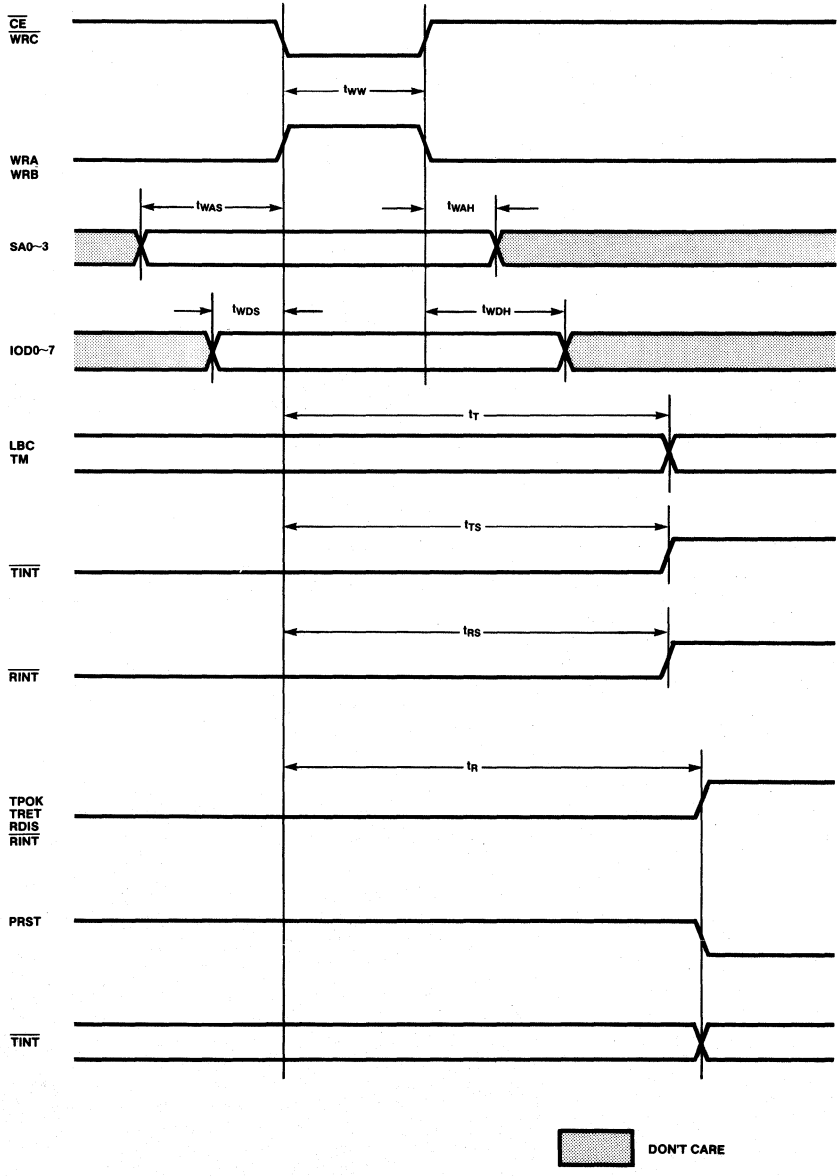
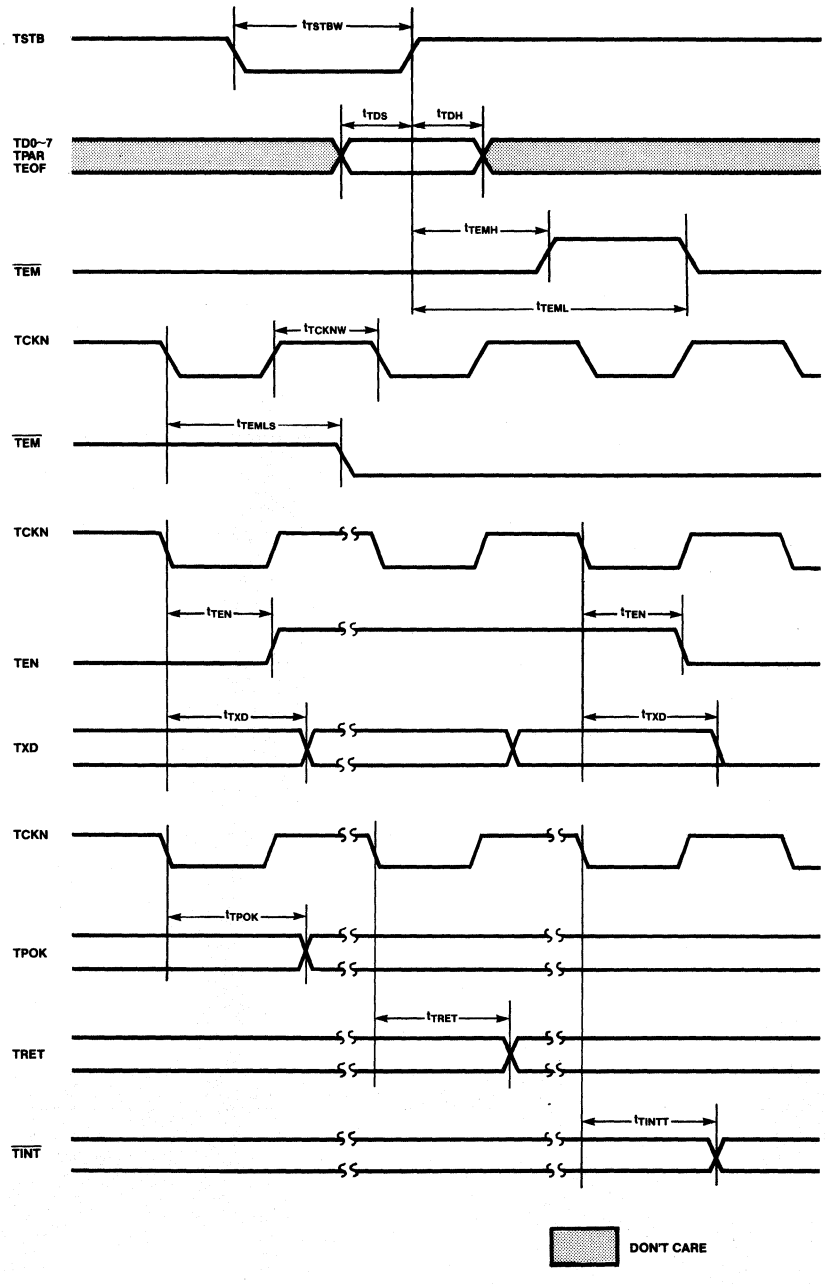
Timing Diagram
(Continued)

Control Register Write



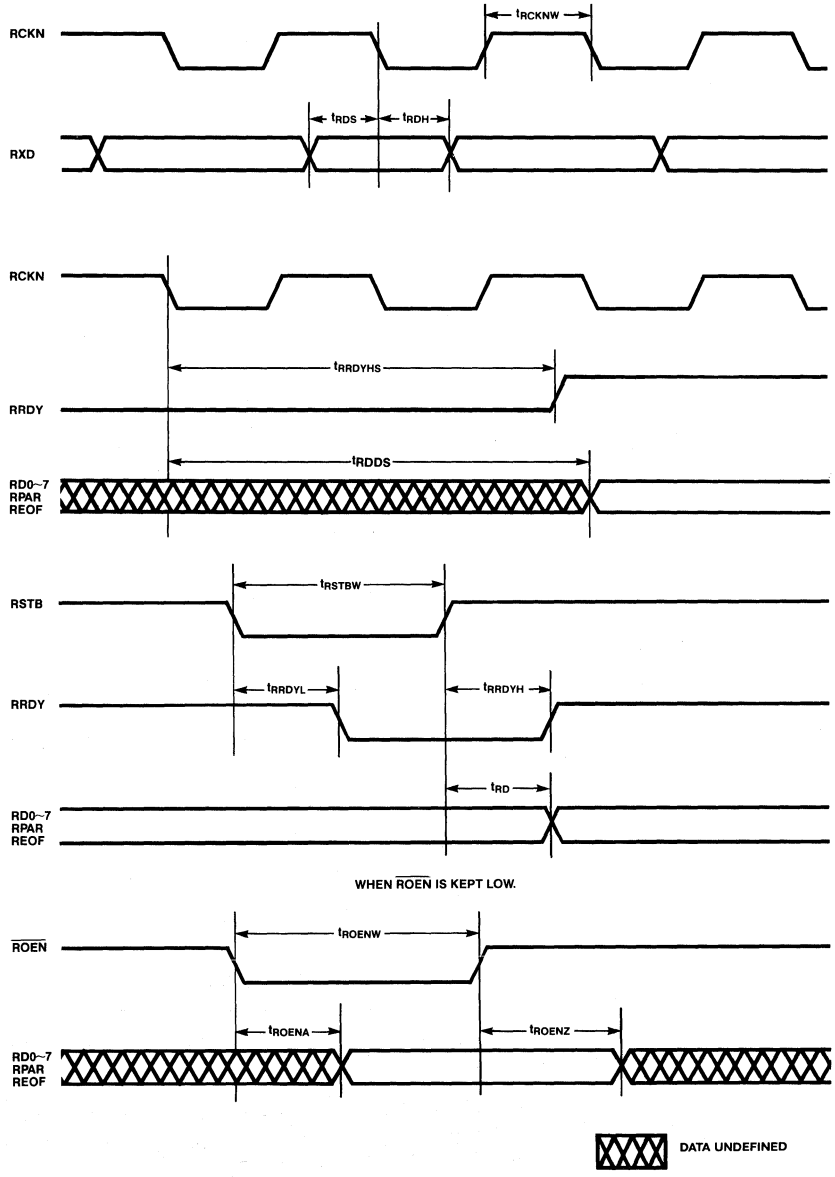
Timing Diagram
(Continued)

Transmit



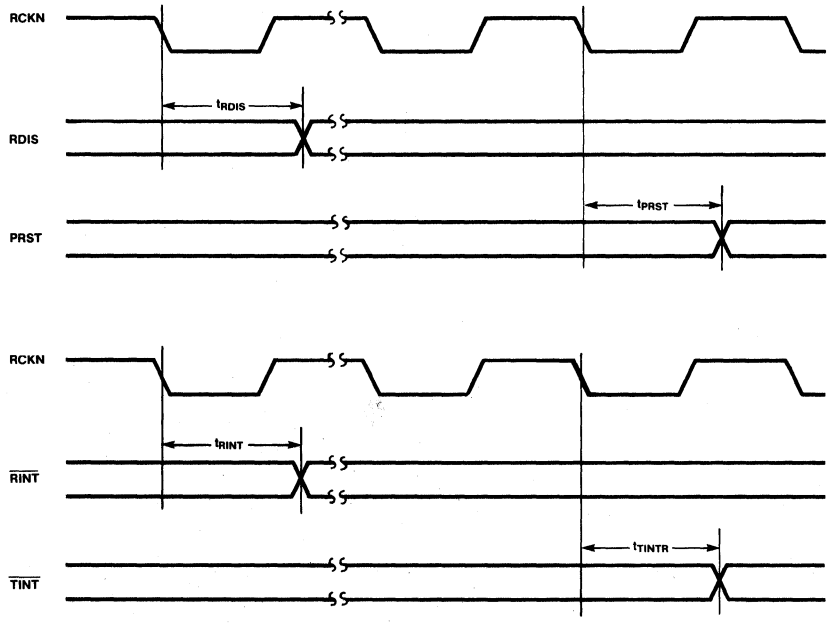
Timing Diagram
(Continued)

Receive



Timing Diagram
(Continued)

Receive (Continued)



Functional Description

The MB8795B EDLC is designed as two distinct sections, a transmitter and a receiver. Each section provides a small amount of asynchronous buffering, provisions for byte parity (which can be ignored), preamble generation/stripping, CRC generation/checking, and conversion between serial and parallel data. In addition, the transmitter provides contention resolution by means of binary exponential backoff. Finally, the receiver provides various modes of address recognition.

Transmitter

The block diagram on page 2 shows the various functions the transmitter performs.

Asynchronous FIFO

A two-byte FIFO provides a minimum amount of elastic buffering for the transmit byte data. Two signals are used for the byte controls. The first signal, $\overline{TEM}$, indicates that the input register is full. The second signal, $\overline{TSTB}$, is the input register data strobe. On the rising edge of this strobe input, the eight data bits, the parity bit and the 'end of frame' (TEOF) bit are latched into the input register. Strobes are ignored while the register is full.

The TRET signal indicates that a collision has occurred and that the packet in progress should be restarted. The buffer management would typically flush any buffers and reset its pointers to the beginning of the packet. Note that on the block diagram the asynchronous FIFO is cleared by this signal.

The TPOK signal indicates that successful transmission of the packet has been completed and the transmitter is ready for the next packet. This signal goes high when transmission of the packet is complete.

Note: The TPOK signal remains low long enough after the last byte is strobed into the FIFO, so the FIFO can be emptied and the CRC appended. Therefore the buffer management must remain prepared to reset its pointers in the case of a late collision.

Transmit Parallel/Serial Conversion

This section has a shift register for parallel to serial data conversion, a preamble generator, and a sychronization circuit for the collision and carrier detect signals. Also included is the optional 'ODD' parity check that is performed on the byte data supplied to the CRC generator. The parity check provides added security against internal chip failures due to undetected bad data transmissions.

Transmit CRC

The 32-bit CRC generator as defined in the Ethernet Specification.

Backoff

A pseudo-random number generator (17-bits), clocked at the bit rate so that distances between stations becomes part of the randomizing function, is sampled at the time of collision and counted down at the slot-time rate (512-bits) defined in the Ethernet specification, which provides a binary exponential backoff from collisions.

Transmitter State Machine

The state machine provides the major sequencing of events for the transmitter including idle, preamble, data, CRC, interframe gap, jam, and backoff. It also provides indicators for various error conditions.

Receiver

Refer to the block diagram for the relation of the sections. (See page 2).

Asynchronous FIFO

A six byte FIFO is provided so that when in diagnostic mode a minimum size packet (6 byte destination address and 4 byte CRC) can be received even in systems where the buffer management is half duplex. The data, parity and 'end of frame' bit are tri-stated with signal $\overline{ROEN}$, a low true enable. The 'receive byte ready' (RRDY) indicates a byte is available to the host system. RSTB is a low true clock whose falling edge causes RRDY to be false and whose rising edge causes the data in the register to be removed. See the timing charts for further clarification.

CRC Trap

All received bytes are delayed by four bytes so that the last bytes of the received packet (CRC) can be removed. After four bytes are received the trap will put one byte into the asynchronous FIFO for each subsequent byte received, thereby always maintaining four bytes in the trap. At the 'end of frame' the four bytes in the trap are the CRC and they are never put into the asynchronous FIFO.

Receive Serial/Parallel Conversion

This section has a shift register for data serial to parallel conversion, a circuit to recognize the end of preamble, and an odd parity check circuit.

Receive CRC

The 32-bit CRC checking register and comparison logic as described in the Ethernet specification.

6 Byte Address RAM

A 48-bit storage RAM used for comparing with the Destination Address Field of the incoming packets (the first 48 bits after the preamble).

Receiver State Machine

The state machine provides the major sequencing through the receiver states including idle, address recognition, data, and holding as a discarded packet completes. It also provides indicators of various error conditions.

Functional Description
(Continued)

Command/Status/Interrupt

This section has fifteen registers, a register address decoder, and gating for interrupt conditions. Each register is one byte length. The host system communicates with the MB8795B EDLC using these registers accessed through the control port.

Interrupt conditions are defined by setting the registers of Transmit Marks and Receive Masks.

Register Description

The Register in the MB8795B EDLC can be accessed via the control port with their address assigned by the signals SA0-3. (SA0 represents the LSB of the address.) The address signals SA0-3 are activated by both the chip enable signal CE and, write signals WRA, WRB, WRC, or, read signals RDA, RDB, RDC. A brief description of each register is given in the table below.

Register Description

			7	6	5	4	3	2	1	0
0	XMIT STATUS	RD	RDY For PKT	NET BUSY	XMIT RECVD	SHORT-ED	UNDER-FLOW	COLL	16 COLL	PAR ERR
		WR	—	—	—	—	CLR UNDER-FLOW	CLR COLL	CLR 16 COLL	CLR PAR ERR
1	XMIT MASKS	RD/WR	MASK STATUS 7	—	MASK STATUS 5	—	MASK STATUS 3	MASK STATUS 2	MASK STATUS 1	MASK STATUS 0
2	REC STATUS	RD	PKT OK	—	—	RESET PKT	SHORT PKT	ALIGN ERR	CRC ERR	OVER-FLOW ERR
		WR	CLR PKT	—	—	—	CLR ERR	CLR ERR	CLR ERR	CLR ERR
3	REC MASKS	RD/WR	MASK STATUS 7	—	—	MASK STATUS 4	MASK STATUS 3	MASK STATUS 2	MASK STATUS 1	MASK STATUS 0
4	TMODE + COLL ATTEMPT	RD/WR	3	2	1	0	IGNORE PARITY	TM	LBC	DIS-ABLE CONTNT
			Collision Attempts, Read Only							
5	RMODE	RD/WR	TST CRC	—	—	ADD SIZE	ENA SHORT PKT	ENA RST	ADD ENA1	ADD ENA0
6	RESET	Write Only	RESET	—	—	—	—	—	—	—
7	TDR1	Read Only	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0

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Register Description
(Continued)

48-Bit Ethernet Address

			7	6	5	4	3	2	1	0
8	NODE IDO	RD/WR	8th BIT A.P.	7th BIT A.P.	6th BIT A.P.	5th BIT A.P.	4th BIT A.P.	3rd BIT A.P.	2nd BIT A.P.	1st BIT A.P.*
			First Byte After Preamble							
9	NODE ID1	RD/WR	16th BIT A.P.	15th BIT A.P.	14th BIT A.P.	13th BIT A.P.	12th BIT A.P.	11th BIT A.P.	10th BIT A.P.	9th BIT A.P.
			Second Byte After Preamble							
A	NODE ID2	RD/WR	24th BIT A.P.	23rd BIT A.P.	22nd BIT A.P.	21st BIT A.P.	20th BIT A.P.	19th BIT A.P.	18th BIT A.P.	17th BIT A.P.
			Third Byte After Preamble							
B	NODE ID3	RD/WR	32nd BIT A.P.	31st BIT A.P.	30th BIT A.P.	29th BIT A.P.	28th BIT A.P.	27th BIT A.P.	26th BIT A.P.	25th BIT A.P.
			Fourth Byte After Preamble							
C	NODE ID4	RD/WR	40th BIT A.P.	39th BIT A.P.	38th BIT A.P.	37th BIT A.P.	36th BIT A.P.	35th BIT A.P.	34th BIT A.P.	33rd BIT A.P.
			Fifth Byte After Preamble							
D	NODE ID5	RD/WR	48th BIT A.P.	47th BIT A.P.	46th BIT A.P.	45th BIT A.P.	44th BIT A.P.	43rd BIT A.P.	42nd BIT A.P.	41st BIT A.P.
			Sixth Byte After Preamble							
E	(RESERVED)		—	—	—	—	—	—	—	—
F	TDR2	Read Only	—	—	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

*Multicast bit

Register Description
(Continued)

Transmit Status—Address 00H

This register indicates the status of the transmitter.

Bit 7

Read—Ready for Packet—A copy of the Transmit Packet Successful (TPOK) signal pin. For use in systems where the processor handles the transmit buffer management.

Write—no effect.

Bit 6

Read—Net Busy—A copy of the Receive Carrier Detect (XCD) input.

Write—no effect.

Bit 5

Read—Transmitted Packet was Received—Indicates that shortly after transmission was completed a good packet was received by the receiver. This is used to indicate self-reception of the packet, which allows the software to take advantage of the hardware address matching even in systems which are designed for half duplex operation. This bit is cleared as each transmission begins.

Write—no effect.

Bit 4

Read—Shorted—Set if the Receive Carrier Detect (XCD) stops during packet transmission. Either a collision or shorted coax can cause the bit to be set. This bit is cleared as each transmission begins.
—Write—no effect.

Bit 3

Read—Underflow—Set when data to be transmitted is not available to the parallel to serial converter before the converter is empty. Transmission is aborted immediately while bytes will be accepted from the FIFO until an EOF is encountered.

Write—0, no effect; 1, clear the error condition.

Bit 2

Read—Collision—Set when a collision terminates transmission of a packet.

Write—0, no effect; 1, clear the error condition.

Bit 1

Read—16 Collisions—Set when the 16th collision for a single packet aborts transmission. Bytes are strobed through FIFO normally to discard the packet.

Write—0, no effect; 1, clear the error condition.

Bit 0

Read—Parity Error—Set when the parallel to serial converter detects a parity error in the data. If parity check is enabled transmission is aborted while the bytes continue to be strobed from the FIFO, until EOF.

Write—0, no effect; 1, clear the error condition.

Transmit Masks—Address 01H

The interrupt conditions which define the signal at $\overline{\text{TINT}}$ are defined by setting the bits of this register.

Bit 7—Rd/Wr—Gates 'Ready For Packet'
Bit 6—no bit, read as 0
Bit 5—Rd/Wr—Gates 'Transmit Received'
Bit 4—no bit, read as 0.
Bit 3—Rd/Wr—Gates 'Underflow'
Bit 2—Rd/Wr—Gates 'Collision'
Bit 1—Rd/Wr—Gates '16 Collisions'
Bit 0—Rd/Wr—Gates 'Parity Error'

Receive Status—Address 02H

This register indicates the status of the receiver.

Bit 7

Read—Packet OK—Set when CRC of a legal length packet received is correct.

Write—0, no effect; 1, clear the error condition.

Bit 6

not used

Bit 5

not used

Bit 4

Read—Reset Packet—Set when a packet is received successfully and the field type is 0900H. The bit is cleared at the beginning of the next packet reception. The bit is set only if the Node ID matches, not multicast or broadcast. Reset packets are recognized in any Address Match mode from NONE to PROMISCUOUS.

Write—no effect

Bit 3

Read—Short Packet—Set if a packet does not meet the minimum length requirements of the Ethernet specification.

Write—0, no effect; 1, clear condition.

Bit 2

Read—Alignment Error—Set if a packet has bad CRC at the last octet boundary and the number of bits are not divisible by eight.

Write—0, no effect; 1, clear condition.

Bit 1

Read—CRC Error—Set if the CRC does not verify at the end of the packet.

Write—0, no effect; 1, clear the error condition.

Bit 0

Read—Overflow—Set if the internal asynchronous FIFO is full when a byte is available from the serial to parallel converter.

Write—0, no effect; 1, clear error condition.

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Register Description
(Continued)

Receive Masks—Address 03H

The interrupt conditions which define the signal at RINT are defined by setting the bits of this register.

Bit 7—Rd/Wr—Gates 'Packet OK'
Bit 6—no bit, read as 0.
Bit 5—no bit, read as 0.
Bit 4—Rd/Wr—Gates 'Reset Packet'
Bit 3—Rd/Wr—Gates 'Short Packet'
Bit 2—Rd/Wr—Gates 'Alignment Error'
Bit 1—Rd/Wr—Gates 'CRC Error'
Bit 0—Rd/Wr—Gates 'Overflow'

Transmit Mode—Address 04H

Bits 7-4

Read Only—Collision Attempts—Indicates the number of collisions occured before the last packet was sent (or aborted). This is a testing aid as the number is cleared at the beginning of a subsequent transmission.

Bit 3

Rd/Wr—Ignore Parity—if set this bit prevents the setting of the Parity Error condition.

Bit 2

Rd/Wr—TM—A bit whose complement is available as signal pin TM. Intended to control the power to the transceiver or any other function external to the chip.

Bit 1

Rd/Wr—LBC—A bit whose complement is available as signal pin LBC. Intended to control the loopback function of the Encoder/Decoder or any other function external to the chip.

Bit 0

Rd/Wr—Disable Contention—When this bit is set the transmitter disregards Receive Carrier Detect. This special function would only be used if the MB8795B EDLC were used in a two wire point to point link, in true full duplex operation. In this case the Collision Detect signal (a low level will inhibit the start of transmission) acts as carrier sense for the transmitter while collisions during transmissions are ignored.

Receive Mode—Address 05H

Bit 7

Rd/Wr—Test Mode—For chip testing this bit:

1) Inhibits the receiver from accumulating CRC. The last four bytes of a packet are shifted into the CRC register and checked without being modified.

2) Changes the backoff algorithm so that the pseudo-random number generator is disabled and the number to backoff becomes $2^{n-1}+1$, where n is the number of collisions. Also, the slot time is reduced to one (1) byte.

Bit 6

not used.

Bit 5

not used.

Bit 4

Rd/Wr—Address Size—When set this bit reduces the Node ID address match to 5 bytes instead of the normal 6. This is used where the node is performing some multiplex function on the least significant byte of the destination address.

Bit 3

Rd/Wr—Short Packet Enable—For testing, when this bit is set the receiver will successfully receive any packet of ten (10) bytes or more. This function is used in half duplex systems for the loopback check and can be used by all testing programs to reduce testing time.

Bit 2

Rd/Wr—Reset Enable—When this bit is zero, the checking done for the special type field is disabled.

Bit 1-0

Rd/Wr—Address Match Mode—

- Mode 0—accept no packets
- Mode 1—accept Node ID packets, multicasts which match the first three bytes of the Node ID packets, and broadcast packets.
- Mode 2—accept Node ID packets, and all multicasts including broadcast of course
- Mode 3—promiscuous, accept all packets.

Reset—Address 06H

Bit 7

Write Only—Reset—This latch is writeable and will hold the device in the reset state while set. It is set by the external reset pin RST being low. After power up the software should first initialize all the modes and masks, and then clear the reset.

Bit 6-0

not used

TDR LSB—Address 07H

Bits 7-0

Read Only—contains the least significant 8 bits of the TDR register which counts how many bits were successfully transmitted. Counting stops on collision or drop of carrier. Count is reset with each transmission.

Node ID—Addresses 10-15H

These 6 bytes are Rd/Wr and represent the address against which th frame addresses are matched during Address Match Modes 1 and 2. Bit 0 of address 10H is equivalent to the multicast bit.

TDR MSB—Address 17H

Bits 7-6

not used

Bits 5-0

Read Only—Contains the most significant six bits of the TDR register which was described above.

Register Description (Continued)

Interface Signal Description

Power Group

V_{CC}—+5V power supply (two pins)

GND—ground (two pins)

Control Group

$\overline{CE}$ (Chip enable, low active input)

This active low signal gates all control port reads and writes.

RDA,RDB,$\overline{RDC}$ (Control read, inputs)

These two active high and one active low signals are ANDed with $\overline{CE}$ to form read signals inside the MB8795B EDLC.

WRA,WRB,$\overline{WRC}$ (Control write, inputs)

These two active high and one active low signals are ANDed with $\overline{CE}$ to form write strobes inside the MB8795B EDLC. One of the signals is intended to be a clock so that address, data, and other controls will be stable when the internal write is active.

SA0-3 (Control port address, input)

These four signals address the 16 possible registers of the MB8795B EDLC. SA0 is the least significant bit of the address.

IOD0-7 (Control port data, 3-state outputs and inputs)

These eight signals are the bi-directional data used to read and write the 16 possible internal registers of the MB8795B EDLC.

Transmit Group

TD0-7 (Transmit data bytes, inputs)

Eight bits of data to be transmitted.

TPAR (Transmit data parity, input)

Optional parity accompanying the transmit byte data.

TEOF (Transmit data end of frame, input)

Required data bit which signals the last byte of the frame. After the byte having this bit is sent, CRC transmission will start.

$\overline{TEM}$ (Transmit byte register not empty, output)

Indicates that the asynchronous FIFO has no room for a byte.

TSTB (Transmit byte register strobe, positive edge-trigger input)

Strobes the transmit data into the asynchronous FIFO.

TRET (Transmit packet - retransmit packet, output)

Indicates that a collision or underflow has occurred. Buffer management logic should discard any remaining bytes of the current packet and then restart transmission of the packet.

TPOK (Transmit packet successful, output)

Indicates to the buffer management that it will not be required to retransmit the current packet again and thus can proceed to the next packet.

Receive Group

RD0-7 (Receive data bytes, 3-state outputs)

Eight bits of data being received.

RPAR (Receive data parity, 3-state output)

Odd parity computed on the incoming data stream.

REOF (Receive data end of frame, 3-state output)

A tenth data bit which accompanies the last byte of the frame, which is only present if reception was successful. Successful reception means that a packet had good CRC, appropriate length and an address match in the current mode.

$\overline{ROEN}$ (Receive byte output enable, low active input)

3-state enable for the ten data bits above. This allows multiplexing the receive data port with the transmit and control ports in low cost systems.

RRDY (Receive byte ready, output)

Indicates that a byte is available at the output of the async FIFO.

RSTB (Receive byte strobe, positive edge trigger input)

Strobes the receive data out of the async FIFO to the host system.

RDIS (Receive packet discard, output)

Indicates that the bytes received so far should be discarded because of bad address, bad length or bad CRC. This signal and the REOF output are mutually exclusive.

Physical Link Group

RCKN (Receive data clock, negative edge trigger input)

This signal is generated by the Ethernet Encoder/Decoder (EED) MB502A. It is a strobe frequency source for the receive bit clock and is used to strobe RXD.

RXD (Receive serial data, input)

Decoded data from the MB502A EED.

TCKN (Transmit data clock, negative edge trigger input)

Generated by the MB502A EED as a strobe frequency source for the transmit bit clock.

TEN (Transmit encode enable, output)

High true enable for Manchester encoding. This signal is strobed and stable at the same time as TXD.

TXD (Transmit serial data, output)

Serial data to be encoded onto the Ethernet Coax. Gated by TEN

XCD (Receive carrier detect, input)

Carrier detect signal of the decoder. Used by the receiver as data gate and by the transmitter as contention information.

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Register Description
(Continued)

XCOL (Collision presence, input)

A TTL copy of the Collision presence pair of the transceiver cable. The idle state is indicated by a logic "1" and the collision is indicated by a 10 MHz square wave.

LBC (Loopback Control, output)

A copy of a software setable latch used to command the MB502A EED to operate in Loopback mode.

Misc. Group

PRST (Packet reset, output)

Indicates that a complete and legal packet of type 0900H was received. This is intended to be used as a remote reset function.

$\overline{\text{RINT}}$ (Receive interrupt, output)

A logic "0" indicates the receiver interrupt condition coincides with its corresponding mask bit.

$\overline{\text{TINT}}$ (Transmitter interrupt, output)

Same as $\overline{\text{RINT}}$ for transmitter interrupt.

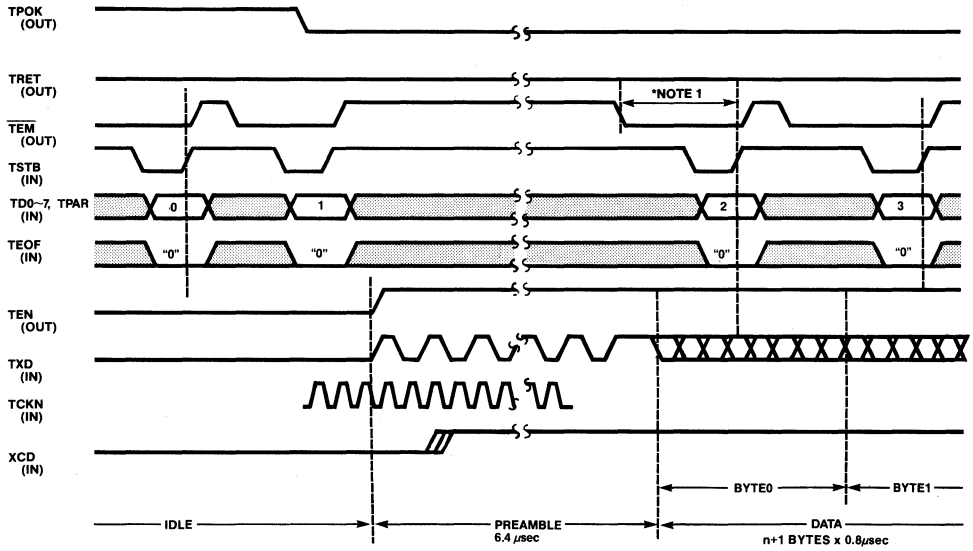
$\overline{\text{RST}}$ (Reset, low active input)

TM (Test mode, output)

A copy of a software loadable latch. Intended to control a circuit to turn the Transceiver power on and off.

Timing Diagram

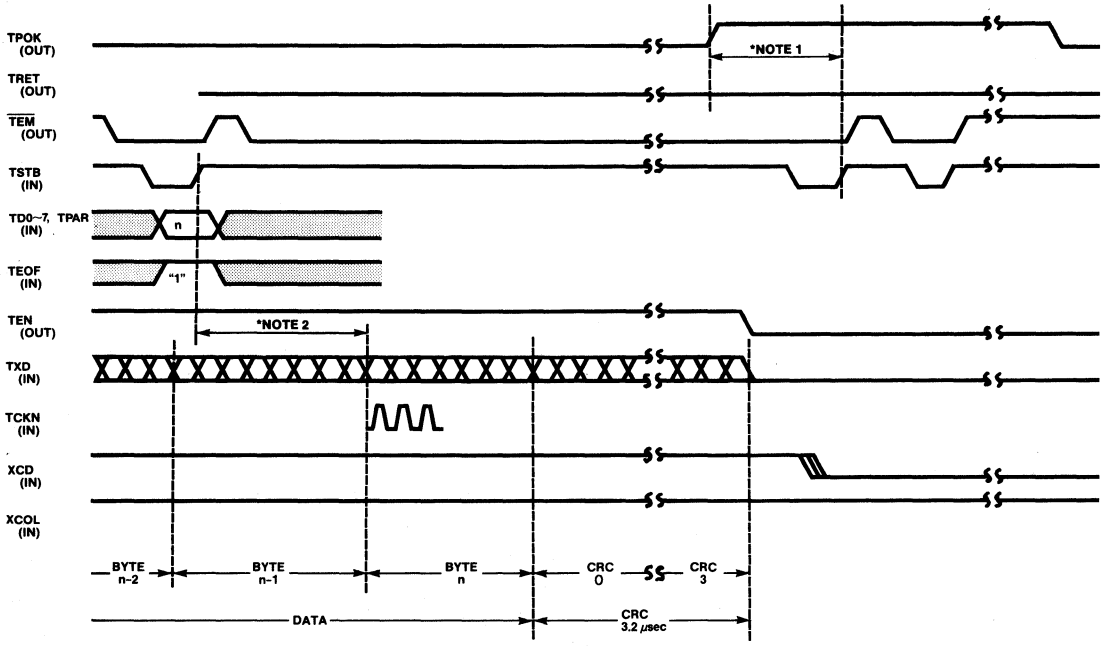
Transmit Good Packet (1)



***Note 1:** This period could be as great as 1½ byte times.

Timing Diagram
(Continued)

Transmit Good Packet (2)



***Note 1:** Must be less than ≈ 5.0 μ sec. to guarantee minimum packet spacing.
***Note 2:** This could be ½-2½ byte times.

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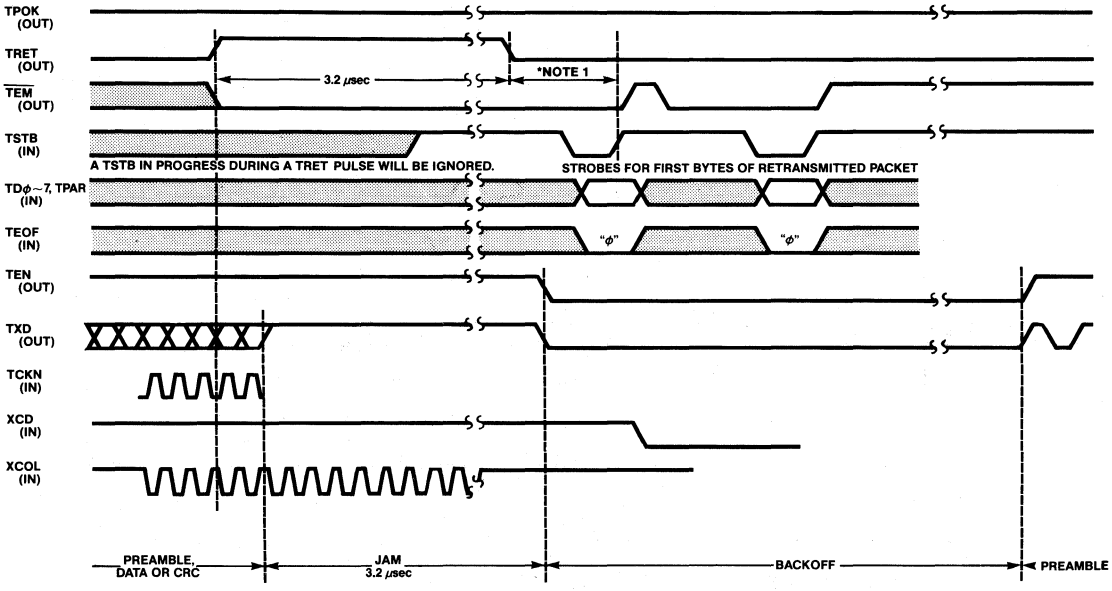
Timing Diagram
(Continued)

Transmit Collision—First Fifteen Collisions only



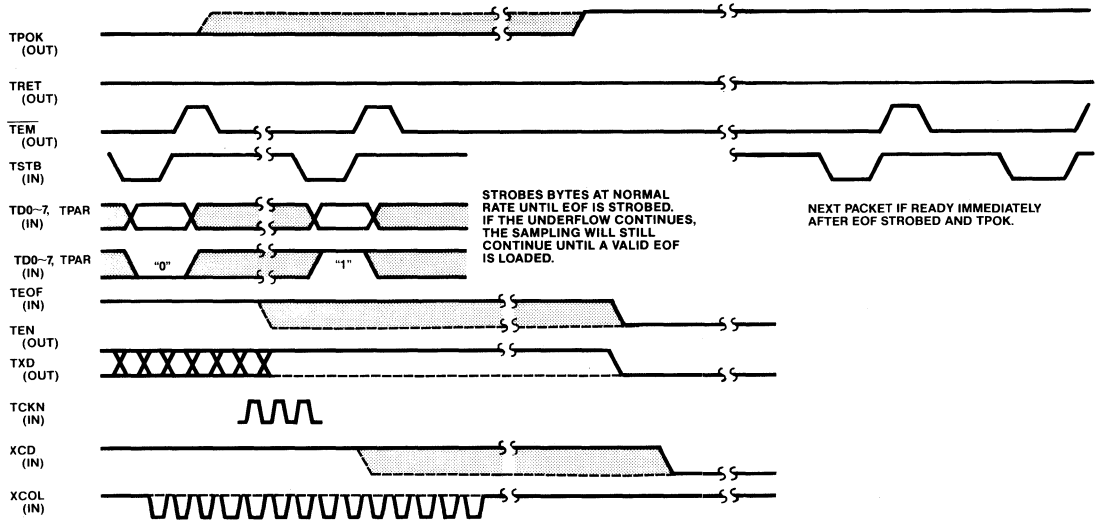
TRANSMIT 16TH COLLISION, PARITY ERROR, UNDERFLOW ERROR
- SOLID LINES INDICATE 16TH COLLISION.
- DOTTED LINES INDICATE PARITY ERROR OR UNDERFLOW ERROR.

***Note 1:** Must be less than ≈ 5.0 μ sec. to guarantee minimum backoff time.

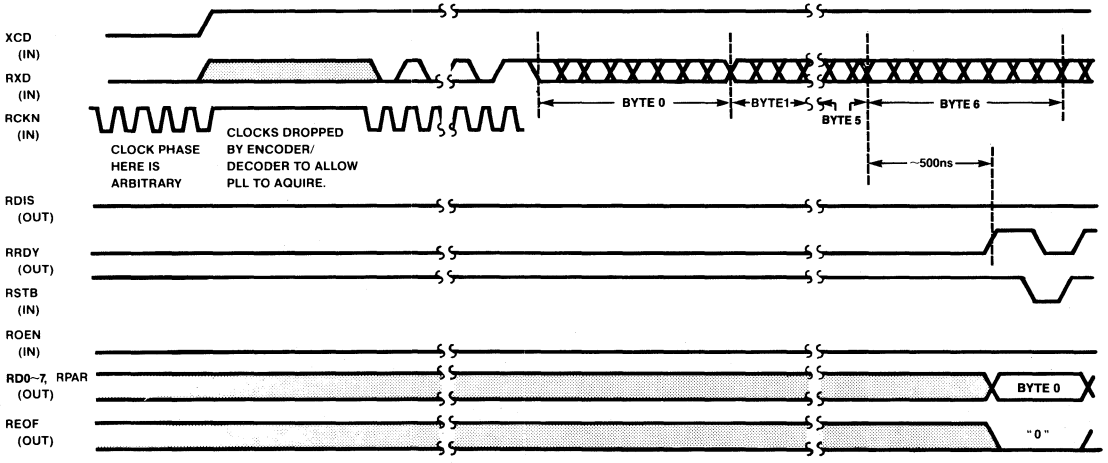
Timing Diagram
(Continued)

Transmit 16th Collision, Parity Error, Underflow Error

- **Solid lines indicate 16th collision.**
- **Dotted lines indicate parity error or underflow error.**

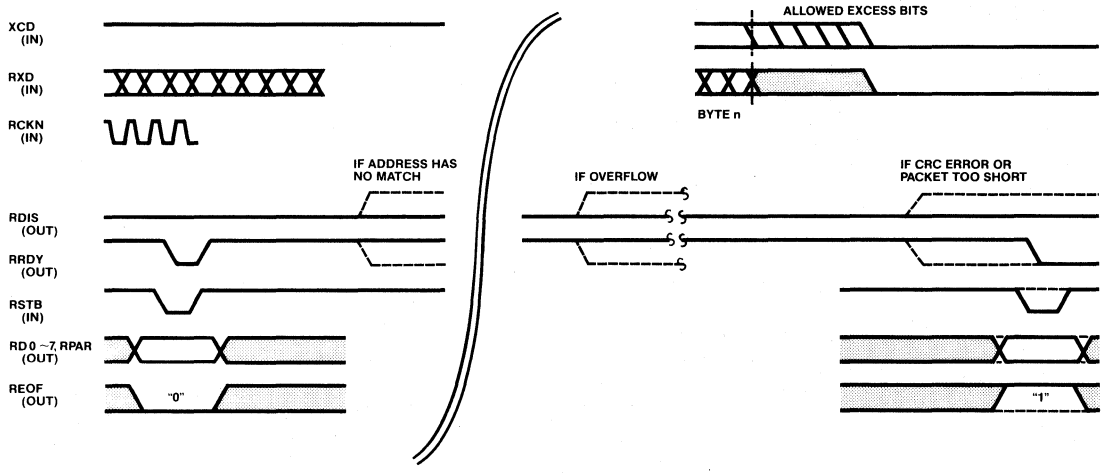


Receive

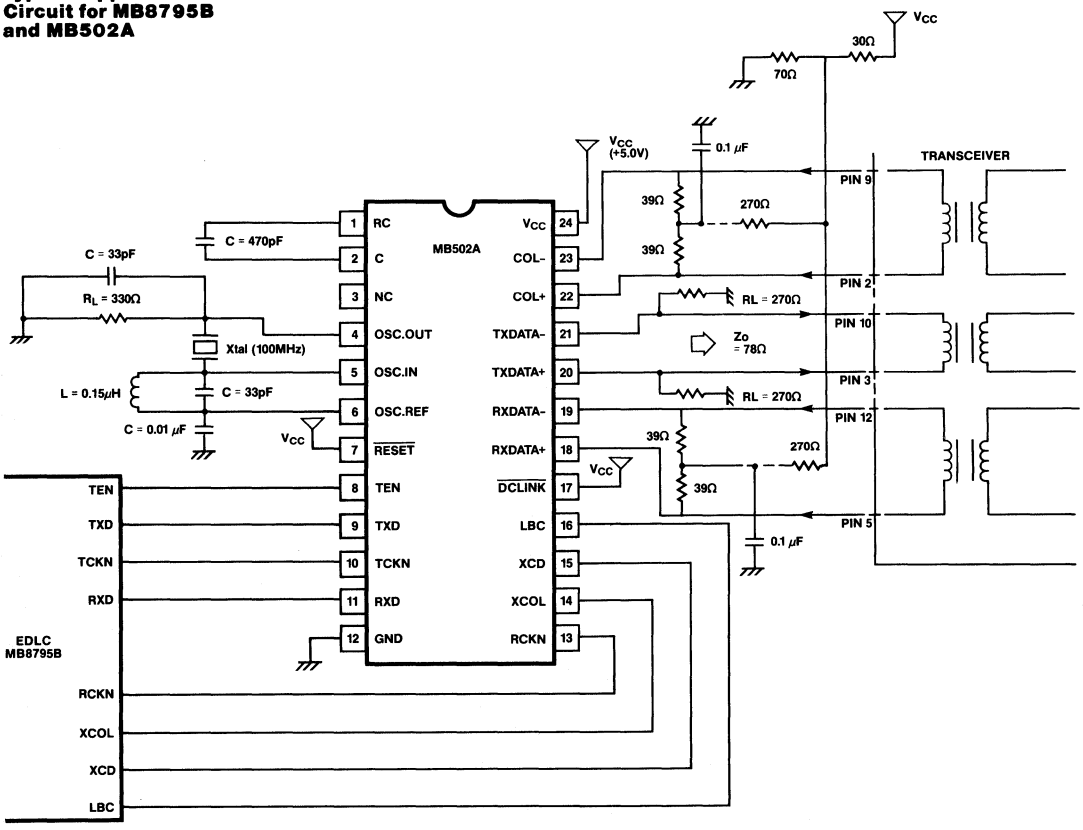


Timing Diagram
(Continued)

Receive—Address Mismatch, Overflow Error, CRC Error, Packet Length Error



Typical Application Circuit for MB8795B and MB502A



Package Dimensions
Dimensions in inches
(millimeters)

64-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-64C-A02)