

Memory FRAM

CMOS

2 M Bit (256 K × 8)

MB85R2001

■ DESCRIPTIONS

The MB85R2001 is an FRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 8 bits of non-volatile memory cells created using ferroelectric process and silicon gate CMOS process technologies.

The MB85R2001 is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85R2001 can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.

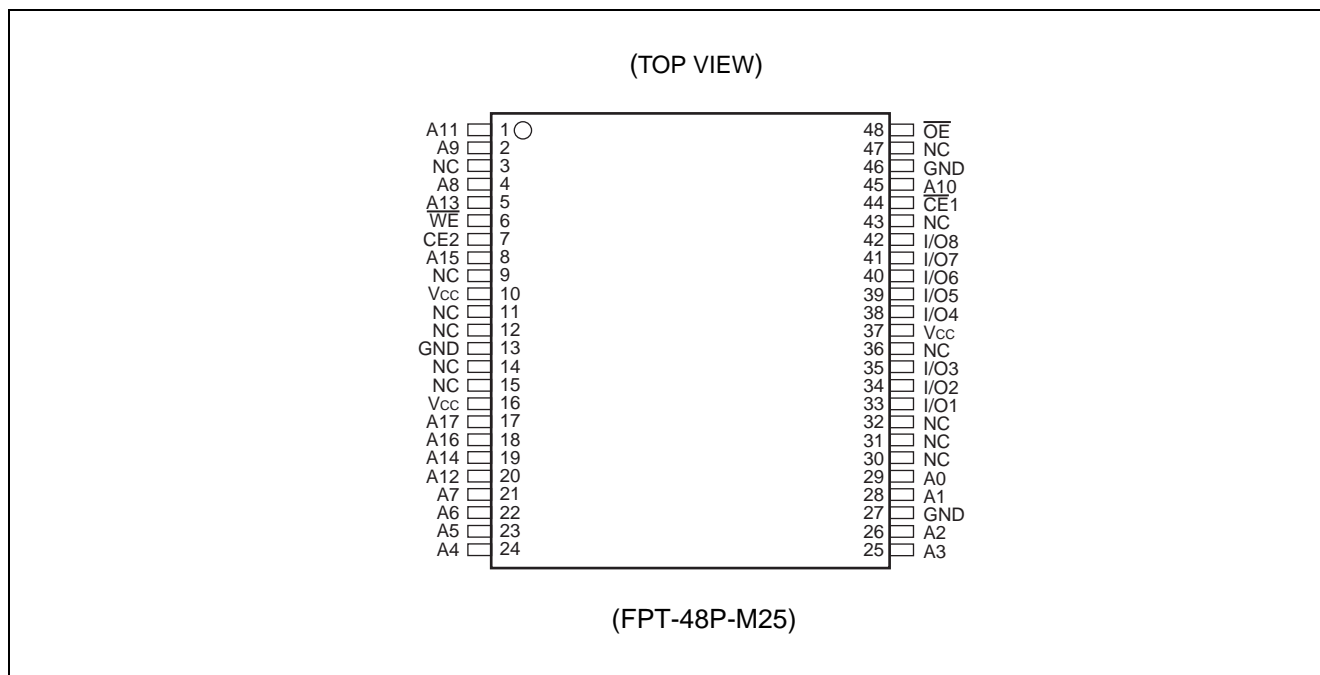
The MB85R2001 uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

■ FEATURES

- Bit configuration : 262,144 words × 8 bits
- Read/write endurance : 10^{10} times/bit
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : - 40 °C to + 85 °C
- Data retention : 10 years (+ 55 °C)
- Package : 48-pin plastic TSOP (1)

MB85R2001

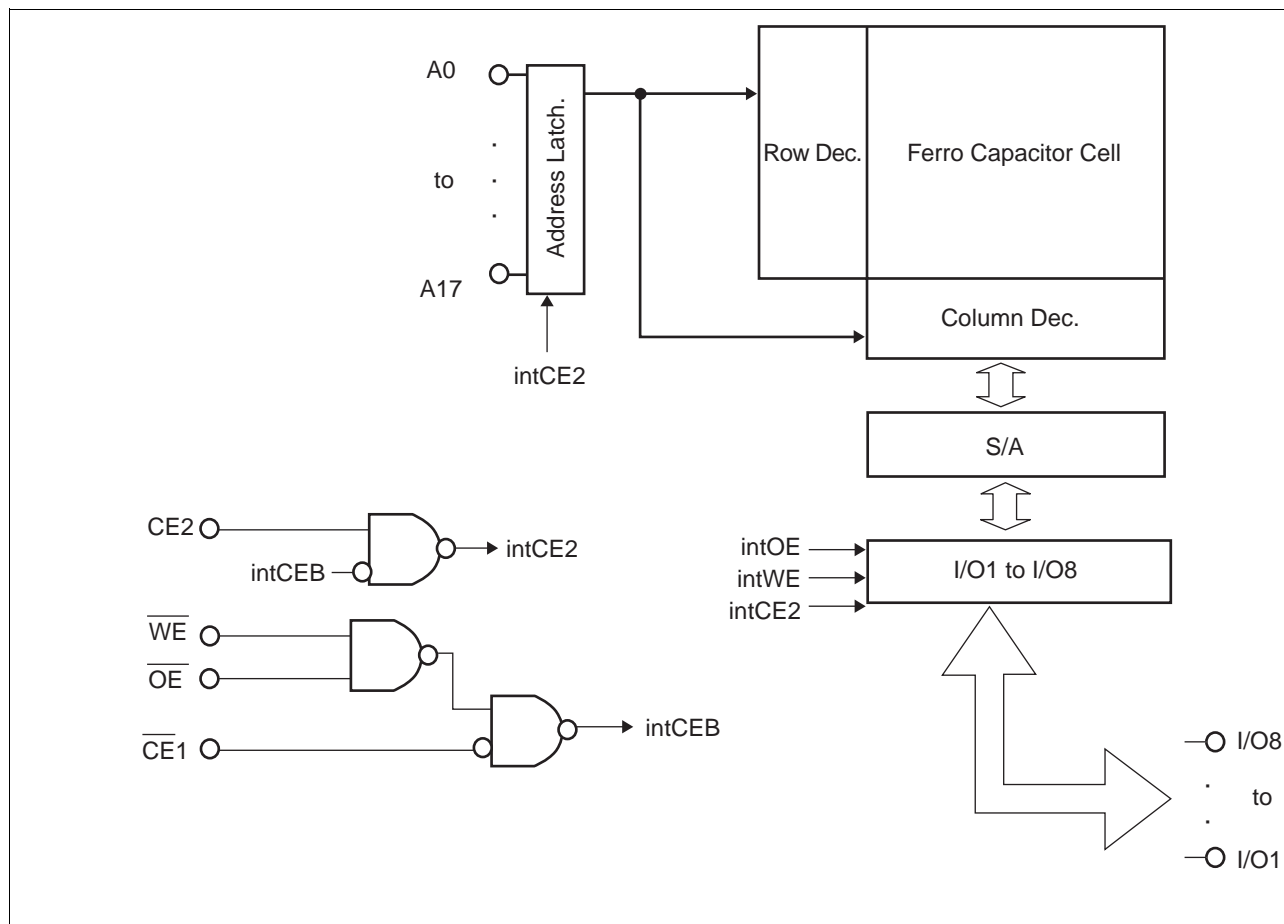
PIN ASSIGNMENTS



PIN DESCRIPTIONS

Pin name	Function
A0 to A17	Address Input
I/O1 to I/O8	Data Input/Output
$\overline{CE}1$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
Vcc	Power Supply
GND	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Operation Mode	$\overline{CE1}$	CE2	\overline{WE}	\overline{OE}	I/O1 to I/O8	Supply Current
Standby Pre-charge	H	X	X	X	High-Z	Standby (I _{SB})
	X	L	X	X		
	X	X	H	H		
Read	$\overline{\downarrow}$ L	H \uparrow	H	L	Dout	Operation (I _{CC})
Read (Pseudo-SRAM, \overline{OE} control*1)	L	H	H	$\overline{\downarrow}$		
Write	$\overline{\downarrow}$ L	H \uparrow	L	H	Din	
Write (Pseudo-SRAM, \overline{WE} control*2)	L	H	$\overline{\downarrow}$	H		

L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

$\overline{\downarrow}$: Latch address and latch data at falling edge, \uparrow : Latch address and latch data at rising edge

*1 : \overline{OE} control of the Pseudo-SRAM means the valid address at the falling edge of \overline{OE} to read.

*2 : \overline{WE} control of the Pseudo-SRAM means the valid address and data at the falling edge of \overline{WE} to write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage*	V_{CC}	-0.5	+4.0	V
Input Voltage*	V_{IN}	-0.5	$V_{CC} + 0.5$	V
Output Voltage*	V_{OUT}	-0.5	$V_{CC} + 0.5$	V
Ambient Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{stg}	-40	+125	°C

* : All voltages are referenced to GND = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage*	V_{CC}	3.0	3.3	3.6	V
Input Voltage (high)*	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.5$	V
Input Voltage (low)*	V_{IL}	-0.5	—	+0.8	V
Operating Temperature	T_A	-40	—	+85	°C

* : All voltages are referenced to GND = 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

WARNING:

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$ I_{LI} $	$V_{IN} = 0\text{ V to }V_{CC}$	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{CC}$, $\overline{CE}1 = V_{IH}$ or $\overline{OE} = V_{IH}$	—	—	10	μA
Supply Current	I_{CC}	$\overline{CE}1 = 0.2\text{ V}$, $CE2 = V_{CC} - 0.2\text{ V}$, $I_{OUT} = 0\text{ mA}^{*1}$	—	10	15	mA
Standby Current	I_{SB}	$\overline{CE}1 \geq V_{CC} - 0.2\text{ V}$	—	10	50	μA
		$CE2 \leq 0.2\text{ V}^{*2}$				
		$\overline{OE} \geq V_{CC} - 0.2\text{ V}$, $\overline{WE} \geq V_{CC} - 0.2\text{ V}^{*2}$				
Output Voltage (high)	V_{OH}	$I_{OH} = -2.0\text{ mA}$	$V_{CC} \times 0.8$	—	—	V
Output Voltage (low)	V_{OL}	$I_{OL} = 2.0\text{ mA}$	—	—	0.4	V

*1 : During the measurement of I_{CC} , the Address, Data In were taken to only change once per active cycle.
 I_{OUT} : output current

*2 : All pins other than setting pins should be input at the CMOS level voltages such as $H \geq V_{CC} - 0.2\text{ V}$, $L \leq 0.2\text{ V}$.

2. AC CHARACTERISTICS

• AC TEST CONDITIONS

Supply Voltage	: 3.0 V to 3.6 V
Operating Temperature	: -40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Impedance	: 50 pF

(1) Read Operation

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle Time	t_{RC}	150	—	ns
$\overline{CE1}$ Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
\overline{OE} Active Time	t_{RP}	120	—	ns
Pre-charge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	5	—	ns
Address Hold Time	t_{AH}	50	—	ns
\overline{OE} Setup Time	t_{ES}	5	—	ns
Output Hold Time	t_{OH}	0	—	ns
Output Set Time	t_{LZ}	30	—	ns
$\overline{CE1}$ Access Time	t_{CE1}	—	100	ns
CE2 Access Time	t_{CE2}	—	100	ns
\overline{OE} Access Time	t_{OE}	—	100	ns
Output Floating Time	t_{OHZ}	—	20	ns

(2) Write Operation

(within recommended operating conditions)

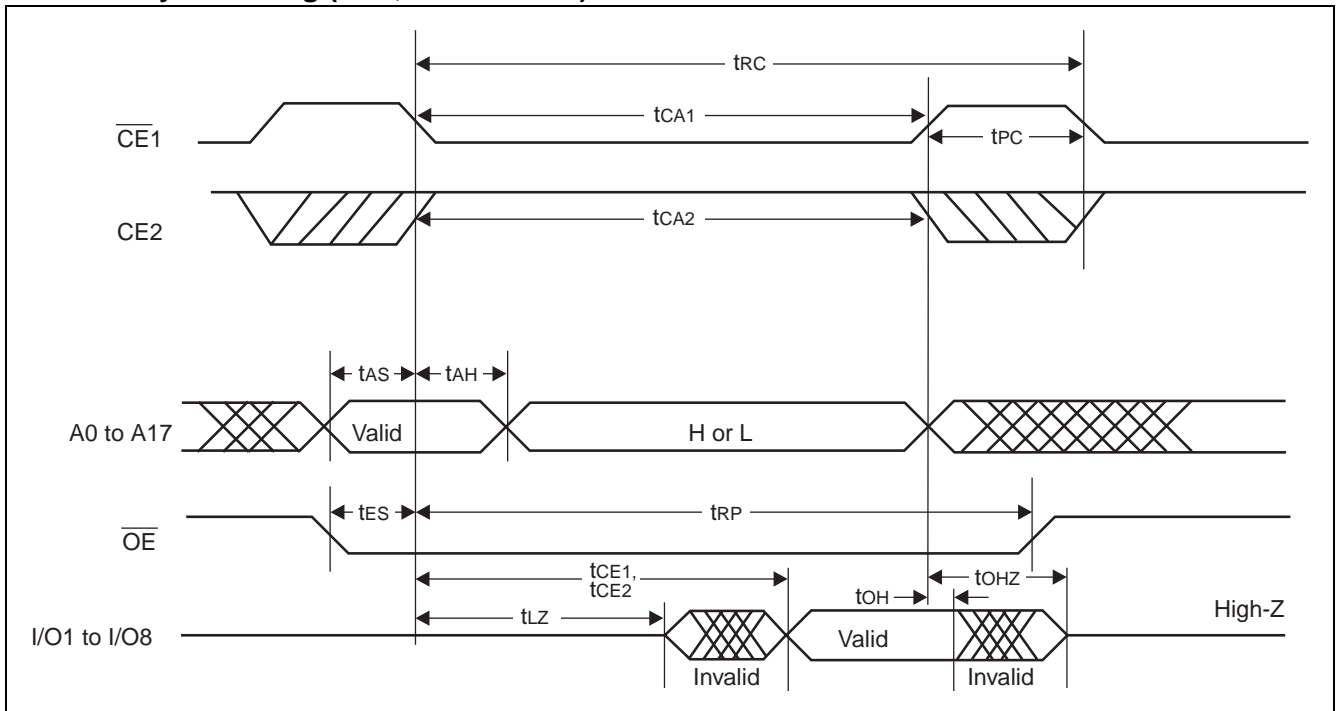
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	150	—	ns
$\overline{CE1}$ Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
Pre-charge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	5	—	ns
Address Hold Time	t_{AH}	50	—	ns
Write Pulse Width	t_{WP}	120	—	ns
Data Setup Time	t_{DS}	0	—	ns
Data Hold Time	t_{DH}	50	—	ns
Write Setup Time	t_{WS}	5	—	ns

3. Pin Capacitance

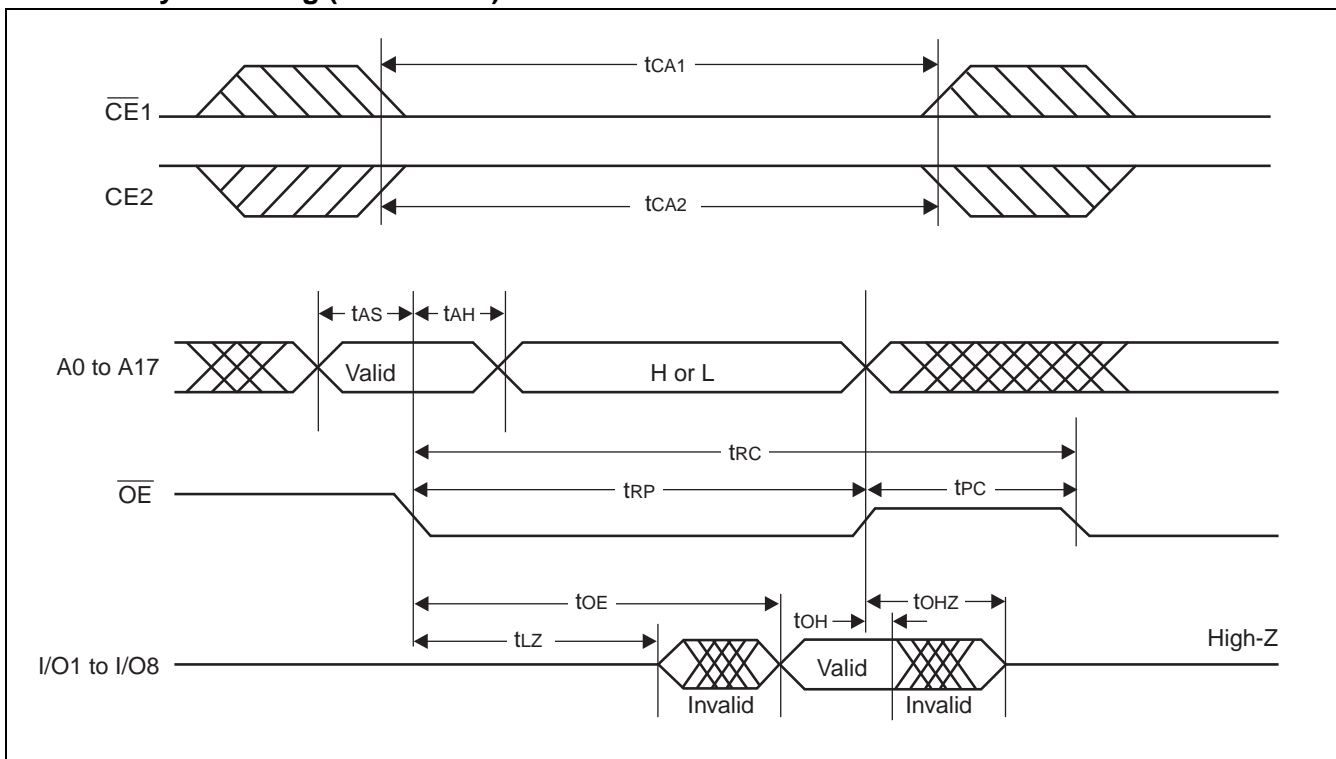
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = V_{OUT} = GND$ $f = 1\text{ MHz}$, $T_A = +25\text{ }^{\circ}\text{C}$	—	—	10	pF
Output Capacitance	C_{OUT}		—	—	10	pF

■ TIMING DIAGRAMS

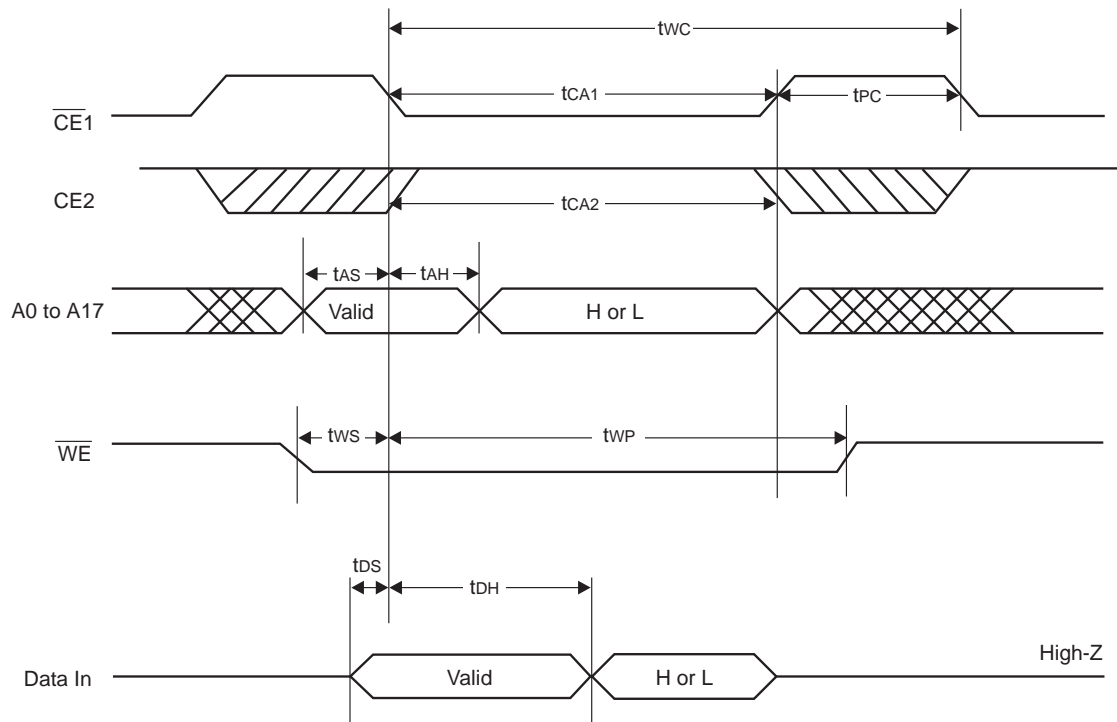
1. Read Cycle Timing ($\overline{\text{CE1}}$, CE2 Control)



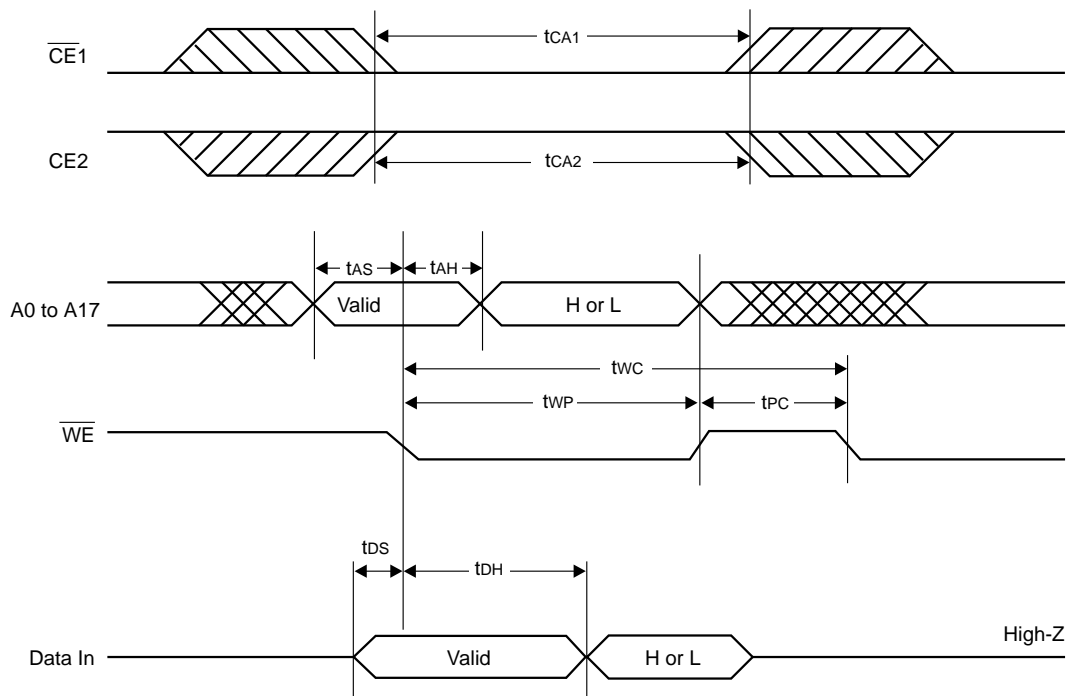
2. Read Cycle Timing ($\overline{\text{OE}}$ Control)



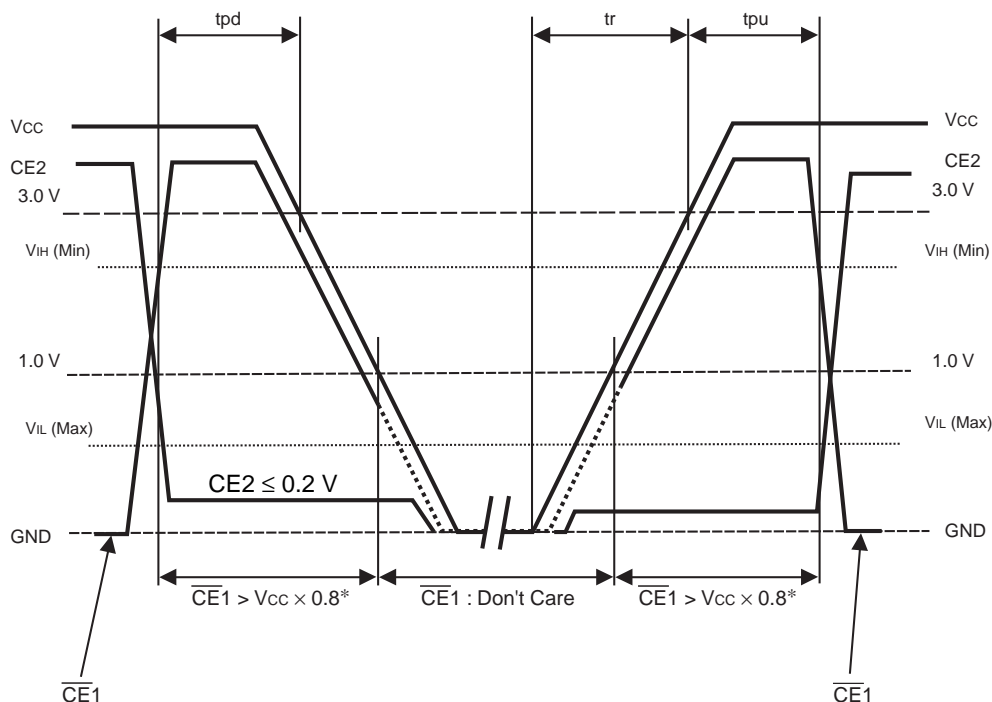
3. Write Cycle Timing ($\overline{\text{CE1}}$, CE2 Control)



4. Write Cycle Timing ($\overline{\text{WE}}$ Control)



POWER ON/OFF SEQUENCE



* : $\overline{CE1} \text{ (Max)} < V_{CC} + 0.5 \text{ V}$

- Notes:
- Use either of $\overline{CE1}$ or CE2, or both for disenable control of the device.
 - Because turning the power-on from an intermediate level cause malfunction, when the power is turned on, V_{CC} is required to be started from 0 V.
 - If the device does not operate within the specified conditions of read cycle, write cycle, power on/off sequence, memory data can not be guaranteed.

(within recommended operating conditions)

Parameter	Sym- bol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ level hold time for Power OFF	t_{pd}	85	—	—	ns
$\overline{CE1}$ level hold time for Power ON	t_{pu}	85	—	—	ns
Power supply rising time	t_r	0.05	—	200	ms

NOTES ON USE

After the IR reflow completed, it is not guaranteed to save the data written prior to the IR reflow.

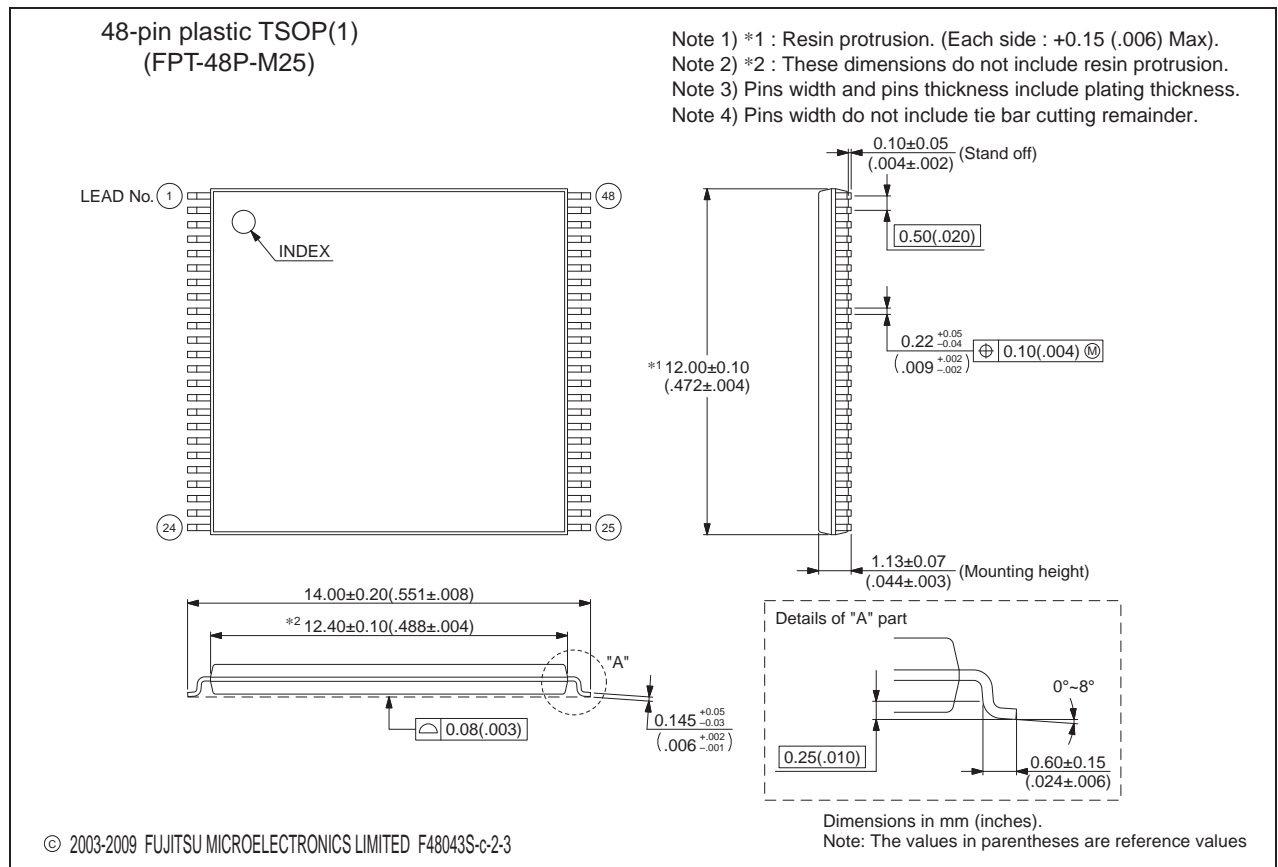
ORDERING INFORMATION

Part number	Package
MB85R2001PFTN-GE1	48-pin plastic TSOP(1) (FPT-48P-M25)

MB85R2001

■ PACKAGE DIMENSIONS

<p>48-pin plastic TSOP(1)</p> <p>(FPT-48P-M25)</p>	Lead pitch	0.50 mm
	Package width × package length	12.00 × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.37 g
	Code (Reference)	P-TSOP(1)48-12×12.4-0.50



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

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FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,

Shinjuku-ku, Tokyo 163-0722, Japan

Tel: +81-3-5322-3329

<http://jp.fujitsu.com/fml/en/>

For further information please contact:

North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://www.fma.fujitsu.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel : +65-6281-0770 Fax : +65-6281-0220

<http://www.fmal.fujitsu.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/microelectronics/>

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),

Shanghai 200002, China

Tel : +86-21-6146-3688 Fax : +86-21-6335-1605

<http://cn.fujitsu.com/fmc/>

Korea

FUJITSU MICROELECTRONICS KOREA LTD.

206 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fmk/>

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,

Tsimshatsui, Kowloon, Hong Kong

Tel : +852-2377-0226 Fax : +852-2376-3269

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